

## Selection Guide

Part Number	Packing*	Package
A4937KLPTR-A-T	4000 pieces per 13-in. reel	4.4 mm × 9.7 mm, 1.2 mm maximum height TSSOP with exposed thermal pad



\*Contact Allegro™ for additional packing options.

## Absolute Maximum Ratings\*

Characteristic	Symbol	Notes	Rating	Unit
Load Supply Voltage	$V_{BB}$		−0.3 to 50	V
Logic Supply Voltage	$V_{DD}$		−0.3 to 6	V
Terminal VREG	$V_{REG}$		−0.3 to 16	V
Terminal CP1	$V_{CP1}$		−0.3 to 16	V
Terminal CP2	$V_{CP2}$		$V_{CP1} - 0.3$ to $V_{REG} + 0.3$	V
Logic Inputs	$V_I$	STRn, SCK, SDI, PWMH, PWML	−0.3 to 6	V
		RESETh; can be pulled to $V_{BB}$ with >22 kΩ	−0.3 to 6	V
Logic Outputs	$V_O$	SDO	−0.3 to $V_{DD} + 0.3$	V
Terminal DIAG	$V_{DIAG}$		−0.3 to $V_{DD} + 0.3$	V
Terminal VBRG	$V_{BRG}$		−5 to 55	V
Terminals CA, CB, CC	$V_{Cx}$		−0.3 to $V_{REG} + 50$	V
Terminals GHA, GHB, GHC	$V_{GHx}$		$V_{Cx} - 16$ to $V_{Cx} + 0.3$	V
Terminals SA, SB, SC	$V_{Sx}$		$V_{Cx} - 16$ to $V_{Cx} + 0.3$	V
Terminals GLA, GLB, GLC	$V_{GLx}$		$V_{REG} - 16$ to 18	V
Terminal LSS	$V_{LSS}$		$V_{REG} - 16$ to 18	V
Ambient Operating Temperature Range	$T_A$	Limited by power dissipation	−40 to 150	°C
Maximum Continuous Junction Temperature	$T_J(\text{max})$		150	°C
Transient Junction Temperature	$T_{tj}$	Overtemperature event not exceeding 10s, lifetime duration not exceeding 10 hours, guaranteed by design characterization.	175	°C
Storage Temperature Range	$T_{stg}$		−55 to 150	°C

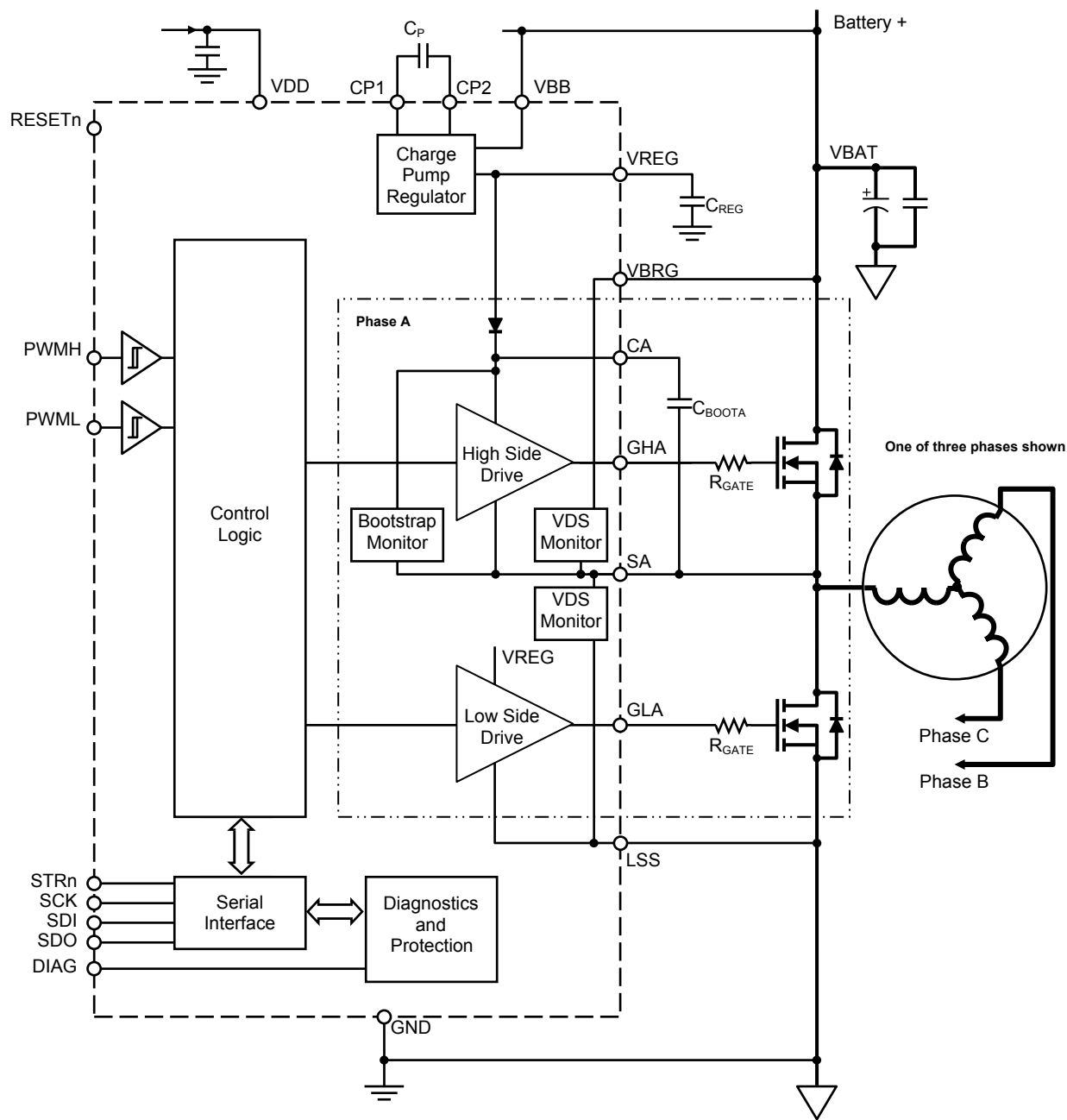
\*With respect to GND. Ratings apply when no other circuit operating constraints are present.

## Thermal Characteristics may require derating at maximum conditions

Characteristic	Symbol	Test Conditions*	Value	Unit
Package Thermal Resistance (Junction to Ambient)	$R_{\theta JA}$	On 4-layer PCB based on JEDEC standard	28	°C/W
		2-layer PCB with 3.8 in. <sup>2</sup> of copper area each side	32	°C/W
Package Thermal Resistance (Junction to Pad)	$R_{\theta JP}$		2	°C/W

\*Additional thermal information available on the Allegro website.

Functional Block Diagram



**Revision Table**

Number	Date	Description
2	January 29, 2019	Minor editorial updates
3	February 6, 2020	Minor editorial updates

Copyright 2020, Allegro MicroSystems.

Allegro MicroSystems reserves the right to make, from time to time, such departures from the detail specifications as may be required to permit improvements in the performance, reliability, or manufacturability of its products. Before placing an order, the user is cautioned to verify that the information being relied upon is current.

Allegro's products are not to be used in any devices or systems, including but not limited to life support devices or systems, in which a failure of Allegro's product can reasonably be expected to cause bodily harm.

The information included herein is believed to be accurate and reliable. However, Allegro MicroSystems assumes no responsibility for its use; nor for any infringement of patents or other rights of third parties which may result from its use.

Copies of this document are considered uncontrolled documents.