

74AC377, 74ACT377

Octal D-Type Flip-Flop with Clock Enable

Features

- I_{CC} reduced by 50%
- Ideal for addressable register applications
- Clock enable for address and data synchronization applications
- Eight edge-triggered D-type flip-flops
- Buffered common clock
- Outputs source/sink 24mA
- See 273 for master reset version
- See 373 for transparent latch version
- See 374 for 3-STATE version
- ACT377 has TTL-compatible inputs

General Description

The AC/ACT377 has eight edge-triggered, D-type flip-flops with individual D inputs and Q outputs. The common buffered Clock (CP) input loads all flip-flops simultaneously, when the Clock Enable ($\overline{CE}$) is LOW.

The register is fully edge-triggered. The state of each D input, one setup time before the LOW-to-HIGH clock transition, is transferred to the corresponding flip-flop's Q output. The $\overline{CE}$ input must be stable only one setup time prior to the LOW-to-HIGH clock transition for predictable operation.

Ordering Information

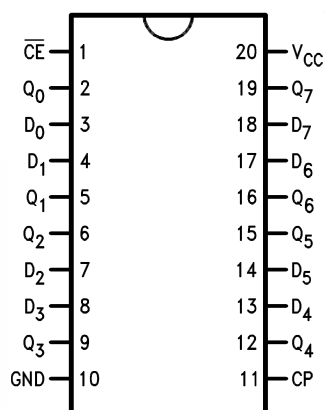
Order Number	Package Number	Package Description
74AC377SC	M20B	20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide
74AC377SJ	M20D	20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74AC377MTC	MTC20	20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
74ACT377SC	M20B	20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide
74ACT377SJ	M20D	20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74ACT377MTC	MTC20	20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
74ACT377PC	N20A	20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

Device also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering number.



All packages are lead free per JEDEC: J-STD-020B standard.

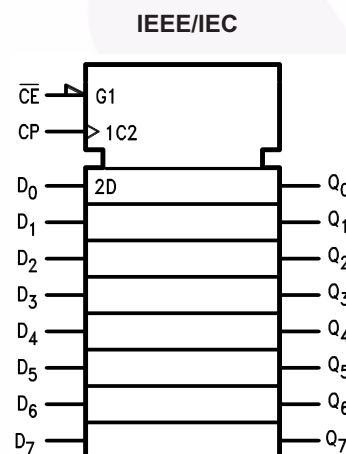
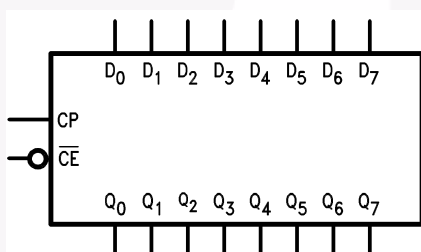
Connection Diagram



Pin Descriptions

Pin Names	Description
D ₀ –D ₇	Data Inputs
$\overline{CE}$	Clock Enable (Active LOW)
Q ₀ –Q ₇	Data Outputs
CP	Clock Pulse Input

Logic Symbols



Mode Select-Function Table

Operating Mode	Inputs			Outputs
	CP	$\overline{CE}$	D _n	Q _n
Load '1'	⌈	L	H	H
Load '0'	⌈	L	L	L
Hold (Do Nothing)	⌈	H	X	No Change
	X	H	X	No Change

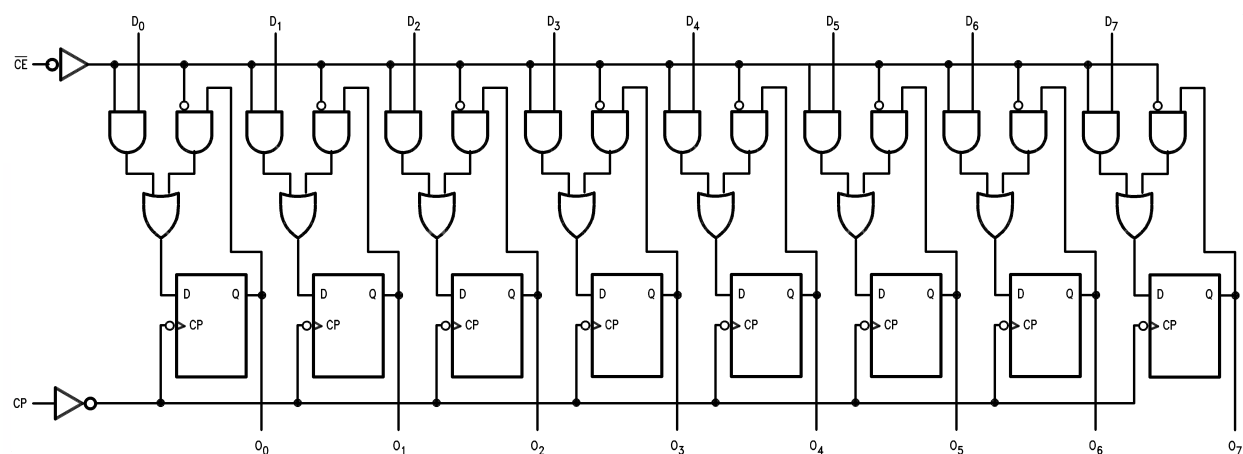
H = HIGH Voltage Level

L = LOW Voltage Level

X = Immaterial

⌈ = LOW-to-HIGH Clock Transition

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter	Rating
V_{CC}	Supply Voltage	−0.5V to +7.0V
I_{IK}	DC Input Diode Current $V_I = -0.5V$ $V_I = V_{CC} + 0.5V$	−20mA +20mA
V_I	DC Input Voltage	−0.5V to $V_{CC} + 0.5V$
I_{OK}	DC Output Diode Current $V_O = -0.5V$ $V_O = V_{CC} + 0.5V$	−20mA +20mA
V_O	DC Output Voltage	−0.5V to $V_{CC} + 0.5V$
I_O	DC Output Source or Sink Current	±50mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current per Output Pin	±50mA
T_{STG}	Storage Temperature	−65°C to +150°C
T_J	Junction Temperature	140°C

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to absolute maximum ratings.

Symbol	Parameter	Rating
V_{CC}	Supply Voltage AC ACT	2.0V to 6.0V 4.5V to 5.5V
V_I	Input Voltage	0V to V_{CC}
V_O	Output Voltage	0V to V_{CC}
T_A	Operating Temperature	−40°C to +85°C
$\Delta V / \Delta t$	Minimum Input Edge Rate, AC Devices: V_{IN} from 30% to 70% of V_{CC} , V_{CC} @ 3.3V, 4.5V, 5.5V	125mV/ns
$\Delta V / \Delta t$	Minimum Input Edge Rate, ACT Devices: V_{IN} from 0.8V to 2.0V, V_{CC} @ 4.5V, 5.5V	125mV/ns

DC Electrical Characteristics for AC

Symbol	Parameter	V _{CC} (V)	Conditions	T _A = +25°C		T _A = −40°C to +85°C		Units
				Typ.	Guaranteed Limits			
V _{IH}	Minimum HIGH Level Input Voltage	3.0	V _{OUT} = 0.1V or V _{CC} − 0.1V	1.5	2.1	2.1		V
		4.5		2.25	3.15	3.15		
		5.5		2.75	3.85	3.85		
V _{IL}	Maximum LOW Level Input Voltage	3.0	V _{OUT} = 0.1V or V _{CC} − 0.1V	1.5	0.9	0.9		V
		4.5		2.25	1.35	1.35		
		5.5		2.75	1.65	1.65		
V _{OH}	Minimum HIGH Level Output Voltage	3.0	I _{OUT} = −50μA	2.99	2.9	2.9		V
		4.5		4.49	4.4	4.4		
		5.5		5.49	5.4	5.4		
		3.0	V _{IN} = V _{IL} or V _{IH} , I _{OH} = −12mA		2.56	2.46		
		4.5	V _{IN} = V _{IL} or V _{IH} , I _{OH} = −24mA		3.86	3.76		
		5.5	V _{IN} = V _{IL} or V _{IH} , I _{OH} = −24mA ⁽¹⁾		4.86	4.76		
V _{OL}	Maximum LOW Level Output Voltage	3.0	I _{OUT} = 50μA	0.002	0.1	0.1		V
		4.5		0.001	0.1	0.1		
		5.5		0.001	0.1	0.1		
		3.0	V _{IN} = V _{IL} or V _{IH} , I _{OL} = 12mA		0.36	0.44		
		4.5	V _{IN} = V _{IL} or V _{IH} , I _{OL} = 24mA		0.36	0.44		
		5.5	V _{IN} = V _{IL} or V _{IH} , I _{OL} = 24mA ⁽¹⁾		0.36	0.44		
I _{IN} ⁽³⁾	Maximum Input Leakage Current	5.5	V _I = V _{CC} , GND		±0.1	±1.0		μA
I _{OLD}	Minimum Dynamic Output Current ⁽²⁾	5.5	V _{OLD} = 1.65V Max.			75		mA
I _{OHD}			V _{OHD} = 3.85V Min.			−75	mA	
I _{CC} ⁽³⁾	Maximum Quiescent Supply Current	5.5	V _{IN} = V _{CC} or GND		4.0	40.0		μA

Notes:

1. All outputs loaded; thresholds on input associated with output under test.
2. Maximum test duration 2.0ms, one output loaded at a time.
3. I_{IN} and I_{CC} @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V V_{CC}.

DC Electrical Characteristics for ACT

Symbol	Parameter	V _{CC} (V)	Conditions	T _A = +25°C		T _A = −40°C to +85°C		Units
				Typ.	Guaranteed Limits			
V _{IH}	Minimum HIGH Level Input Voltage	4.5	V _{OUT} = 0.1V or V _{CC} − 0.1V	1.5	2.0	2.0		V
		5.5		1.5	2.0	2.0		
V _{IL}	Maximum LOW Level Input Voltage	4.5	V _{OUT} = 0.1V or V _{CC} − 0.1V	1.5	0.8	0.8		V
		5.5		1.5	0.8	0.8		
V _{OH}	Minimum HIGH Level Output Voltage	4.5	I _{OUT} = −50μA	4.49	4.4	4.4		V
		5.5		5.49	5.4	5.4		
		4.5	V _{IN} = V _{IL} or V _{IH} , I _{OH} = −24mA		3.86	3.76		
		5.5	V _{IN} = V _{IL} or V _{IH} , I _{OH} = −24mA ⁽⁴⁾		4.86	4.76		
V _{OL}	Maximum LOW Level Output Voltage	4.5	I _{OUT} = 50μA	0.001	0.1	0.1		V
		5.5		0.001	0.1	0.1		
		4.5	V _{IN} = V _{IL} or V _{IH} , I _{OL} = 24mA		0.36	0.44		
		5.5	V _{IN} = V _{IL} or V _{IH} , I _{OL} = 24mA ⁽⁴⁾		0.36	0.44		
I _{IN}	Maximum Input Leakage Current	5.5	V _I = V _{CC} , GND		±0.1	± 1.0		μA
I _{CCT}	Maximum I _{CC} /Input	5.5	V _I = V _{CC} − 2.1V	0.6		1.5		mA
I _{OLD}	Minimum Dynamic Output Current ⁽⁵⁾	5.5	V _{OLD} = 1.65V Max.			75		mA
I _{OHD}			V _{OHD} = 3.85V Min.			−75		mA
I _{CC}	Maximum Quiescent Supply Current	5.5	V _{IN} = V _{CC} or GND		4.0	40.0		μA

Notes:

4. All outputs loaded; thresholds on input associated with output under test.
5. Maximum test duration 2.0ms, one output loaded at a time.

AC Electrical Characteristics for AC

Symbol	Parameter	V_{CC} (V) ⁽⁶⁾	$T_A = +25^\circ\text{C}$			$T_A = -40^\circ\text{C to } +85^\circ\text{C}$		Units
			Min.	Typ.	Max.	Min.	Max.	
f_{MAX}	Maximum Clock Frequency	3.3	90	125		75		MHz
		5.0	140	175		125		
t_{PLH}	Propagation Delay, CP to Q_n	3.3	3.0	8.0	13.0	1.5	14.0	ns
		5.0	2.0	6.0	9.0	1.5	10.0	
t_{PHL}	Propagation Delay, CP to Q_n	3.3	3.5	8.5	13.0	2.0	14.5	ns
		5.0	2.5	6.5	10.0	1.5	11.0	

Note:

6. Voltage range 3.3 is $3.3\text{V} \pm 0.3\text{V}$. Voltage range 5.0 is $5.0\text{V} \pm 0.5\text{V}$

AC Operating Requirements for AC

Symbol	Parameter	V _{CC} (V) ⁽⁷⁾	T _A = +25°C, C _L = 50pF		T _A = −40°C to +85°C, C _L = 50pF	Units
			Typ.	Guaranteed Minimum		
t _S	Setup Time, HIGH or LOW, D _n to CP	3.3	3.5	5.5	6.0	ns
		5.0	2.5	4.0	4.5	
t _H	Hold Time, HIGH or LOW, D _n to CP	3.3	−2.0	0	0	ns
		5.0	−1.0	1.0	1.0	
t _S	Setup Time, HIGH or LOW, CE to CP	3.3	4.0	6.0	7.5	ns
		5.0	2.5	4.0	4.5	
t _H	Hold Time, HIGH or LOW, CE to CP	3.3	−3.5	0	0	ns
		5.0	−2.0	1.0	1.0	
t _W	CP Pulse Width, HIGH or LOW	3.3	3.5	5.5	6.0	ns
		5.0	2.5	4.0	4.5	

Note:

7. Voltage range 3.3 is $3.0\text{V} \pm 0.3\text{V}$. Voltage range 5.0 is $5.0\text{V} \pm 0.5\text{V}$

AC Electrical Characteristics for ACT

Symbol	Parameter	V_{CC} (V) ⁽⁸⁾	$T_A = +25^\circ\text{C}$, $C_L = 50\text{pF}$			$T_A = -40^\circ\text{C to } +85^\circ\text{C}$, $C_L = 50\text{pF}$		Units
			Min.	Typ.	Max.	Min.	Max.	
f_{MAX}	Maximum Clock Frequency	5.0	140	175		125		MHz
t_{PLH}	Propagation Delay, CP to Q_n	5.0	3.0	6.5	9.0	2.5	10.0	ns
t_{PHL}	Propagation Delay, CP to Q_n	5.0	3.5	7.0	10.0	2.5	11.0	ns

Note:8. Voltage Range 5.0 is $5.0\text{V} \pm 0.5\text{V}$ **AC Operating Requirements for ACT**

Symbol	Parameter	V_{CC} (V) ⁽⁹⁾	$T_A = +25^\circ\text{C}$, $C_L = 50\text{pF}$		$T_A = -40^\circ\text{C to } +85^\circ\text{C}$, $C_L = 50\text{pF}$		Units
			Typ.	Guaranteed Minimum			
t_S	Setup Time, HIGH or LOW, D_n to CP	5.0	2.5	4.5	5.5		ns
t_H	Hold Time, HIGH or LOW, D_n to CP	5.0	-1.0	1.0	1.0		ns
t_S	Setup Time, HIGH or LOW, $\overline{\text{CE}}$ to CP	5.0	2.5	4.5	5.5		ns
t_H	Hold Time, HIGH or LOW, $\overline{\text{CE}}$ to CP	5.0	-1.0	1.0	1.0		ns
t_W	CP Pulse Width, HIGH or LOW	5.0	2.0	4.0	4.5		ns

Note:9. Voltage Range 5.0 is $5.0\text{V} \pm 0.5\text{V}$ **Capacitance**

Symbol	Parameter	Conditions	Typ.	Units
C_{IN}	Input Capacitance	$V_{CC} = \text{OPEN}$	4.5	pF
C_{PD}	Power Dissipation Capacitance	$V_{CC} = 5.0\text{V}$	90.0	pF

Physical Dimensions



Figure 1. 20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide

Package drawings are provided as a service to customers considering Fairchild components. Drawings may change in any manner without notice. Please note the revision and/or date on the drawing and contact a Fairchild Semiconductor representative to verify or obtain the most recent revision. Package specifications do not expand the terms of Fairchild's worldwide terms and conditions, specifically the warranty therein, which covers Fairchild products.

Always visit Fairchild Semiconductor's online packaging area for the most recent package drawings:

<http://www.fairchildsemi.com/packaging/>

Physical Dimensions (Continued)



M20DREVC

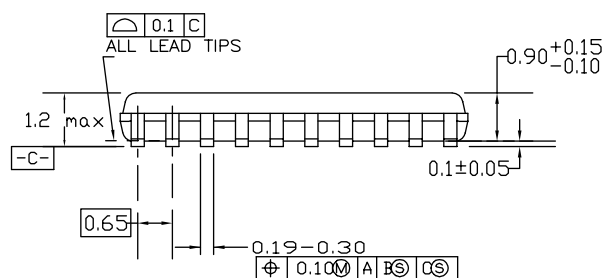
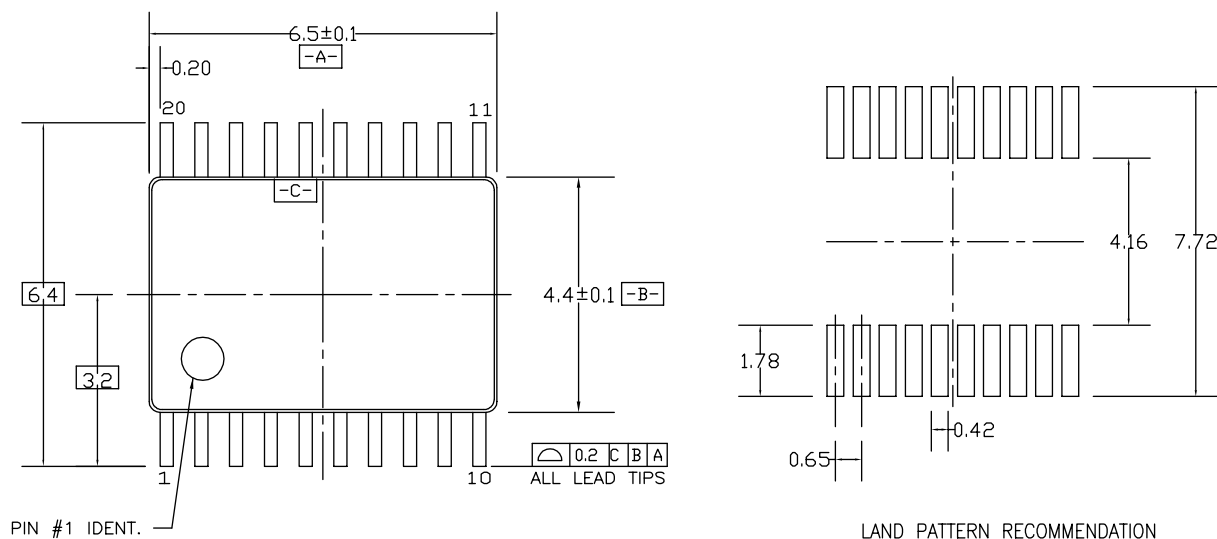
Figure 2. 20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide

Package drawings are provided as a service to customers considering Fairchild components. Drawings may change in any manner without notice. Please note the revision and/or date on the drawing and contact a Fairchild Semiconductor representative to verify or obtain the most recent revision. Package specifications do not expand the terms of Fairchild's worldwide terms and conditions, specifically the warranty therein, which covers Fairchild products.

Always visit Fairchild Semiconductor's online packaging area for the most recent package drawings:

<http://www.fairchildsemi.com/packaging/>

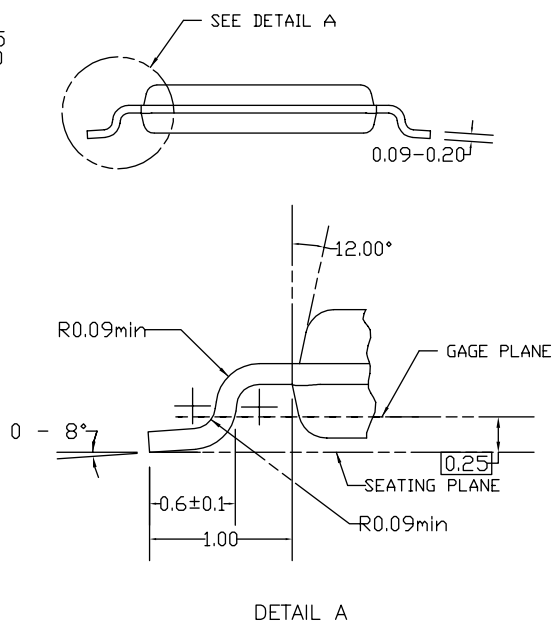
Physical Dimensions (Continued)



DIMENSIONS ARE IN MILLIMETERS

NOTES:

- CONFORMS TO JEDEC REGISTRATION MO-153, VARIATION AC, REF NOTE 6, DATE 7/93.
- DIMENSIONS ARE IN MILLIMETERS.
- DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLDS FLASH, AND TIE BAR EXTRUSIONS.
- DIMENSIONS AND TOLERANCES PER ANSI Y14.5M, 1982.



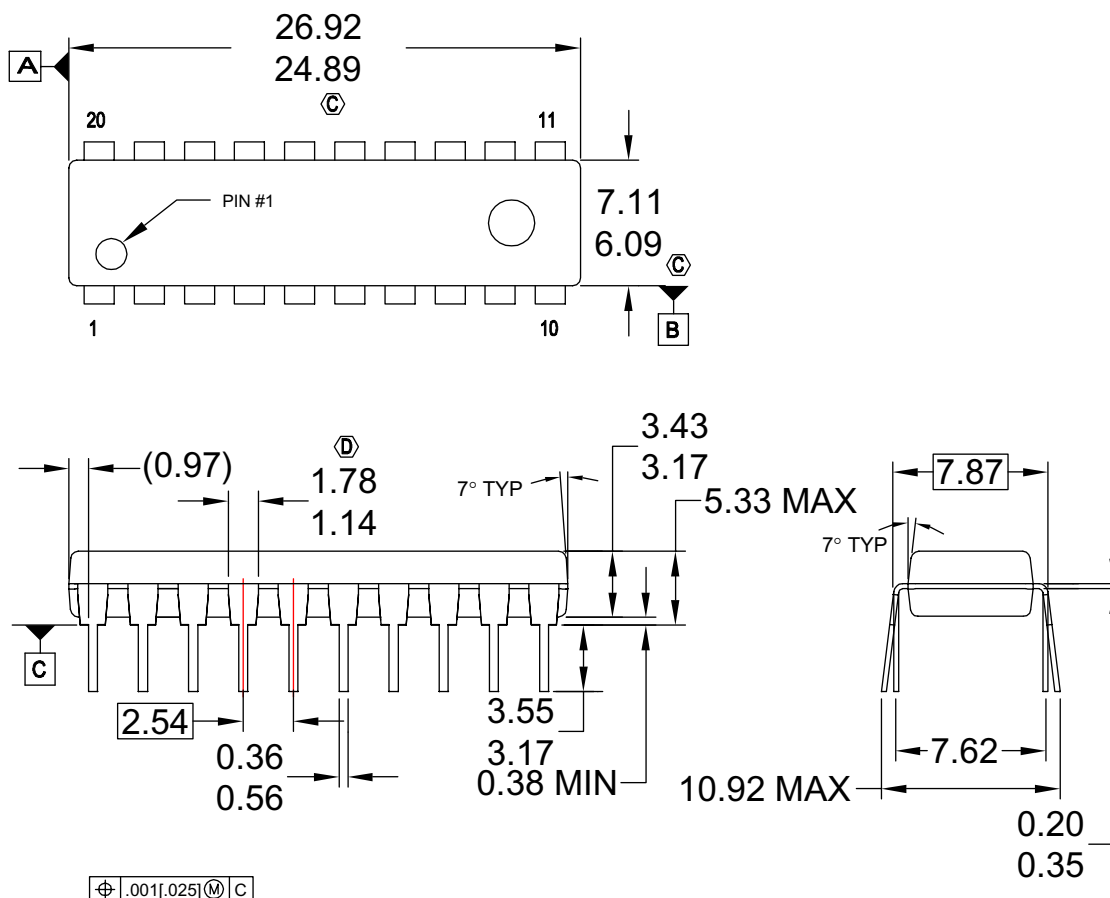
MTC20REV D1

Figure 3. 20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide

Package drawings are provided as a service to customers considering Fairchild components. Drawings may change in any manner without notice. Please note the revision and/or date on the drawing and contact a Fairchild Semiconductor representative to verify or obtain the most recent revision. Package specifications do not expand the terms of Fairchild's worldwide terms and conditions, specifically the warranty therein, which covers Fairchild products.

Always visit Fairchild Semiconductor's online packaging area for the most recent package drawings:

<http://www.fairchildsemi.com/packaging/>

Physical Dimensions (Continued)**Figure 4. 20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide**

Package drawings are provided as a service to customers considering Fairchild components. Drawings may change in any manner without notice. Please note the revision and/or date on the drawing and contact a Fairchild Semiconductor representative to verify or obtain the most recent revision. Package specifications do not expand the terms of Fairchild's worldwide terms and conditions, specifically the warranty therein, which covers Fairchild products.

Always visit Fairchild Semiconductor's online packaging area for the most recent package drawings:

<http://www.fairchildsemi.com/packaging/>



TRADEMARKS

The following includes registered and unregistered trademarks and service marks, owned by Fairchild Semiconductor and/or its global subsidiaries, and is not intended to be an exhaustive list of all such trademarks.

ACEx [®]	FPS [™]	PDP-SPM [™]	SyncFET [™]
Build it Now [™]	FRFET [®]	Power220 [®]	SYSTEM [®]
CorePLUS [™]	Global Power Resource SM	Power247 [®]	GENERAL
CROSSVOLT [™]	Green FPS [™]	POWEREDGE [®]	The Power Franchise [®]
CTL [™]	Green FPS [™] e-Series [™]	Power-SPM [™]	the power [™]
Current Transfer Logic [™]	GTO [™]	PowerTrench [®]	franchise
EcoSPARK [®]	i-Lo [™]	Programmable Active Droop [™]	TinyBoost [™]
EZSWITCH [™] *	IntelliMAX [™]	QFET [®]	TinyBuck [™]
 [™]	ISOPLANAR [™]	QST [™]	TinyLogic [®]
 [®]	MegaBuck [™]	QT Optoelectronics [™]	TINYOPTO [™]
Fairchild [®]	MICROCOUPLER [™]	Quiet Series [™]	TinyPower [™]
Fairchild Semiconductor [®]	MicroFET [™]	RapidConfigure [™]	TinyPWM [™]
FACT Quiet Series [™]	MicroPak [™]	SMART START [™]	TinyWire [™]
FACT [®]	MillerDrive [™]	SPM [®]	μSerDes [™]
FAST [®]	Motion-SPM [™]	STEALTH [™]	UHC [®]
FastvCore [™]	OPTOLOGIC [®]	SuperFET [™]	Ultra FRFET [™]
FlashWriter [®] *	OPTOPLANAR [®]	SuperSOT [™] -3	UniFET [™]
		SuperSOT [™] -6	VCX [™]
		SuperSOT [™] -8	

* EZSWITCH[™] and FlashWriter[®] are trademarks of System General Corporation, used under license by Fairchild Semiconductor.

DISCLAIMER

FAIRCHILD SEMICONDUCTOR RESERVES THE RIGHT TO MAKE CHANGES WITHOUT FURTHER NOTICE TO ANY PRODUCTS HEREIN TO IMPROVE RELIABILITY, FUNCTION, OR DESIGN. FAIRCHILD DOES NOT ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN; NEITHER DOES IT CONVEY ANY LICENSE UNDER ITS PATENT RIGHTS, NOR THE RIGHTS OF OTHERS. THESE SPECIFICATIONS DO NOT EXPAND THE TERMS OF FAIRCHILD'S WORLDWIDE TERMS AND CONDITIONS, SPECIFICALLY THE WARRANTY THEREIN, WHICH COVERS THESE PRODUCTS.

LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF FAIRCHILD SEMICONDUCTOR CORPORATION.

As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury of the user.
2. A critical component in any component of a life support, device, or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

PRODUCT STATUS DEFINITIONS

Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative or In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
Obsolete	Not In Production	This datasheet contains specifications on a product that has been discontinued by Fairchild Semiconductor. The datasheet is printed for reference information only.

Rev. I32

ON Semiconductor and  are trademarks of Semiconductor Components Industries, LLC dba ON Semiconductor or its subsidiaries in the United States and/or other countries. ON Semiconductor owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of ON Semiconductor's product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent-Marking.pdf. ON Semiconductor reserves the right to make changes without further notice to any products herein. ON Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does ON Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using ON Semiconductor products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by ON Semiconductor. "Typical" parameters which may be provided in ON Semiconductor data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. ON Semiconductor does not convey any license under its patent rights nor the rights of others. ON Semiconductor products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use ON Semiconductor products for any such unintended or unauthorized application, Buyer shall indemnify and hold ON Semiconductor and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that ON Semiconductor was negligent regarding the design or manufacture of the part. ON Semiconductor is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:

Literature Distribution Center for ON Semiconductor
19521 E. 32nd Pkwy, Aurora, Colorado 80011 USA
Phone: 303-675-2175 or 800-344-3860 Toll Free USA/Canada
Fax: 303-675-2176 or 800-344-3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800-282-9855 Toll Free
USA/Canada

Europe, Middle East and Africa Technical Support:
Phone: 421 33 790 2910

Japan Customer Focus Center
Phone: 81-3-5817-1050

ON Semiconductor Website: www.onsemi.com

Order Literature: <http://www.onsemi.com/orderlit>

For additional information, please contact your local
Sales Representative