

# 2N7000

## 1.0 ELECTRICAL CHARACTERISTICS

### Absolute Maximum Ratings†

Drain-to-Source Voltage .....	$BV_{DSS}$
Drain-to-Gate Voltage .....	$BV_{DGS}$
Gate-to-Source Voltage .....	$\pm 30V$
Operating Ambient Temperature, $T_A$ .....	$-55^{\circ}C$ to $+150^{\circ}C$
Storage Temperature, $T_S$ .....	$-55^{\circ}C$ to $+150^{\circ}C$

† **Notice:** Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not intended. Exposure to maximum rating conditions for extended periods may affect device reliability.

### DC ELECTRICAL CHARACTERISTICS

**Electrical Specifications:**  $T_A = 25^{\circ}C$  unless otherwise specified. All DC parameters are 100% tested at  $25^{\circ}C$  unless otherwise stated. (Pulse test: 300  $\mu s$  pulse, 2% duty cycle)

Parameter	Sym.	Min.	Typ.	Max.	Unit	Conditions
Drain-to-Source Breakdown Voltage	$BV_{DSS}$	60	—	—	V	$V_{GS} = 0V$ , $I_D = 10 \mu A$
Gate Threshold Voltage	$V_{GS(th)}$	0.8	—	3	V	$V_{GS} = V_{DS}$ , $I_D = 1 mA$
Gate Body Leakage Current	$I_{GSS}$	—	—	10	nA	$V_{GS} = \pm 15V$ , $V_{DS} = 0V$
Zero-Gate Voltage Drain Current	$I_{DSS}$	—	—	1	$\mu A$	$V_{GS} = 0V$ , $V_{DS} = 48V$
		—	—	1	mA	$V_{GS} = 0V$ , $V_{DS} = 48V$ , $T_A = 125^{\circ}C$ (Note 1)
On-State Drain Current	$I_{D(ON)}$	75	—	—	mA	$V_{GS} = 4.5V$ , $V_{DS} = 10V$
Static Drain-to-Source On-State Resistance	$R_{DS(ON)}$	—	—	5.3	$\Omega$	$V_{GS} = 4.5V$ , $I_D = 75 mA$
		—	—	5	$\Omega$	$V_{GS} = 10V$ , $I_D = 500 mA$

**Note 1:** Specification is obtained by characterization and is not 100% tested.

### AC ELECTRICAL CHARACTERISTICS

**Electrical Specifications:**  $T_A = 25^{\circ}C$  unless otherwise specified. All AC parameters are not 100% sample tested.

Parameter	Sym.	Min.	Typ.	Max.	Unit	Conditions
Forward Transconductance	$G_{FS}$	100	—	—	mmho	$V_{DS} = 10V$ , $I_D = 200 mA$
Input Capacitance	$C_{ISS}$	—	—	60	pF	$V_{GS} = 0V$ , $V_{DS} = 25V$ , $f = 1 MHz$
Common-Source Output Capacitance	$C_{OSS}$	—	—	25	pF	
Reverse Transfer Capacitance	$C_{RSS}$	—	—	5	pF	
Turn-On Delay Time	$t_{d(ON)}$	—	—	10	ns	$V_{DD} = 15V$ , $I_D = 500 mA$ , $R_{GEN} = 25\Omega$
Turn-Off Delay Time	$t_{d(OFF)}$	—	—	10	ns	

#### DIODE PARAMETER

Diode Forward Voltage Drop	$V_{SD}$	—	0.85	—	V	$V_{GS} = 0V$ , $I_{SD} = 200 mA$ (Note 1)
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**Note 1:** All DC parameters are 100% tested at  $25^{\circ}C$  unless otherwise stated.  
(Pulse test: 300  $\mu s$  pulse, 2% duty cycle)

## TEMPERATURE SPECIFICATIONS

**Electrical Characteristics:** Unless otherwise specified, for all specifications  $T_A = T_J = +25^\circ\text{C}$ .

Parameter	Sym.	Min.	Typ.	Max.	Unit	Conditions
<b>TEMPERATURE RANGE</b>						
Operating Ambient Temperature	$T_A$	-55	—	+150	$^\circ\text{C}$	
Storage Temperature	$T_S$	-55	—	+150	$^\circ\text{C}$	
<b>PACKAGE THERMAL RESISTANCE</b>						
3-lead TO-92	$\theta_{JA}$	—	132	—	$^\circ\text{C/W}$	

**Note 1:** Mounted on an FR4 board; 25 mm x 25 mm x 1.57 mm

## THERMAL CHARACTERISTICS

Package	$I_D$ (Note 1) (Continuous) (mA)	$I_D$ (Pulsed) (mA)	Power Dissipation at $T_C = 25^\circ\text{C}$ (W)	$I_{DR}$ (Note 1) (mA)	$I_{DRM}$ (mA)
3-lead TO-92	200	500	1	200	500

**Note 1:**  $I_D$  (continuous) is limited by maximum  $T_J$ .

2.0 TYPICAL PERFORMANCE CURVES

**Note:** The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g. outside specified power supply range) and therefore outside the warranted range.

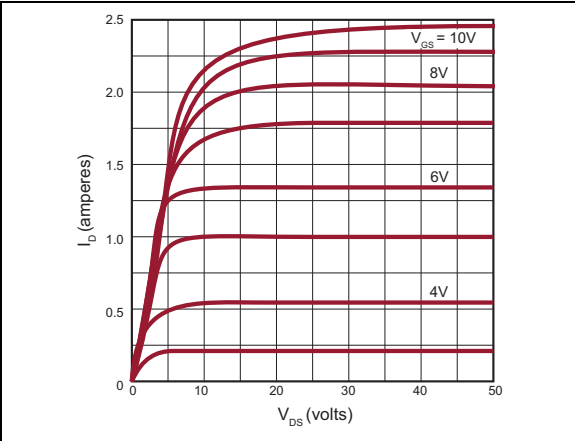


FIGURE 2-1: Output Characteristics.

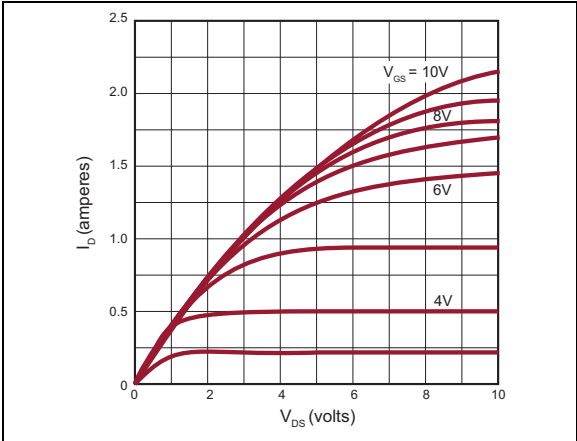


FIGURE 2-4: Saturation Characteristics.

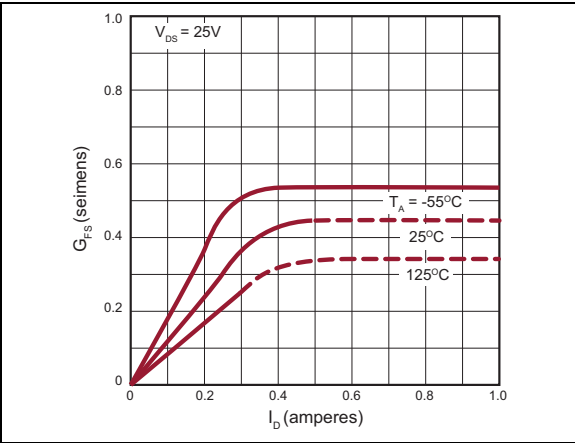


FIGURE 2-2: Transconductance vs. Drain Current.

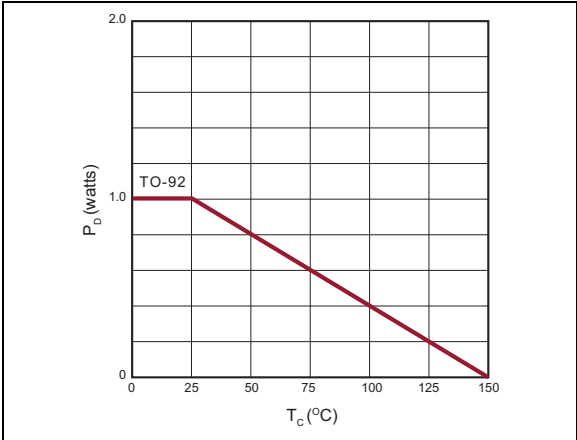


FIGURE 2-5: Power Dissipation vs. Case Temperature.

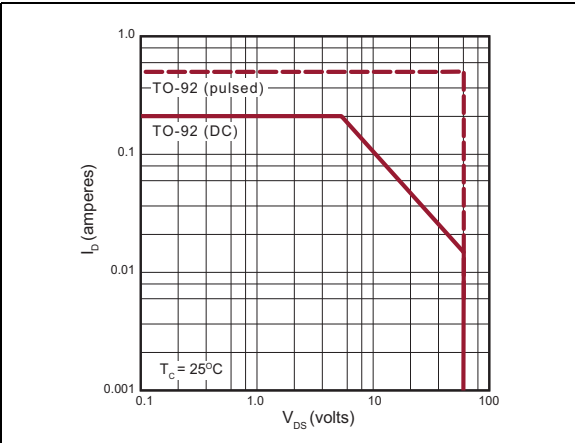


FIGURE 2-3: Maximum Rated Safe Operating Area.

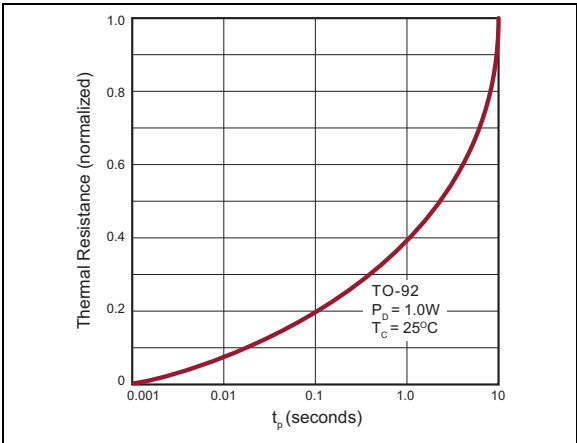
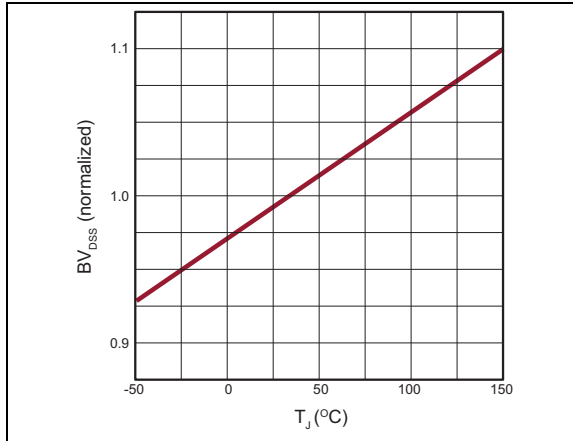
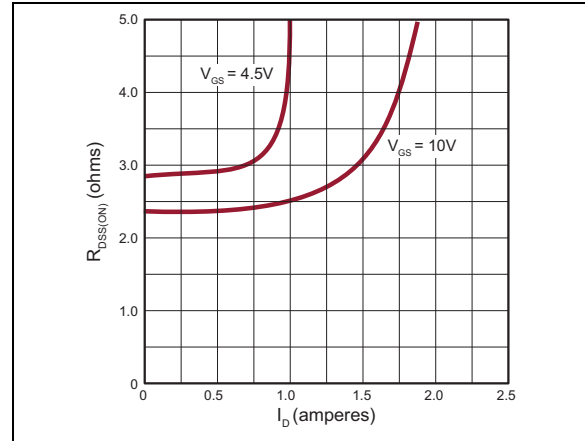


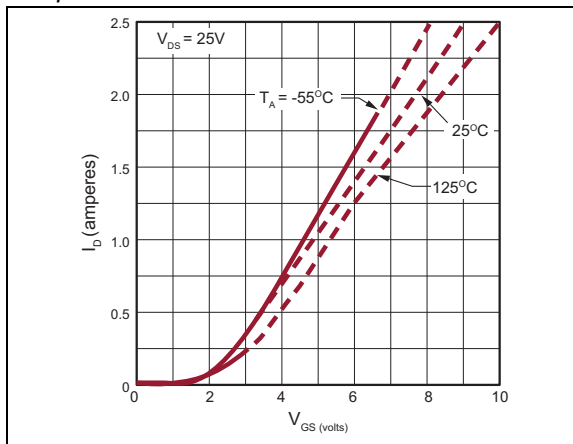
FIGURE 2-6: Thermal Response Characteristics.



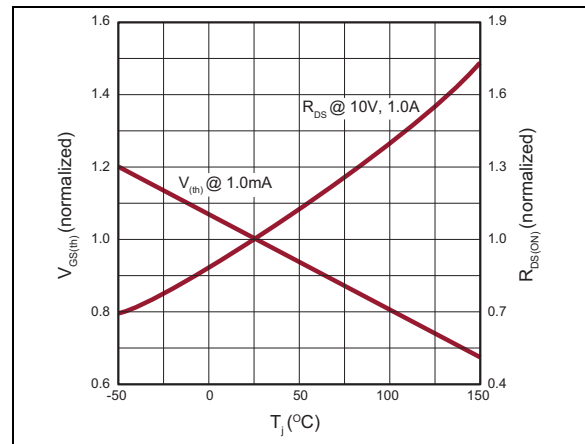
**FIGURE 2-7:**  $BV_{DSS}$  Variation with Temperature.



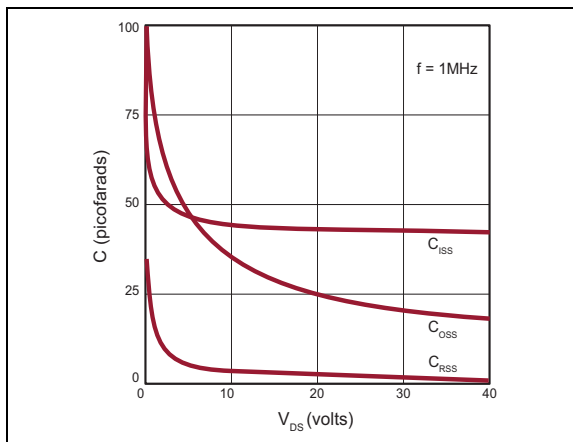
**FIGURE 2-10:** On-Resistance vs. Drain Current.



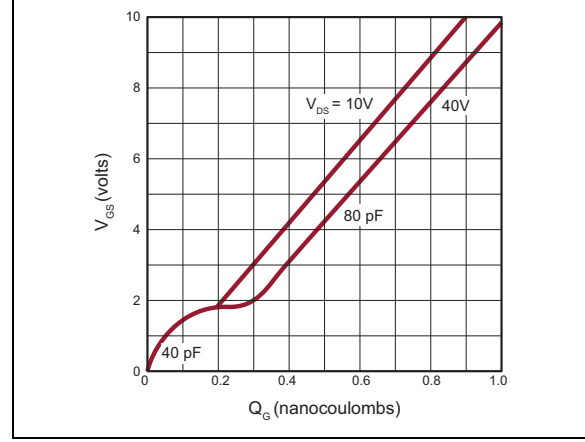
**FIGURE 2-8:** Transfer Characteristics.



**FIGURE 2-11:**  $V_{GS(th)}$  and  $R_{DS}$  Variation with Temperature.



**FIGURE 2-9:** Capacitance vs. Drain-to-Source Voltage.



**FIGURE 2-12:** Gate Drive Dynamic Characteristics.

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## 3.0 PIN DESCRIPTION

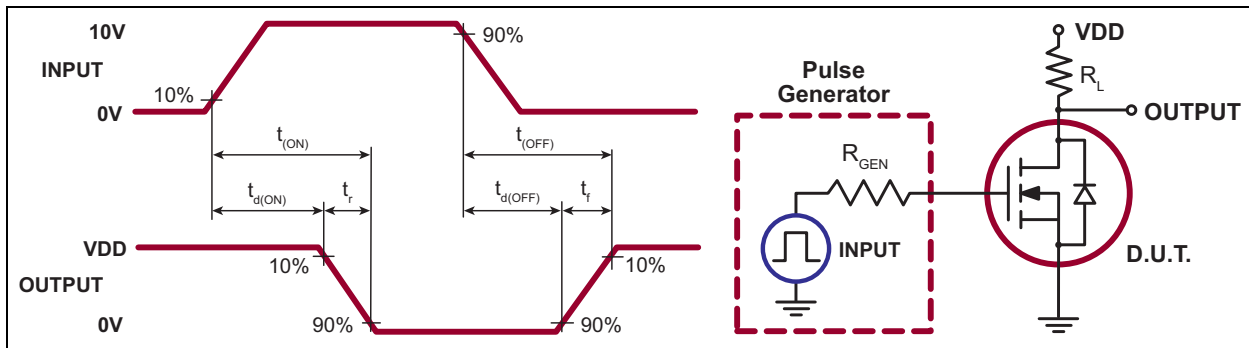
Table 3-1 shows the description of pins in 2N7000.  
Refer to [Package Type](#) for the location of the pins.

**TABLE 3-1: PIN FUNCTION TABLE**

Pin Number	Pin Name	Description
1	Source	Source
2	Gate	Gate
3	Drain	Drain

## 4.0 FUNCTIONAL DESCRIPTION

Figure 4-1 illustrates the switching waveforms and test circuit for 2N7000.



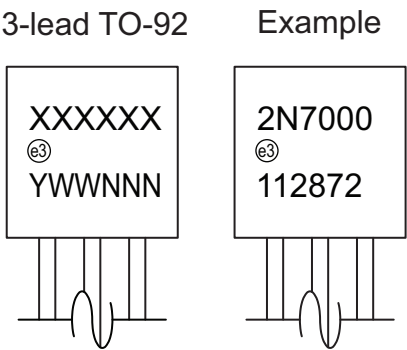
**FIGURE 4-1:** Switching Waveforms and Test Circuit.

**TABLE 4-1: PRODUCT SUMMARY**

$BV_{DSS}/BV_{DGS}$ (V)	$R_{DS(ON)}$ (Maximum) ( $\Omega$ )	$V_{GS(th)}$ (Maximum) (mA)
60	5	75

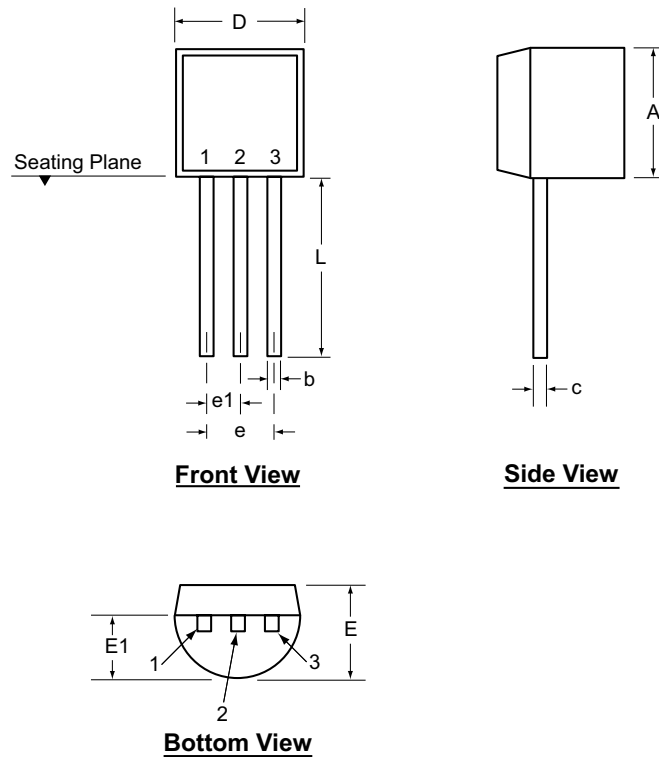
## 5.0 PACKAGING INFORMATION

### 5.1 Package Marking Information



<b>Legend:</b>	XX...X	Product Code or Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week '01')
	NNN	Alphanumeric traceability code
	e3	Pb-free JEDEC® designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator (e3) can be found on the outer packaging for this package.
	e4	Pre-plated
<b>Note:</b> In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for product code or customer-specific information. Package may or not include the corporate logo.		

## 3-Lead TO-92 Package Outline (L/LL/N3)



Note: For the most current package drawings, see the Microchip Packaging Specification at [www.microchip.com/packaging](http://www.microchip.com/packaging).

Symbol		A	b	c	D	E	E1	e	e1	L
Dimensions (inches)	MIN	.170	.014 <sup>†</sup>	.014 <sup>†</sup>	.175	.125	.080	.095	.045	.500
	NOM	-	-	-	-	-	-	-	-	-
	MAX	.210	.022 <sup>†</sup>	.022 <sup>†</sup>	.205	.165	.105	.105	.055	.610*

JEDEC Registration TO-92.

\* This dimension is not specified in the JEDEC drawing.

† This dimension differs from the JEDEC drawing.

Drawings not to scale.

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NOTES:

## APPENDIX A: REVISION HISTORY

### Revision A (February 2021)

- Converted Supertex Doc# DSFP-2N7000 to Microchip D20005695A
- Removed the TO-92 N3 P002, P003, P005, P013, and P014 media types to align package specifications with the actual BQM
- Made minor text changes throughout the document

# 2N7000

## PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, contact your local Microchip representative or sales office.

<u>PART NO.</u>	<u>XX</u>	-	<u>X</u>	-	<u>X</u>
Device	Package Options		Environmental		Media Type
Device:	2N7000	=	N-Channel Enhancement-Mode Vertical DMOS FET		
Package:	(blank)	=	3-lead TO-92		
Environmental:	G	=	Lead (Pb)-free/RoHS-compliant Package		
Media Type:	(blank)	=	1000/Bag for a 3-lead TO-92 Package		

**Examples:**  
  
a) 2N7000-G: N-Channel Enhancement-Mode, Vertical DMOS FET, 3-lead TO-92, 1000/Bag

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