1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings(†)

V_{CC} 7.0V

All inputs and outputs w.r.t. V_{SS} .... -0.6V to V_{CC}+1.0V

Storage temperature .... -65°C to 150°C

Ambient temperature under bias .... -65°C to 125°C

ESD protection on all pins .... 4 KV

† **NOTICE:** Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for an extended period of time may affect device reliability

TABLE 1-1: DC CHARACTERISTICS

DC CHARACTERISTICS			Industrial (I): T_A = -40°C to +85°C V_{CC} = 1.8V to 5.5V Automotive (E): T_A = -40°C to +125°C V_{CC} = 4.5V to 5.5V (25C040 only)			
Param. No.	**Sym.**	**Characteristic**	**Min.**	**Max.**	**Units**	**Test Conditions**
D001	V_{IH1}	High-level input voltage	2.0	V_{CC}+1	V	$V_{CC} \geq$ 2.7V **(Note)**
D002	V_{IH2}		0.7 V_{CC}	V_{CC}+1	V	V_{CC}< 2.7V **(Note)**
D003	V_{IL1}	Low-level input voltage	-0.3	0.8	V	$V_{CC} \geq$ 2.7V **(Note)**
D004	V_{IL2}		-0.3	0.3 V_{CC}	V	V_{CC} < 2.7V **(Note)**
D005	V_{OL}	Low-level output voltage	—	0.4	V	I_{OL} = 2.1 mA
D006	V_{OL}		—	0.2	V	I_{OL} = 1.0 mA, V_{CC} < 2.5V
D007	V_{OH}	High-level output voltage	V_{CC} -0.5	—	V	I_{OH} =-400 µA
D008	I_{LI}	Input leakage current	—	±1	µA	$\overline{CS}$ = V_{CC}, V_{IN} = V_{SS} TO V_{CC}
D009	I_{LO}	Output leakage current	—	±1	µA	$\overline{CS}$ = V_{CC}, V_{OUT} = V_{SS} TO V_{CC}
D010	C_{INT}	Internal Capacitance (all inputs and outputs)	—	7	pF	T_A = 25°C, CLK = 1.0 MHz, V_{CC} = 5.0V **(Note)**
D011	I_{CC} Read	Operating Current	— —	1 500	mA µA	V_{CC} = 5.5V; F_{CLK} = 3.0 MHz; SO = Open V_{CC} = 2.5V; F_{CLK} = 2.0 MHz; SO = Open
D012	I_{CC} Write		— —	5 3	mA mA	V_{CC} = 5.5V V_{CC} = 2.5V
D013	I_{CCS}	Standby Current	— —	5 1	µA µA	$\overline{CS}$ = V_{CC} = 5.5V, Inputs tied to V_{CC} or V_{SS} $\overline{CS}$ = V_{CC} = 2.5V, Inputs tied to V_{CC} or V_{SS}

Note: This parameter is periodically sampled and not 100% tested.

TABLE 1-2: AC CHARACTERISTICS

AC CHARACTERISTICS			Industrial (I): T_A = -40°C to +85°C V_{CC} = 1.8V to 5.5V Automotive (E): T_A = -40°C to +125°C V_{CC} = 4.5V to 5.5V (25C040 only)			
Param No.	**Sym.**	**Characteristic**	**Min.**	**Max.**	**Units**	**Test Conditions**
1	FCLK	Clock Frequency	— — —	3 2 1	MHz MHz MHz	VCC = 4.5V to 5.5V VCC = 2.5V to 4.5V VCC = 1.8V to 2.5V
2	TCSS	$\overline{CS}$ Setup Time	100 250 500	— — —	ns ns ns	VCC = 4.5V to 5.5V VCC = 2.5V to 4.5V VCC = 1.8V to 2.5V
3	TCSH	$\overline{CS}$ Hold Time	150 250 475	— — —	ns ns ns	VCC = 4.5V to 5.5V VCC = 2.5V to 4.5V VCC = 1.8V to 2.5V
4	TCSD	$\overline{CS}$ Disable Time	500	—	ns	—
5	TSU	Data Setup Time	30 50 50	— — —	ns ns ns	VCC = 4.5V to 5.5V VCC = 2.5V to 4.5V VCC = 1.8V to 2.5V
6	THD	Data Hold Time	50 100 100	— — —	ns ns ns	VCC = 4.5V to 5.5V VCC = 2.5V to 4.5V VCC = 1.8V to 2.5V
7	TR	CLK Rise Time	—	2	µs	**(Note 1)**
8	TF	CLK Fall Time	—	2	µs	**(Note 1)**
9	THI	Clock High Time	150 230 475	— — —	ns ns ns	VCC = 4.5V to 5.5V VCC = 2.5V to 4.5V VCC = 1.8V to 2.5V
10	TLO	Clock Low Time	150 230 475	— — —	ns ns ns	VCC = 4.5V to 5.5V VCC = 2.5V to 4.5V VCC = 1.8V to 2.5V
11	TCLD	Clock Delay Time	50	—	ns	—
12	TCLE	Clock Enable Time	50	—	ns	—
13	TV	Output Valid from Clock Low	— — —	150 230 475	ns ns ns	VCC = 4.5V to 5.5V VCC = 2.5V to 4.5V VCC = 1.8V to 2.5V
14	THO	Output Hold Time	0	—	ns	**(Note 1)**
15	TDIS	Output Disable Time	— — —	200 250 500	ns ns ns	VCC = 4.5V to 5.5V **(Note 1)** VCC = 2.5V to 4.5V **(Note 1)** VCC = 1.8V to 2.5V **(Note 1)**
16	THS	$\overline{HOLD}$ Setup Time	100 100 200	— — —	ns ns ns	VCC = 4.5V to 5.5V VCC = 2.5V to 4.5V VCC = 1.8V to 2.5V
17	THH	$\overline{HOLD}$ Hold Time	100 100 200	— — —	ns ns ns	VCC = 4.5V to 5.5V VCC = 2.5V to 4.5V VCC = 1.8V to 2.5V
18	THZ	$\overline{HOLD}$ Low to Output High-Z	100 150 200	— — —	ns ns ns	VCC = 4.5V to 5.5V **(Note 1)** VCC = 2.5V to 4.5V **(Note 1)** VCC = 1.8V to 2.5V **(Note 1)**
19	THV	$\overline{HOLD}$ High to Output Valid	100 150 200	— — —	ns ns ns	VCC = 4.5V to 5.5V VCC = 2.5V to 4.5V VCC = 1.8V to 2.5V
20	TWC	Internal Write Cycle Time	—	5	ms	—
21	—	Endurance	1M	—	E/W Cycles	**(Note 2)**

Note 1: This parameter is periodically sampled and not 100% tested.

2: This parameter is not tested but ensured by characterization. For endurance estimates in a specific application, please consult the Total Endurance™ Model which can be obtained from our web site: www.microchip.com.

FIGURE 1-1: HOLD TIMING

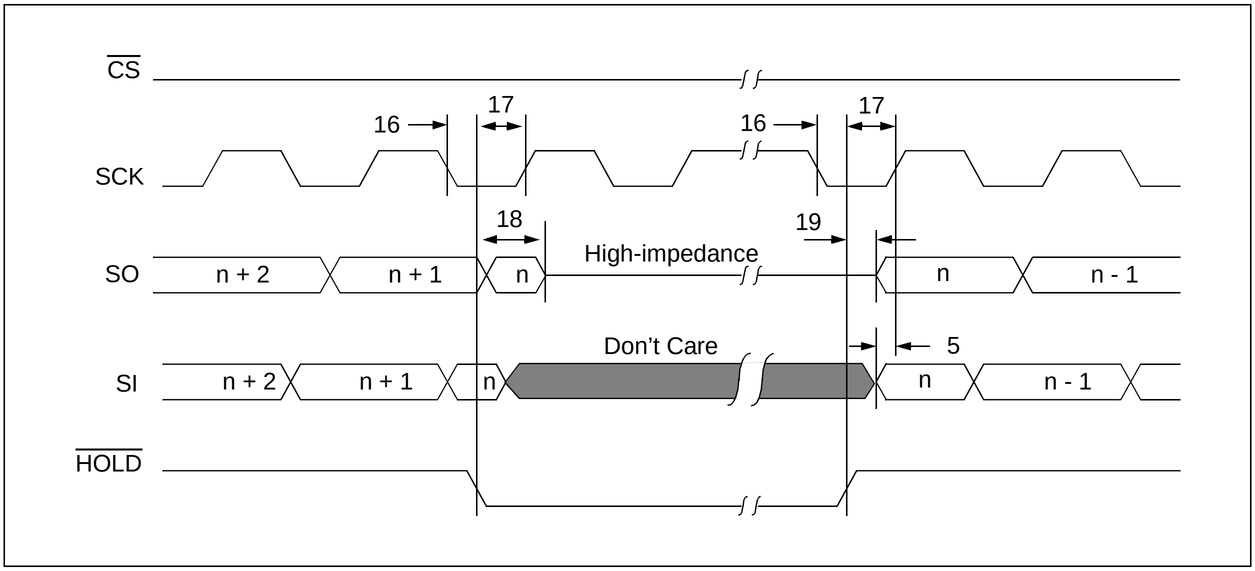


FIGURE 1-2: SERIAL INPUT TIMING

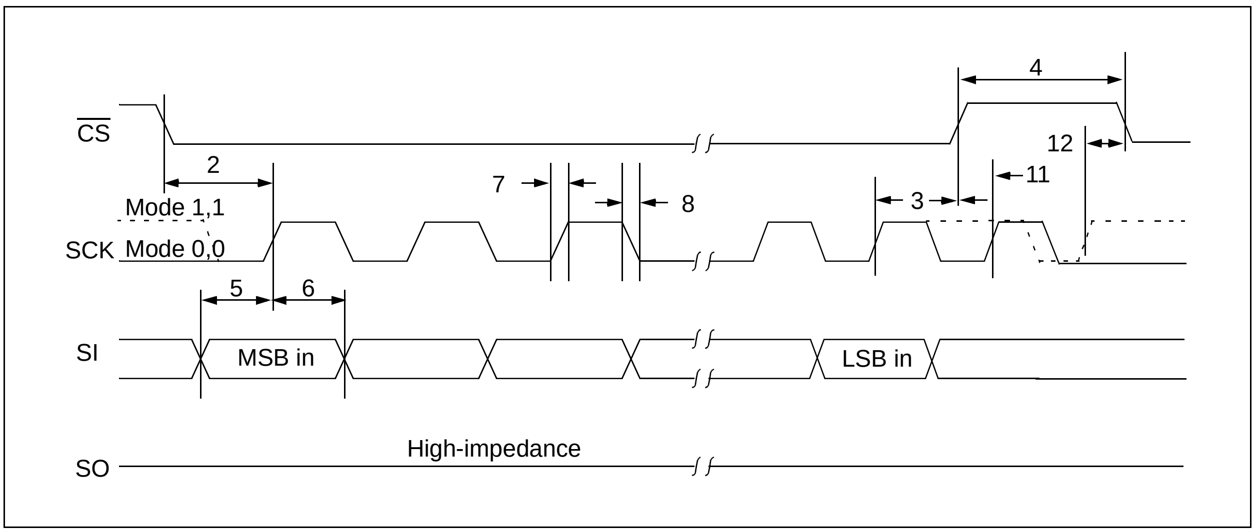


FIGURE 1-3: SERIAL OUTPUT TIMING

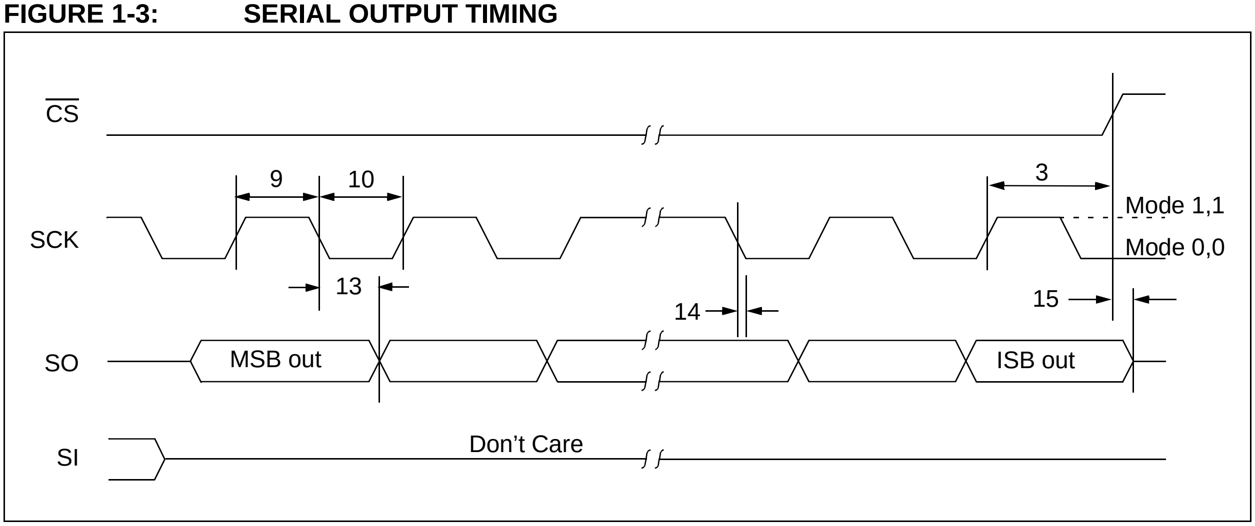


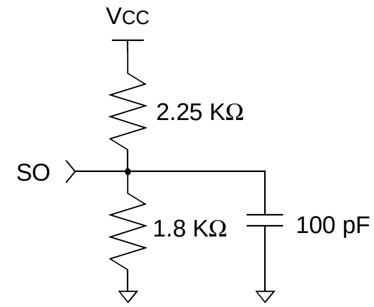
TABLE 1-3: AC TEST CONDITIONS

AC Waveform:	
VLO = 0.2V	—
VHI = VCC - 0.2V	**(Note 1)**
VHI = 4.0V	**(Note 2)**
Timing Measurement Reference Level	
Input	0.5 VCC
Output	0.5 VCC

Note 1: For VCC ≤ 4.0V

2: For VCC > 4.0V

FIGURE 1-4: AC TEST CIRCUIT AC



2.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 2-1.

TABLE 2-1: PIN FUNCTION TABLE

Name	PDIP	SOIC	TSSOP	Description
$\overline{\text{CS}}$	1	1	3	Chip Select Input
SO	2	2	4	Serial Data Output
$\overline{\text{WP}}$	3	3	5	Write-Protect Pin
Vss	4	4	6	Ground
SI	5	5	7	Serial Data Input
SCK	6	6	8	Serial Clock Input
$\overline{\text{HOLD}}$	7	7	1	Hold Input
Vcc	8	8	2	Supply Voltage

2.1 Chip Select ($\overline{\text{CS}}$)

A low level on this pin selects the device. A high level deselects the device and forces it into Standby mode. However, a programming cycle which is already initiated or in progress will be completed, regardless of the $\overline{\text{CS}}$ input signal. If $\overline{\text{CS}}$ is brought high during a program cycle, the device will go in Standby mode as soon as the programming cycle is complete. When the device is deselected, SO goes into the high-impedance state, allowing multiple parts to share the same SPI bus. A low-to-high transition on $\overline{\text{CS}}$ after a valid write sequence initiates an internal write cycle. After power-up, a low level on $\overline{\text{CS}}$ is required prior to any sequence being initiated.

2.2 Serial Output (SO)

The SO pin is used to transfer data out of the 25XX040. During a read cycle, data is shifted out on this pin after the falling edge of the serial clock.

2.3 Write-Protect ($\overline{\text{WP}}$)

This pin is a hardware write-protect input pin. When $\overline{\text{WP}}$ is low, all writes to the array or STATUS register are disabled, but any other operation functions normally. When $\overline{\text{WP}}$ is high, all functions, including nonvolatile writes operate normally. $\overline{\text{WP}}$ going low at any time will reset the write enable latch and inhibit programming, except when an internal write has already begun. If an internal write cycle has already begun, $\overline{\text{WP}}$ going low will have no effect on the write. See Table 3-3 for Write-Protect Functionality Matrix.

2.4 Serial Input (SI)

The SI pin is used to transfer data into the device. It receives instructions, addresses and data. Data is latched on the rising edge of the serial clock.

2.5 Serial Clock (SCK)

The SCK is used to synchronize the communication between a master and the 25XX040. Instructions, addresses or data present on the SI pin are latched on the rising edge of the clock input, while data on the SO pin is updated after the falling edge of the clock input.

2.6 Hold ($\overline{\text{HOLD}}$)

The $\overline{\text{HOLD}}$ pin is used to suspend transmission to the 25XX040 while in the middle of a serial sequence without having to retransmit the entire sequence again at a later time. It must be held high any time this function is not being used. Once the device is selected and a serial sequence is underway, the $\overline{\text{HOLD}}$ pin may be pulled low to pause further serial communication without resetting the serial sequence. The $\overline{\text{HOLD}}$ pin must be brought low while SCK is low, otherwise the HOLD function will not be invoked until the next SCK high-to-low transition. The 25XX040 must remain selected during this sequence. The SI, SCK and SO pins are in a high-impedance state during the time the part is paused and transitions on these pins will be ignored. To resume serial communication, $\overline{\text{HOLD}}$ must be brought high while the SCK pin is low, otherwise serial communication will not resume. Lowering the HOLD line at any time will tri-state the SO line.

3.0 FUNCTIONAL DESCRIPTION

3.1 Principles of Operation

The 25XX040 is a 512 byte Serial EEPROM designed to interface directly with the Serial Peripheral Interface (SPI) port of many of today's popular microcontroller families, including Microchip's PIC16C6X/7X microcontrollers. It may also interface with microcontrollers that do not have a built-in SPI port by using discrete I/O lines programmed properly with the software.

The 25XX040 contains an 8-bit instruction register. The part is accessed via the SI pin, with data being clocked in on the rising edge of SCK. The $\overline{\text{CS}}$ pin must be low and the $\overline{\text{HOLD}}$ pin must be high for the entire operation. The $\overline{\text{WP}}$ pin must be held high to allow writing to the memory array.

Table 3-1 contains a list of the possible instruction bytes and format for device operation. The Most Significant address bit (A8) is located in the instruction byte. All instructions, addresses, and data are transferred MSB first, LSB last.

Data is sampled on the first rising edge of SCK after $\overline{\text{CS}}$ goes low. If the clock line is shared with other peripheral devices on the SPI bus, the user can assert the $\overline{\text{HOLD}}$ input and place the 25XX040 in 'HOLD' mode. After releasing the $\overline{\text{HOLD}}$ pin, operation will resume from the point when the $\overline{\text{HOLD}}$ was asserted.

3.2 Read Sequence

The part is selected by pulling $\overline{\text{CS}}$ low. The 8-bit `READ` instruction with the A8 address bit is transmitted to the 25XX040 followed by the lower 8-bit address (A7 through A0). After the correct `READ` instruction and address are sent, the data stored in the memory at the selected address is shifted out on the SO pin. The data stored in the memory at the next address can be read sequentially by continuing to provide clock pulses. The internal Address Pointer is automatically incremented to the next higher address after each byte of data is shifted out. When the highest address is reached (01FFh), the address counter rolls over to address 0000h allowing the read cycle to be continued indefinitely. The read operation is terminated by raising the $\overline{\text{CS}}$ pin (Figure 3-1).

3.3 Write Sequence

Prior to any attempt to write data to the 25XX040, the write enable latch must be set by issuing the `WREN` instruction (Figure 3-4). This is done by setting $\overline{\text{CS}}$ low and then clocking out the proper instruction into the 25XX040. After all eight bits of the instruction are transmitted, the $\overline{\text{CS}}$ must be brought high to set the write enable latch. If the write operation is initiated immediately after the `WREN` instruction without $\overline{\text{CS}}$ being brought high, the data will not be written to the array because the write enable latch will not have been properly set.

Once the write enable latch is set, the user may proceed by setting the $\overline{\text{CS}}$ low, issuing a `WRITE` instruction, followed by the address, and then the data to be written. Keep in mind that the Most Significant address bit (A8) is included in the instruction byte. Up to 16 bytes of data can be sent to the 25XX040 before a write cycle is necessary. The only restriction is that all of the bytes must reside in the same page. A page address begins with `XXXX 0000` and ends with `XXXX 1111`. If the internal address counter reaches `XXXX 1111` and the clock continues, the counter will roll back to the first address of the page and overwrite any data in the page that may have been written.

For the data to be actually written to the array, the $\overline{\text{CS}}$ must be brought high after the least significant bit (D0) of the n^{th} data byte has been clocked in. If $\overline{\text{CS}}$ is brought high at any other time, the write operation will not be completed. Refer to Figure 3-2 and Figure 3-3 for more detailed illustrations on the byte write sequence and the page write sequence respectively. While the write is in progress, the STATUS register may be read to check the status of the WIP, WEL, BP1 and BP0 bits (Figure 3-6). A read attempt of a memory array location will not be possible during a write cycle. When the write cycle is completed, the write enable latch is reset.

TABLE 3-1: INSTRUCTION SET

Instruction Name	Instruction Format	Description
READ	0000 A8011	Read data from memory array beginning at selected address
WRITE	0000 A8010	Write data to memory array beginning at selected address
WRDI	0000 0100	Reset the write enable latch (disable write operations)
WREN	0000 0110	Set the write enable latch (enable write operations)
RDSR	0000 0101	Read STATUS register
WRSR	0000 0001	Write STATUS register

Note: A8 is the 9^{th} address bit necessary to fully address 512 bytes.

FIGURE 3-1: READ SEQUENCE

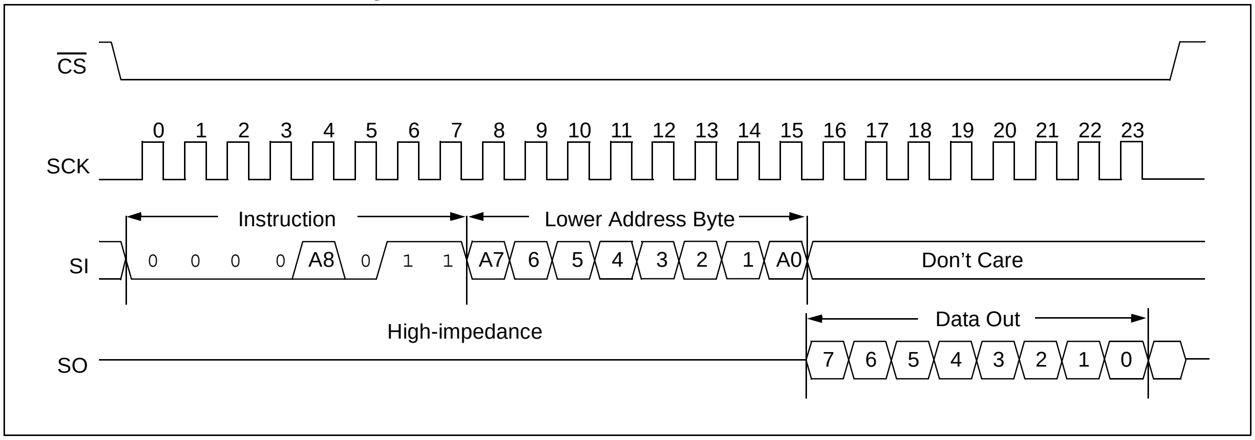


FIGURE 3-2: BYTE WRITE SEQUENCE

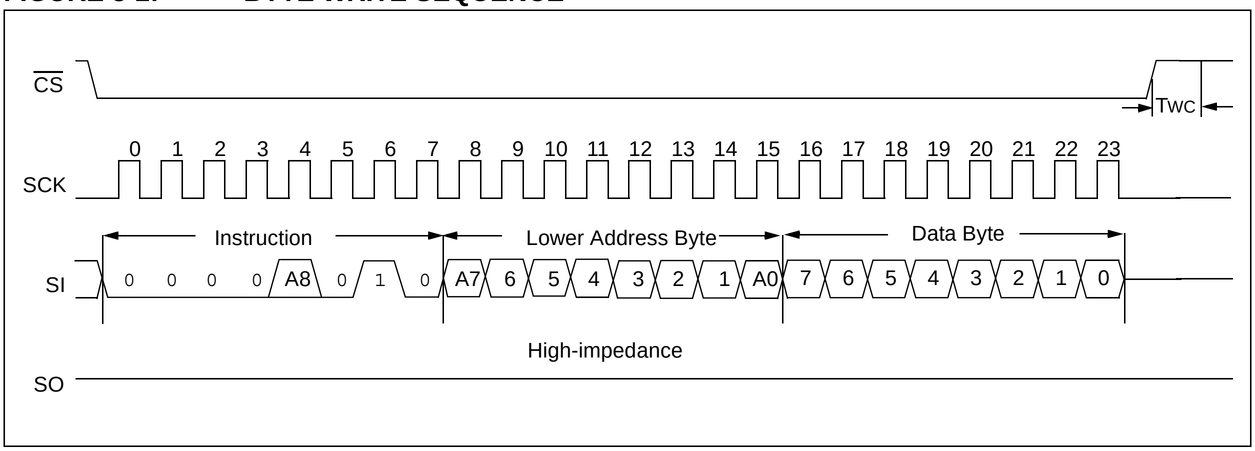
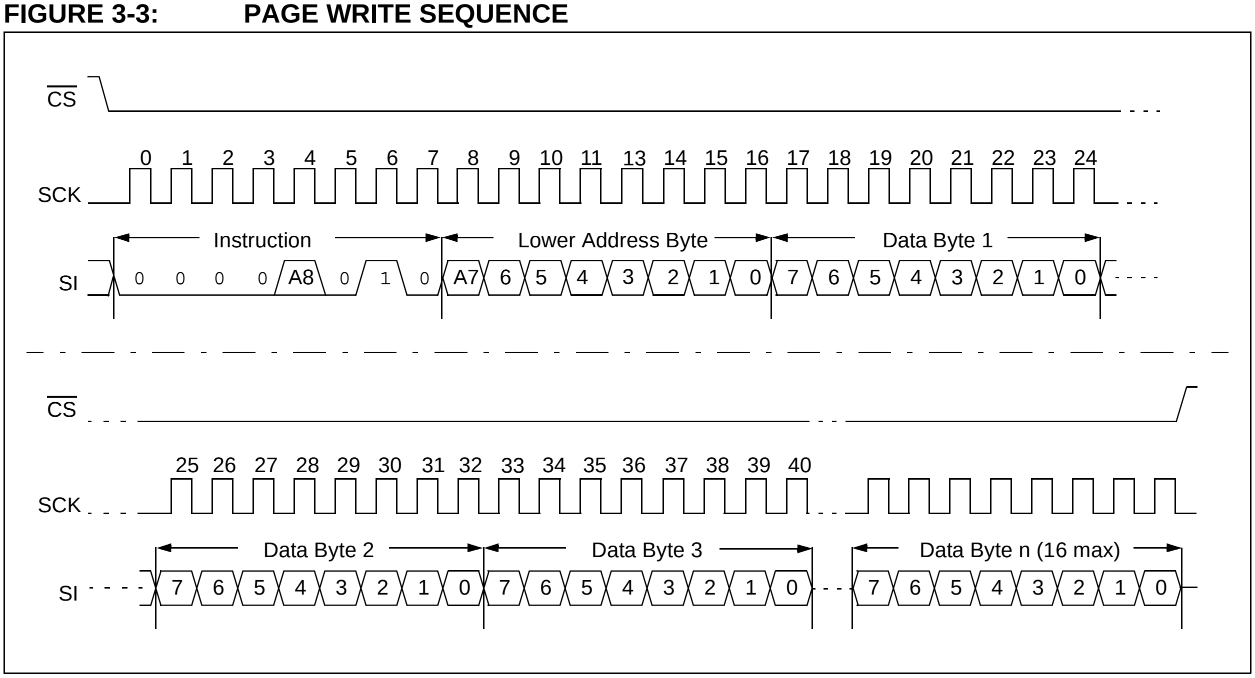


FIGURE 3-3: PAGE WRITE SEQUENCE



3.4 Write Enable (WREN) and Write Disable (WRDI)

The 25XX040 contains a write enable latch. See Table 3-3 for the Write-Protect Functionality Matrix. This latch must be set before any write operation will be completed internally. The `WREN` instruction will set the latch, and the `WRDI` will reset the latch.

The following is a list of conditions under which the write enable latch will be reset:

- Power-up
- `WRDI` instruction successfully executed
- `WRSR` instruction successfully executed
- `WRITE` instruction successfully executed
- $\overline{\text{WP}}$ line is low

FIGURE 3-4: WRITE ENABLE SEQUENCE

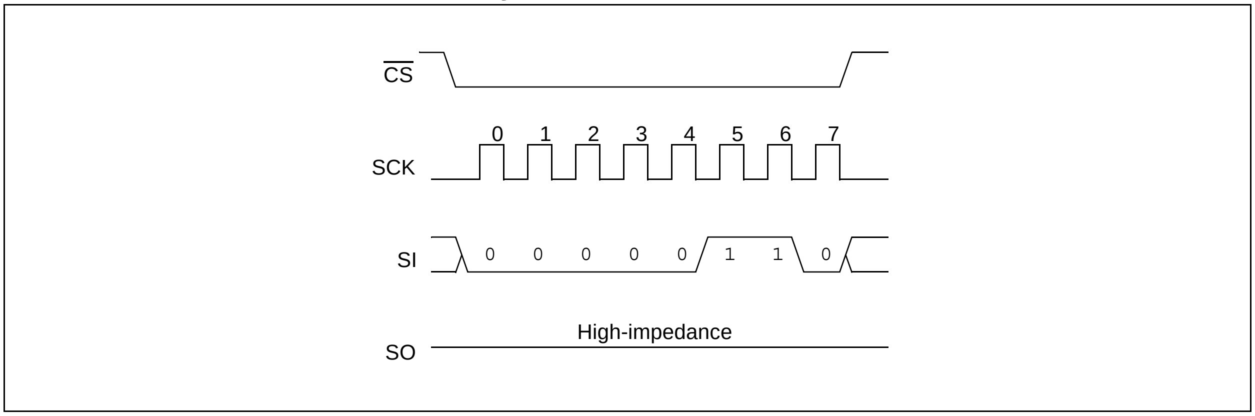
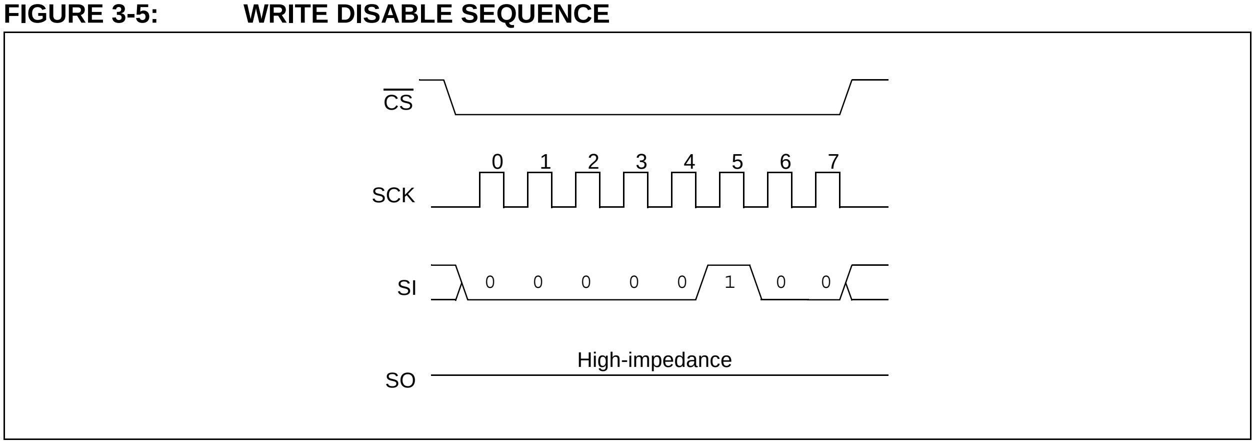


FIGURE 3-5: WRITE DISABLE SEQUENCE



3.5 Read Status Register (RDSR)

The `RDSR` instruction provides access to the STATUS register. The STATUS register may be read at any time, even during a write cycle. The STATUS register is formatted as follows:

7	6	5	4	3	2	1	0
X	X	X	X	BP1	BP0	WEL	WIP

The **Write-In-Process (WIP)** bit indicates whether the 25XX040 is busy with a write operation. When set to a '1', a write is in progress, when set to a '0', no write is in progress. This bit is read-only.

The **Write Enable Latch (WEL)** bit indicates the status of the write enable latch. When set to a '1', the latch allows writes to the array, when set to a '0', the latch prohibits writes to the array. The state of this bit can always be updated via the WREN or WRDI commands regardless of the state of write protection on the STATUS register. This bit is read-only.

The **Block Protection (BP0 and BP1)** bits indicate which blocks are currently write-protected. These bits are set by the user issuing the `WRSR` instruction. These bits are nonvolatile.

See Figure 3-6 for `RDSR` timing sequence.

3.6 Write Status Register (WRSR)

The `WRSR` instruction allows the user to select one of four levels of protection for the array by writing to the appropriate bits in the STATUS register. The array is divided up into four segments. The user has the ability to write-protect none, one, two, or all four of the segments of the array. The partitioning is controlled as illustrated in Table 3-2.

See Figure 3-7 for `WRSR` timing sequence.

TABLE 3-2: ARRAY PROTECTION

BP1	BP0	Array Addresses Write-Protected
0	0	none
0	1	upper 1/4 (0180h-01FFh)
1	0	upper 1/2 (0100h-01FFh)
1	1	all (0000h-01FFh)

FIGURE 3-6: READ STATUS REGISTER SEQUENCE

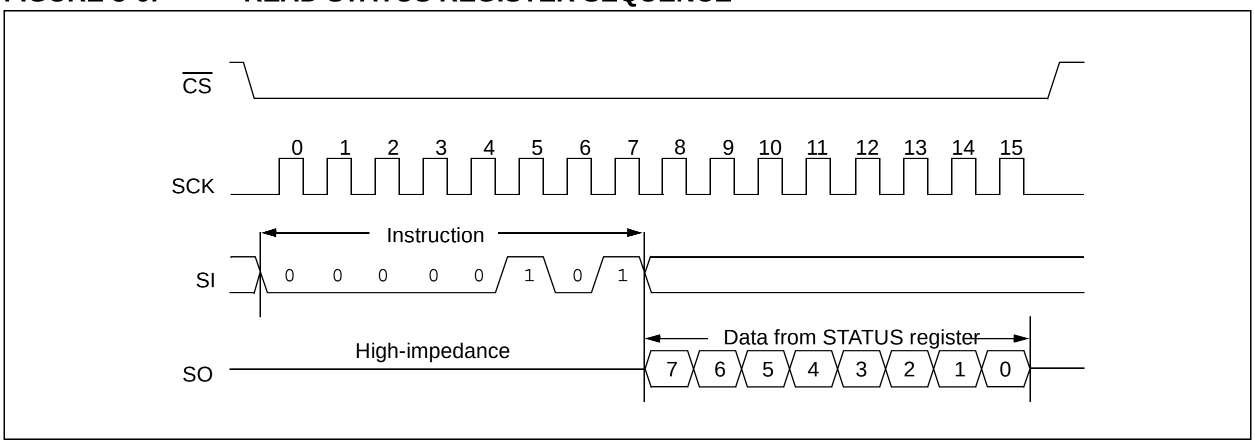
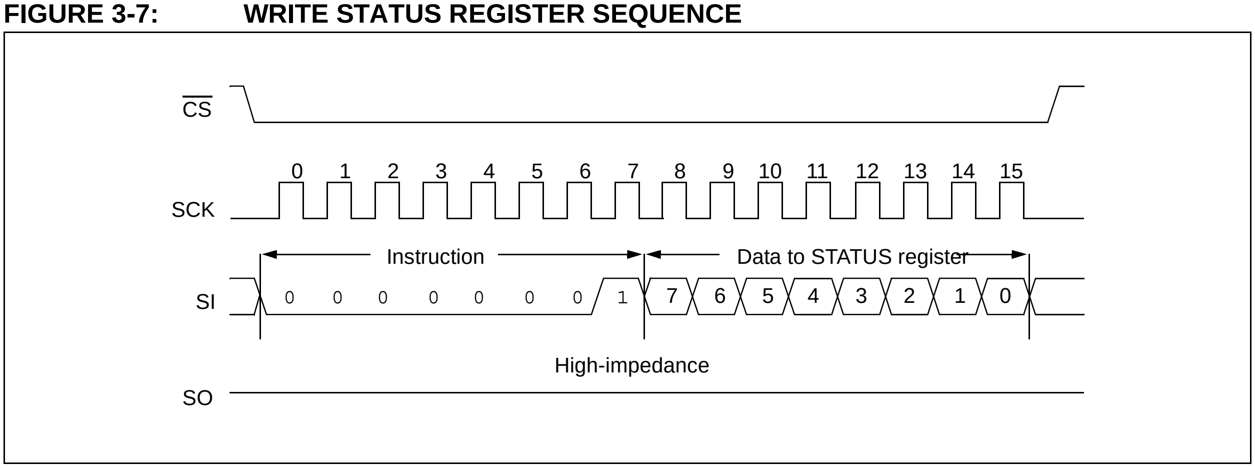


FIGURE 3-7: WRITE STATUS REGISTER SEQUENCE



3.7 Data Protection

The following protection has been implemented to prevent inadvertent writes to the array:

- The write enable latch is reset on power-up
- A write enable instruction must be issued to set the write enable latch
- After a byte write, page write or STATUS register write, the write enable latch is reset
- $\overline{\text{CS}}$ must be set high after the proper number of clock cycles to start an internal write cycle
- Access to the array during an internal write cycle is ignored and programming is continued
- The write enable latch is reset when the $\overline{\text{WP}}$ pin is low

3.8 Power-On State

The 25XX040 powers on in the following state:

- The device is in low-power Standby mode ($\overline{\text{CS}}$ = 1)
- The write enable latch is reset
- SO is in high-impedance state
- A low level on $\overline{\text{CS}}$ is required to enter active state

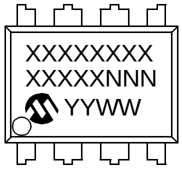
TABLE 3-3: WRITE-PROTECT FUNCTIONALITY MATRIX

WP	WEL	Protected Blocks	Unprotected Blocks	STATUS Register
Low	X	Protected	Protected	Protected
High	0	Protected	Protected	Protected
High	1	Protected	Writable	Writable

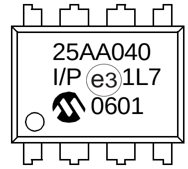
4.0 PACKAGING INFORMATION

4.1 Package Marking Information

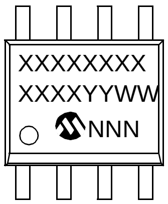
8-Lead PDIP (300 mil)



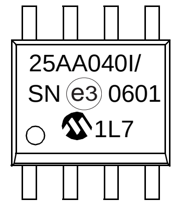
Example:



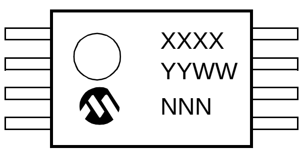
8-Lead SOIC (150 mil)



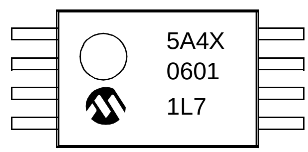
Example:



8-Lead TSSOP



Example:

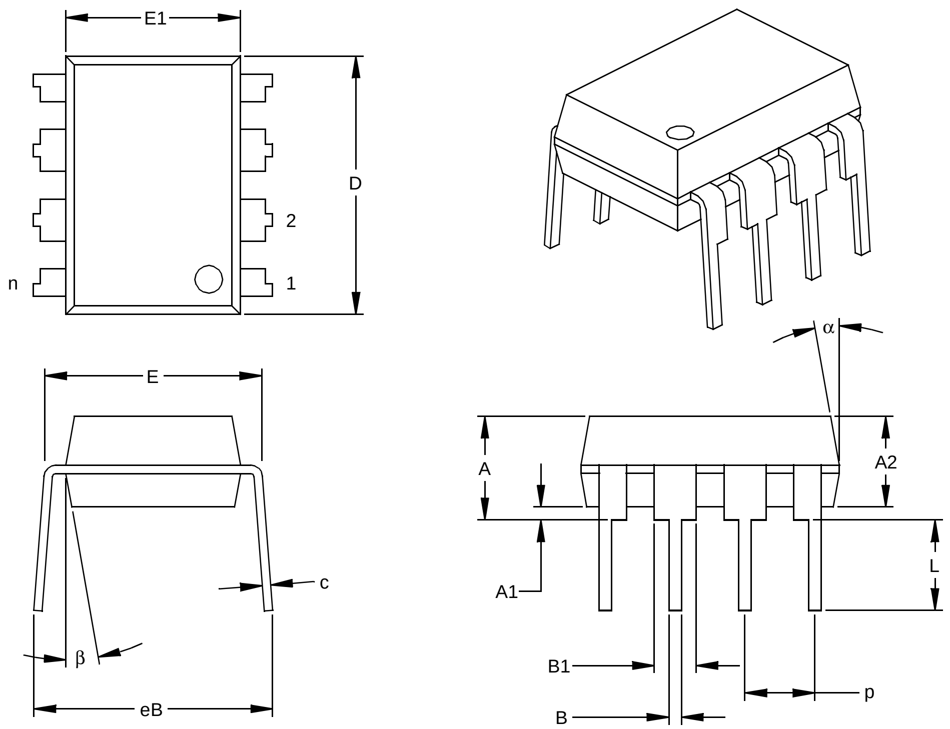


Legend:	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	e3	Pb-free JEDEC designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator (e3) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

8-Lead Plastic Dual In-line (P) – 300 mil (PDIP)

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

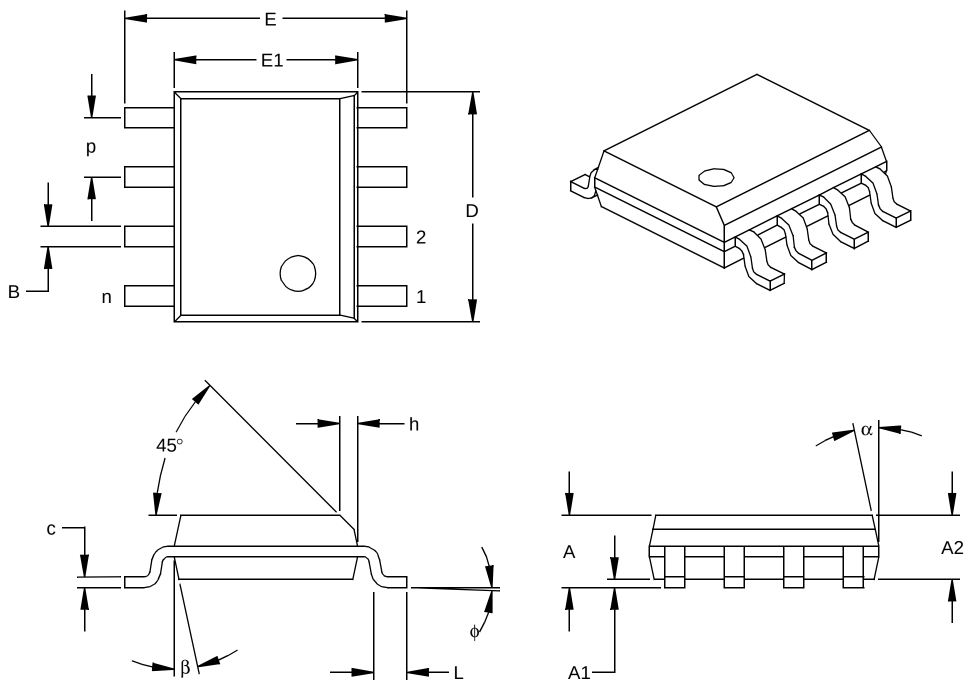


Units		INCHES*			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		8			8	
Pitch	p		.100			2.54	
Top to Seating Plane	A	.140	.155	.170	3.56	3.94	4.32
Molded Package Thickness	A2	.115	.130	.145	2.92	3.30	3.68
Base to Seating Plane	A1	.015			0.38		
Shoulder to Shoulder Width	E	.300	.313	.325	7.62	7.94	8.26
Molded Package Width	E1	.240	.250	.260	6.10	6.35	6.60
Overall Length	D	.360	.373	.385	9.14	9.46	9.78
Tip to Seating Plane	L	.125	.130	.135	3.18	3.30	3.43
Lead Thickness	c	.008	.012	.015	0.20	0.29	0.38
Upper Lead Width	B1	.045	.058	.070	1.14	1.46	1.78
Lower Lead Width	B	.014	.018	.022	0.36	0.46	0.56
Overall Row Spacing §	eB	.310	.370	.430	7.87	9.40	10.92
Mold Draft Angle Top	α	5	10	15	5	10	15
Mold Draft Angle Bottom	β	5	10	15	5	10	15

***** Controlling Parameter
§ Significant Characteristic
Notes:
Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010” (0.254mm) per side.
JEDEC Equivalent: MS-001
Drawing No. C04-018

8-Lead Plastic Small Outline (SN) – Narrow, 150 mil (SOIC)

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

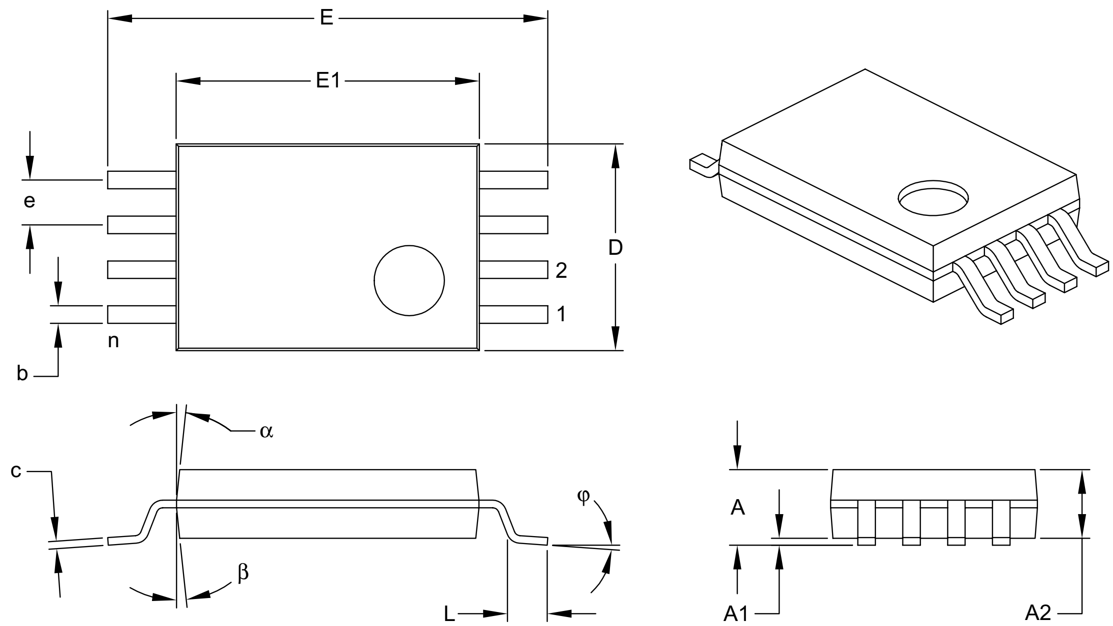


	Units	INCHES*			MILLIMETERS		
	Dimension Limits	MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		8			8	
Pitch	p		.050			1.27	
Overall Height	A	.053	.061	.069	1.35	1.55	1.75
Molded Package Thickness	A2	.052	.056	.061	1.32	1.42	1.55
Standoff §	A1	.004	.007	.010	0.10	0.18	0.25
Overall Width	E	.228	.237	.244	5.79	6.02	6.20
Molded Package Width	E1	.146	.154	.157	3.71	3.91	3.99
Overall Length	D	.189	.193	.197	4.80	4.90	5.00
Chamfer Distance	h	.010	.015	.020	0.25	0.38	0.51
Foot Length	L	.019	.025	.030	0.48	0.62	0.76
Foot Angle	φ	0	4	8	0	4	8
Lead Thickness	c	.008	.009	.010	0.20	0.23	0.25
Lead Width	B	.013	.017	.020	0.33	0.42	0.51
Mold Draft Angle Top	α	0	12	15	0	12	15
Mold Draft Angle Bottom	β	0	12	15	0	12	15

***** Controlling Parameter
§ Significant Characteristic
Notes:
Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" (0.254mm) per side.
JEDEC Equivalent: MS-012
Drawing No. C04-057

8-Lead Plastic Thin Shrink Small Outline (ST) – 4.4 mm (TSSOP)

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		INCHES			MILLIMETERS*		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		8			8	
Pitch	e		.026 BSC			0.65 BSC	
Overall Height	A	–	–	.047	–	–	1.20
Molded Package Thickness	A2	.031	.039	.041	0.80	1.00	1.05
Standoff	A1	.002	–	.006	0.05	–	0.15
Overall Width	E		.252 BSC			6.40 BSC	
Molded Package Width	E1	.169	.173	.177	4.30	4.40	4.50
Molded Package Length	D	.114	.118	.122	2.90	3.00	3.10
Foot Length	L	.018	.024	.030	0.45	0.60	0.75
Foot Angle	φ	0°	–	8°	0°	–	8°
Lead Thickness	c	.004	–	.008	0.09	–	0.20
Lead Width	b	.007	–	.012	0.19	–	0.30
Mold Draft Angle Top	α		12° REF			12° REF	
Mold Draft Angle Bottom	β		12° REF			12° REF	

*Controlling Parameter

Notes:

1. Dimension D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .005" (0.127mm) per side.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.
See ASME Y14.5M

REF: Reference Dimension, usually without tolerance, for information purposes only.
See ASME Y14.5M

Drawing No. C04-086 Revised 7-25-06

APPENDIX A: REVISION HISTORY

Revision D

Corrections to Section 1.0, Electrical Characteristics.

Revision E (8/2006)

Added note to page 1 header (Not recommended for new designs). Added note to package drawings.

Updated document format

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Device: 25AA040/25LC040/25C040 Literature Number: DS21204E

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PART NO.	X	/XX	XXX
Device	Temperature Range	Package	Pattern

Device:

25AA040:	4096-bit 1.8V SPI Serial EEPROM
25AA040T:	4096-bit 1.8V SPI Serial EEPROM (Tape and Reel)
25XX040X:	4096-bit 1.8V SPI Serial EEPROM in alternate pinout (ST only)
25AA040XT:	4096-bit 1.8V SPI Serial EEPROM in alternate pinout Tape and Reel (ST only)
25LC040:	4096-bit 2.5V SPI Serial EEPROM
25LC040T:	4096-bit 2.5V SPI Serial EEPROM (Tape and Reel)
25LC040X:	4096-bit 2.5V SPI Serial EEPROM in alternate pinout (ST only)
25LC040XT:	4096-bit 2.5V SPI Serial EEPROM in alternate pinout Tape and Reel (ST only)
25C040:	4096-bit 5.0V SPI Serial EEPROM
25C040T:	4096-bit 5.0V SPI Serial EEPROM (Tape and Reel)
25C040X:	4096-bit 5.0V SPI Serial EEPROM in alternate pinout (ST only)
25C040XT:	4096-bit 5.0V SPI Serial EEPROM in alternate pinout Tape and Reel (ST only)

Temperature Range:

I	=	-40 °C to+85 °C
E	=	-40 °C to +125 °C

Package:

P	=	Plastic DIP (300 mil body), 8-lead
SN	=	Plastic SOIC (150 mil body), 8-lead
ST	=	Plastic TSSOP (4.4 mm body), 8-lead

Examples:

a) 25AA040-I/P: Industrial Temp., PDIP package
b) 25AA040-I/SN: Industrial Temp., SOIC package
c) 25AA040T-I/SN: Tape and Reel, Industrial Temp., SOIC package
d) 25AA040X-I/ST: Alternate Pinout, Industrial Temp., TSSOP package
e) 25AA040XT-I/ST: Alternate Pinout, Tape and Reel, Industrial Temp., TSSOP package

f) 25LC040-I/P: Industrial Temp., PDIP package
g) 25LC040-I/SN: Industrial Temp., SOIC package
h) 25LC040T-I/SN: Tape and Reel, Industrial Temp., SOIC package
i) 25LC040X-I/ST: Alternate Pinout, Industrial Temp., TSSOP package
j) 25LC040XT-I/ST: Alternate Pinout, Tape and Reel, Industrial Temp., TSSOP package

k) 25C040-I/P: Industrial Temp., PDIP package
l) 25C040-I/SN: Industrial Temp., SOIC package
m) 25C040T-I/SN: Tape and Reel, Industrial Temp., SOIC package
n) 25C040X-I/ST: Alternate Pinout, Industrial Temp., TSSOP package
o) 25C040XT-I/ST: Alternate Pinout, Tape and Reel, Industrial Temp., TSSOP package
p) 25C040-E/P: Extended Temp., PDIP package
q) 25C040-E/SN: Extended Temp., SOIC package
r) 25C040T-E/SN: Tape and Reel, Extended Temp., SOIC package
s) 25C040X-E/ST: Alternate Pinout, Extended Temp., TSSOP package
t) 25C040XT-E/ST: Alternate Pinout, Tape and Reel, Extended Temp., TSSOP package

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