1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings(†)

V_{CC} 6.5V

All inputs and outputs w.r.t. V_{SS} .... -0.6V to V_{CC} +1.0V

Storage temperature .... -65°C to 150°C

Ambient temperature under bias .... -40°C to 85°C

ESD protection on all pins .... 4 kV

† **NOTICE:** Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for an extended period of time may affect device reliability.

TABLE 1-1: DC CHARACTERISTICS

DC CHARACTERISTICS			Industrial (I): T_A = -40°C to +85°C V_{CC} = 1.8V to 5.5V			
Param. No.	**Symbol**	**Characteristic**	**Min.**	**Max.**	**Units**	**Test Conditions**
D1	V_{IH1}	High-Level Input Voltage	0.7 V_{CC}	V_{CC} +1	V	
D2	V_{IL1}	Low-Level Input Voltage	-0.3	0.3 V_{CC}	V	$V_{CC} \geq$ 2.7V (**Note 1**)
D3	V_{IL2}	Low-Level Input Voltage	-0.3	0.2 V_{CC}	V	V_{CC} < 2.7V (**Note 1**)
D4	V_{OL}	Low-Level Output Voltage	—	0.4	V	I_{OL} = 2.1 mA
D5	V_{OL}	Low-Level Output Voltage	—	0.2	V	I_{OL} = 1.0 mA, V_{CC} < 2.5V
D6	V_{OH}	High-Level Output Voltage	V_{CC} -0.5	—	V	I_{OH} = -400 µA
D7	I_{LI}	Input Leakage Current	—	±1	µA	$\overline{CS}$ = V_{CC}, V_{IN} = V_{SS} or V_{CC}
D8	I_{LO}	Output Leakage Current	—	±1	µA	$\overline{CS}$ = V_{CC}, V_{OUT} = V_{SS} or V_{CC}
D9	C_{INT}	Internal Capacitance (all inputs and outputs)	—	7	pF	T_A = 25°C, CLK = 1.0 MHz, V_{CC} = 5.0V (**Note 1**)
D10	I_{CCREAD}	Operating Current	—	5	mA	V_{CC} = 5.5V; F_{CLK} = 10.0 MHz, SO = Open
			—	2.5	mA	V_{CC} = 2.5V; F_{CLK} = 5.0 MHz, SO = Open
D11	$I_{CCWRITE}$	Operating Current	—	5	mA	V_{CC} = 5.5V
			—	3	mA	V_{CC} = 2.5V
D12	I_{CCS}	Standby Current	—	1	µA	$\overline{CS}$ = V_{CC} = 2.5V, Inputs tied to V_{CC} or V_{SS}, T_A = +85°C

Note 1: This parameter is periodically sampled and not 100% tested.

TABLE 1-2: AC CHARACTERISTICS

AC CHARACTERISTICS			Industrial (I): TA = -40°C to +85°C VCC = 1.8V to 5.5V			
Param. No.	**Symbol**	**Characteristic**	**Min.**	**Max.**	**Units**	**Test Conditions**
1	FCLK	Clock Frequency	—	10	MHz	4.5V ≤ VCC < 5.5V
			—	5	MHz	2.5V ≤ VCC < 4.5V
			—	3	MHz	1.8V ≤ VCC < 2.5V
2	TCSS	$\overline{CS}$ Setup Time	50	—	ns	4.5V ≤ VCC < 5.5V
			100	—	ns	2.5V ≤ VCC < 4.5V
			150	—	ns	1.8V ≤ VCC < 2.5V
3	TCSH	$\overline{CS}$ Hold Time	100	—	ns	4.5V ≤ VCC < 5.5V
			200	—	ns	2.5V ≤ VCC < 4.5V
			250	—	ns	1.8V ≤ VCC < 2.5V
4	TCSD	$\overline{CS}$ Disable Time	50	—	ns	
5	TSU	Data Setup Time	10	—	ns	4.5V ≤ VCC < 5.5V
			20	—	ns	2.5V ≤ VCC < 4.5V
			30	—	ns	1.8V ≤ VCC < 2.5V
6	THD	Data Hold Time	20	—	ns	4.5V ≤ VCC < 5.5V
			40	—	ns	2.5V ≤ VCC < 4.5V
			50	—	ns	1.8V ≤ VCC < 2.5V
7	TR	CLK Rise Time	—	100	ns	Note 1
8	TF	CLK Fall Time	—	100	ns	Note 1
9	THI	Clock High Time	50	—	ns	4.5V ≤ VCC < 5.5V
			100	—	ns	2.5V ≤ VCC < 4.5V
			150	—	ns	1.8V ≤ VCC < 2.5V
10	TLO	Clock Low Time	50	—	ns	4.5V ≤ VCC < 5.5V
			100	—	ns	2.5V ≤ VCC < 4.5V
			150	—	ns	1.8V ≤ VCC < 2.5V
11	TCLD	Clock Delay Time	50	—	ns	
12	TCLE	Clock Enable Time	50	—	ns	
13	TV	Output Valid from Clock Low	—	50	ns	4.5V ≤ VCC < 5.5V
			—	100	ns	2.5V ≤ VCC < 4.5V
			—	160	ns	1.8V ≤ VCC < 2.5V
14	THO	Output Hold Time	0	—	ns	Note 1

Note 1: This parameter is periodically sampled and not 100% tested.

2: TWC begins on the rising edge of $\overline{CS}$ after a valid write sequence and ends when the internal write cycle is complete.

3: This parameter is not tested but ensured by characterization. For endurance estimates in a specific application, please consult the Total Endurance™ Model which can be obtained from Microchip's website at www.microchip.com.

TABLE 1-2: AC CHARACTERISTICS (CONTINUED)

AC CHARACTERISTICS			Industrial (I): T_A = -40°C to +85°C V_{CC} = 1.8V to 5.5V			
Param. No.	**Symbol**	**Characteristic**	**Min.**	**Max.**	**Units**	**Test Conditions**
15	T_{DIS}	Output Disable Time	—	40	ns	4.5V ≤ V_{CC} < 5.5V (**Note 1**)
			—	80	ns	2.5V ≤ V_{CC} < 4.5V (**Note 1**)
			—	160	ns	1.8V ≤ V_{CC} < 2.5V (**Note 1**)
16	T_{HS}	$\overline{\text{HOLD}}$ Setup Time	20	—	ns	4.5V ≤ V_{CC} < 5.5V
			40	—	ns	2.5V ≤ V_{CC} < 4.5V
			80	—	ns	1.8V ≤ V_{CC} < 2.5V
17	T_{HH}	$\overline{\text{HOLD}}$ Hold Time	20	—	ns	4.5V ≤ V_{CC} < 5.5V
			40	—	ns	2.5V ≤ V_{CC} < 4.5V
			80	—	ns	1.8V ≤ V_{CC} < 2.5V
18	T_{HZ}	$\overline{\text{HOLD}}$ Low to Output High-Z	30	—	ns	4.5V ≤ V_{CC} < 5.5V (**Note 1**)
			60	—	ns	2.5V ≤ V_{CC} < 4.5V (**Note 1**)
			160	—	ns	1.8V ≤ V_{CC} < 2.5V (**Note 1**)
19	T_{HV}	$\overline{\text{HOLD}}$ High to Output Valid	30	—	ns	4.5V ≤ V_{CC} < 5.5V
			60	—	ns	2.5V ≤ V_{CC} < 4.5V
			160	—	ns	1.8V ≤ V_{CC} < 2.5V
20	T_{WC}	Internal Write Cycle Time (byte or page)	—	5	ms	**Note 2**
21		Endurance	1M	—	E/W cycles	25°C, V_{CC} = 5.5V (**Note 3**)

Note 1: This parameter is periodically sampled and not 100% tested.

2: T_{WC} begins on the rising edge of $\overline{\text{CS}}$ after a valid write sequence and ends when the internal write cycle is complete.

3: This parameter is not tested but ensured by characterization. For endurance estimates in a specific application, please consult the Total Endurance™ Model which can be obtained from Microchip's website at www.microchip.com.

TABLE 1-3: AC TEST CONDITIONS

AC Waveform	
V_{LO} = 0.2V	
V_{HI} = V_{CC} - 0.2V	**Note 1**
V_{HI} = 4.0V	**Note 2**
C_L = 100 pF	
Timing Measurement Reference Level	
Input	0.5 V_{CC}
Output	0.5 V_{CC}

Note 1: For V_{CC} ≤ 4.0V

2: For V_{CC} > 4.0V

FIGURE 1-1: HOLD TIMING

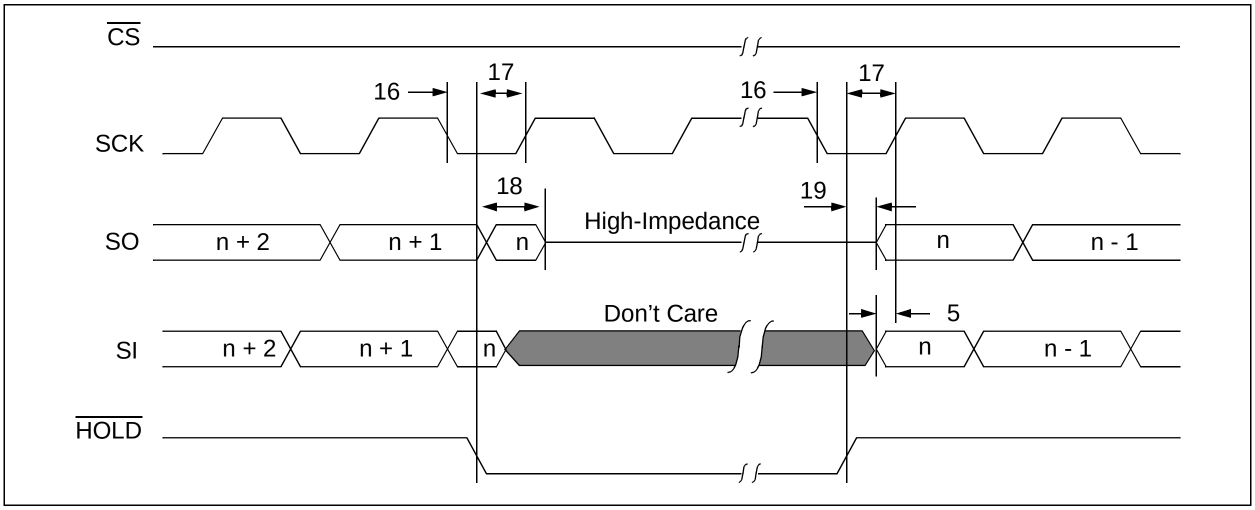


FIGURE 1-2: SERIAL INPUT TIMING

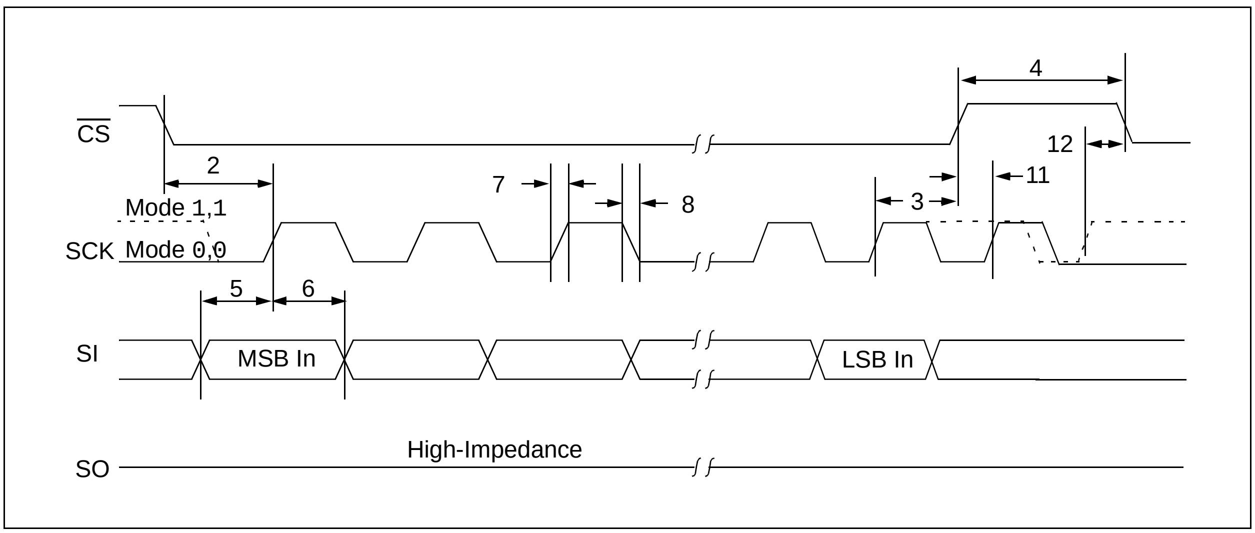
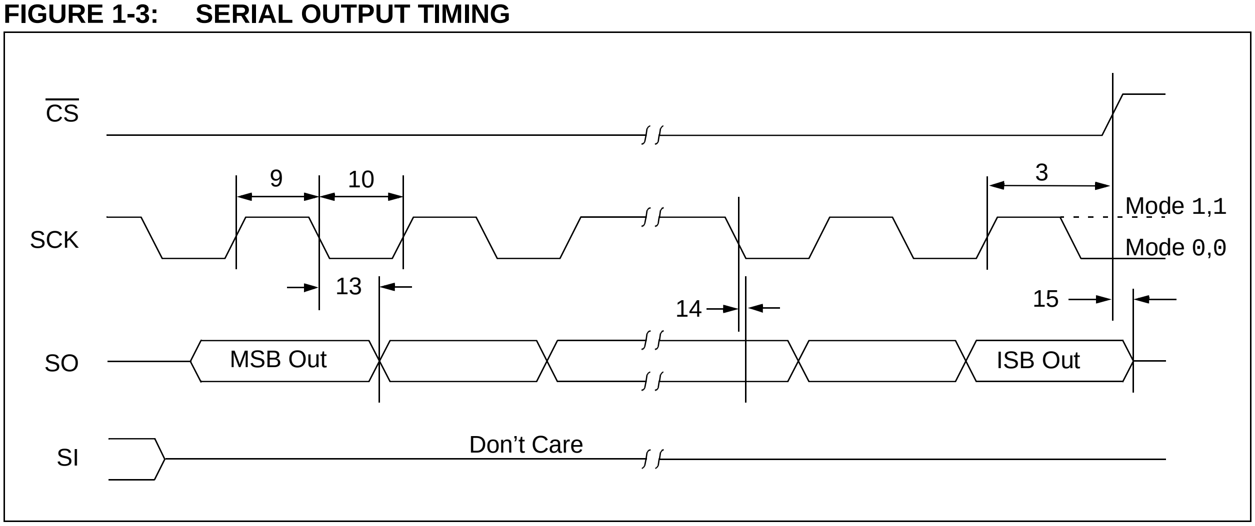


FIGURE 1-3: SERIAL OUTPUT TIMING



2.0 FUNCTIONAL DESCRIPTION

2.1 Principles of Operation

The 25AA02EXX is a 256-byte Serial EEPROM designed to interface directly with the Serial Peripheral Interface (SPI) port of many of today's popular microcontroller families, including Microchip's PIC® microcontrollers. It may also interface with microcontrollers that do not have a built-in SPI port by using discrete I/O lines programmed properly in software to match the SPI protocol.

The 25AA02EXX contains an 8-bit instruction register. The device is accessed via the SI pin, with data being clocked in on the rising edge of SCK. The CS pin must be low and the HOLD pin must be high for the entire operation.

Table 2-1 contains a list of the possible instruction bytes and format for device operation. All instructions, addresses, and data are transferred MSb first, LSb last.

Data (SI) is sampled on the first rising edge of SCK after CS goes low. If the clock line is shared with other peripheral devices on the SPI bus, the user can assert the HOLD input and place the 25AA02EXX in 'HOLD' mode. After releasing the HOLD pin, operation will resume from the point when the HOLD was asserted.

2.2 Read Sequence

The device is selected by pulling CS low. The 8-bit `READ` instruction is transmitted to the 25AA02EXX followed by an 8-bit address. See Figure 2-1 for more details.

After the correct `READ` instruction and address are sent, the data stored in the memory at the selected address is shifted out on the SO pin. Data stored in the memory at the next address can be read sequentially by continuing to provide clock pulses to the slave. The internal Address Pointer automatically increments to the next higher address after each byte of data is shifted out. When the highest address is reached (FFh), the address counter rolls over to address 00h allowing the read cycle to be continued indefinitely. The read operation is terminated by raising the CS pin (Figure 2-1).

2.3 Write Sequence

Prior to any attempt to write data to the 25AA02EXX, the write enable latch must be set by issuing the `WREN` instruction (Figure 2-4). This is done by setting CS low and then clocking out the proper instruction into the 25AA02EXX. After all eight bits of the instruction are transmitted, CS must be driven high to set the write enable latch. If the write operation is initiated immediately after the `WREN` instruction without CS driven high, data will not be written to the array since the write enable latch was not properly set.

After setting the write enable latch, the user may proceed by driving CS low, issuing a `WRITE` instruction, followed by the remainder of the address, and then the data to be written. Up to 16 bytes of data can be sent to the device before a write cycle is necessary. The only restriction is that all of the bytes must reside in the same page. Additionally, a page address begins with `XXXX 0000` and ends with `XXXX 1111`. If the internal address counter reaches `XXXX 1111` and clock signals continue to be applied to the chip, the address counter will roll back to the first address of the page and over-write any data that previously existed in those locations.

Note:	Page write operations are limited to writing bytes within a single physical page, **regardless** of the number of bytes actually being written. Physical page boundaries start at addresses that are integer multiples of the page buffer size (or 'page size') and, end at addresses that are integer multiples of page size – 1. If a Page Write command attempts to write across a physical page boundary, the result is that the data wraps around to the beginning of the current page (overwriting data previously stored there), instead of being written to the next page as might be expected. It is, therefore, necessary for the application software to prevent page write operations that would attempt to cross a page boundary.

For the data to be actually written to the array, the CS must be brought high after the Least Significant bit (D0) of the n^{th} data byte has been clocked in. If CS is driven high at any other time, the write operation will not be completed. Refer to Figure 2-2 and Figure 2-3 for more detailed illustrations on the byte write sequence and the page write sequence, respectively. While the write is in progress, the STATUS register may be read to check the status of the WIP, WEL, BP1 and BP0 bits (Figure 2-6). Attempting to read a memory array location will not be possible during a write cycle. Polling the WIP bit in the STATUS register is recommended in order to determine if a write cycle is in progress. When the write cycle is completed, the write enable latch is reset.

BLOCK DIAGRAM

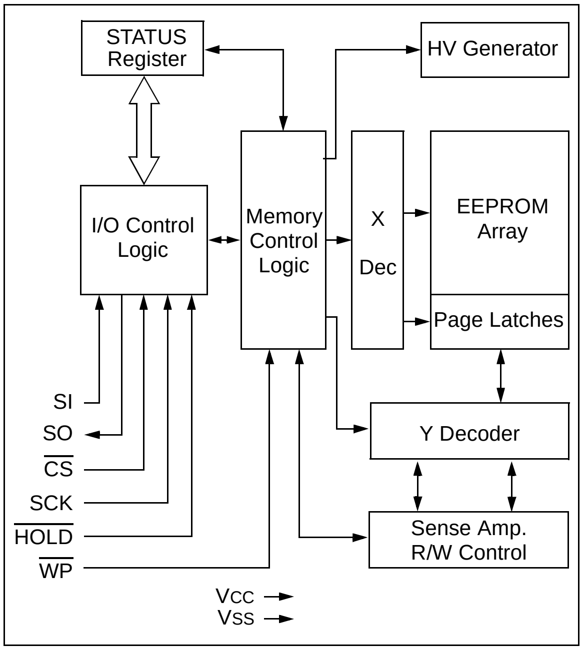


TABLE 2-1: INSTRUCTION SET

Instruction Name	Instruction Format	Description
READ	0000 x011	Read data from memory array beginning at selected address
WRITE	0000 x010	Write data to memory array beginning at selected address
WRDI	0000 x100	Reset the write enable latch (disable write operations)
WREN	0000 x110	Set the write enable latch (enable write operations)
RDSR	0000 x101	Read STATUS register
WRSR	0000 x001	Write STATUS register

x = don't care

FIGURE 2-1: READ SEQUENCE

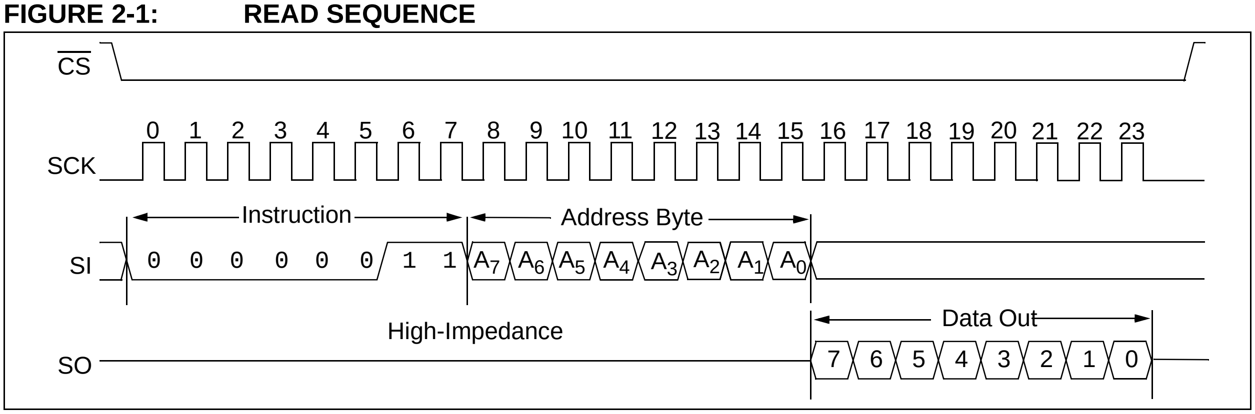


FIGURE 2-2: BYTE WRITE SEQUENCE

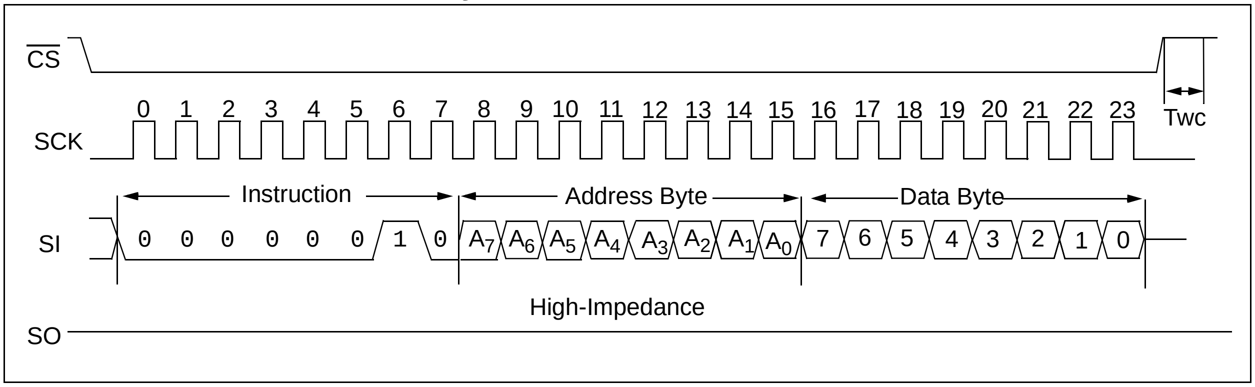
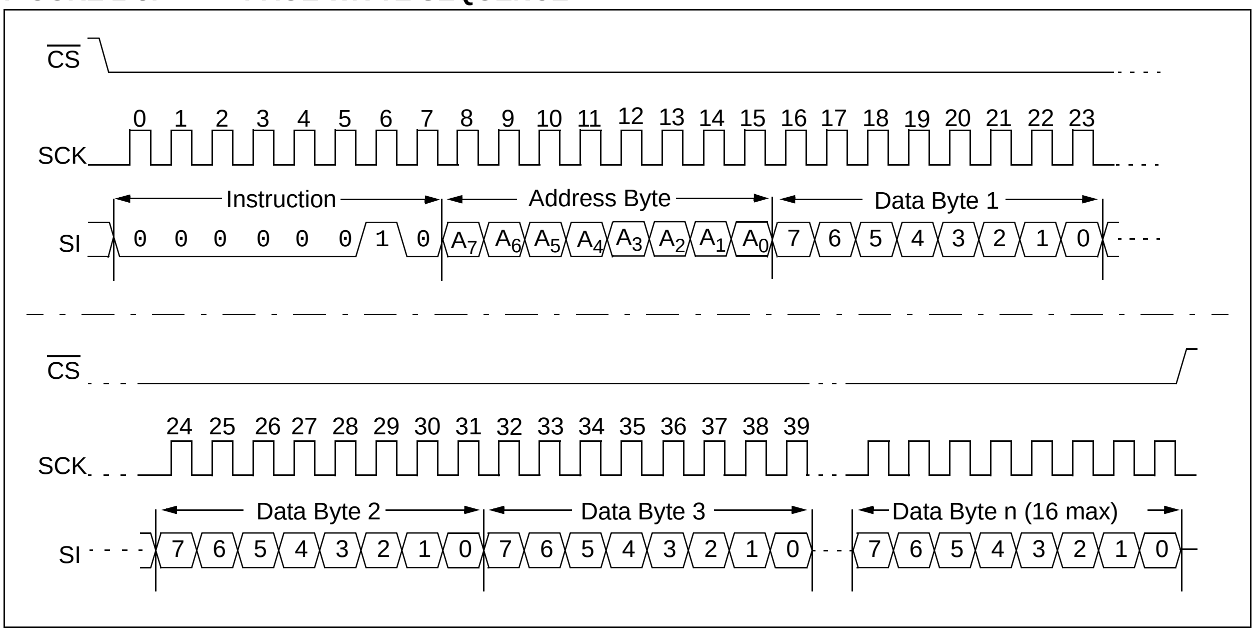


FIGURE 2-3: PAGE WRITE SEQUENCE



2.4 Write Enable (WREN) and Write Disable (WRDI)

The 25AA02EXX contains a write enable latch. See Table 2-4 for the Write-Protect Functionality Matrix. This latch must be set before any write operation will be completed internally. The WREN instruction will set the latch, and the WRDI will reset the latch.

The following is a list of conditions under which the write enable latch will be reset:

- Power-up
- WRDI instruction successfully executed
- WRSR instruction successfully executed
- WRITE instruction successfully executed
- $\overline{WP}$ pin is brought low

FIGURE 2-4: WRITE ENABLE SEQUENCE (WREN)

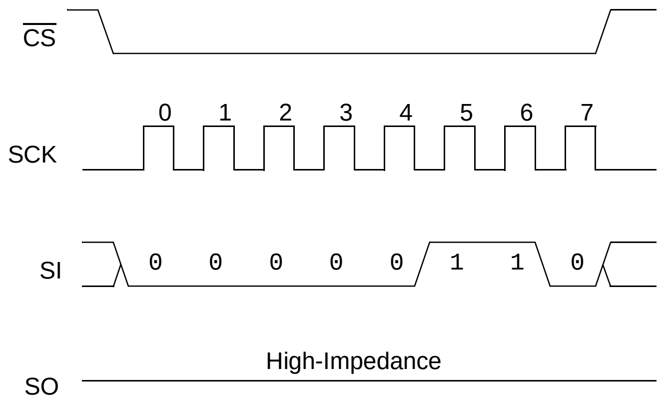
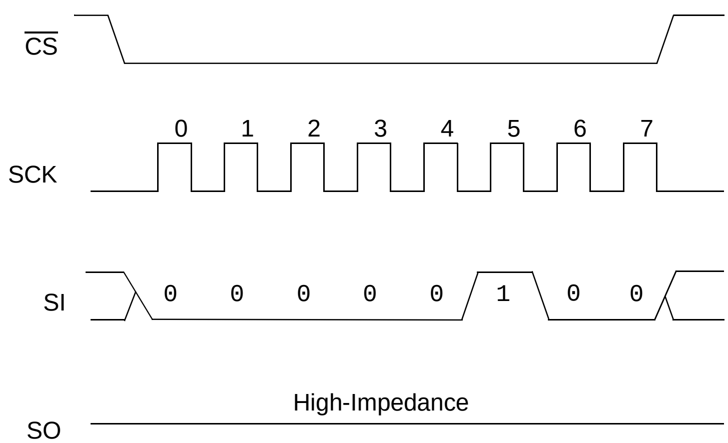


FIGURE 2-5: WRITE DISABLE SEQUENCE (WRDI)



2.5 Read Status Register Instruction (RDSR)

The Read Status Register instruction (RDSR) provides access to the STATUS register. See Figure 2-6 for the RDSR timing sequence. The STATUS register may be read at any time, even during a write cycle. The STATUS register is formatted as follows:

TABLE 2-2: STATUS REGISTER

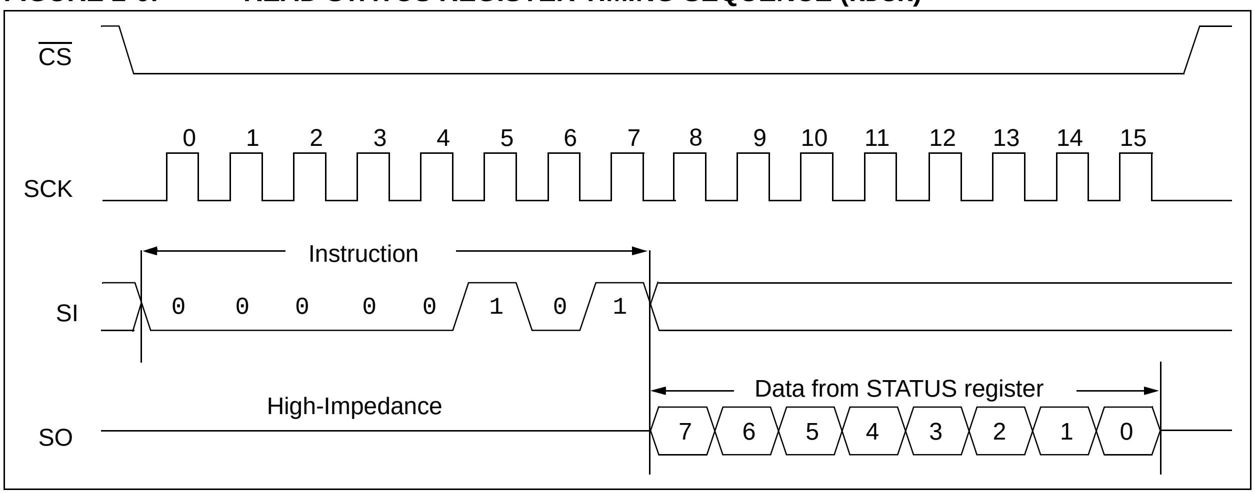
7	6	5	4	3	2	1	0
–	–	–	–	W/R	W/R	R	R
X	X	X	X	BP1	BP0	WEL	WIP
W/R = writable/readable. R = read-only.							

The **Write-In-Process (WIP)** bit indicates whether the 25AA02EXX is busy with a write operation. When set to a '1', a write is in progress, when set to a '0', no write is in progress. This bit is read-only.

The **Write Enable Latch (WEL)** bit indicates the status of the write enable latch and is read-only. When set to a '1', the latch allows writes to the array, when set to a '0', the latch prohibits writes to the array. The state of this bit can always be updated via the WREN or WRDI commands regardless of the state of write protection on the STATUS register. These commands are shown in Figure 2-4 and Figure 2-5.

The **Block Protection (BP0 and BP1)** bits indicate which blocks are currently write-protected. These bits are set by the user issuing the WRSR instruction, which is shown in Figure 2-7. These bits are nonvolatile and are described in more detail in Table 2-3.

FIGURE 2-6: READ STATUS REGISTER TIMING SEQUENCE (RDSR)



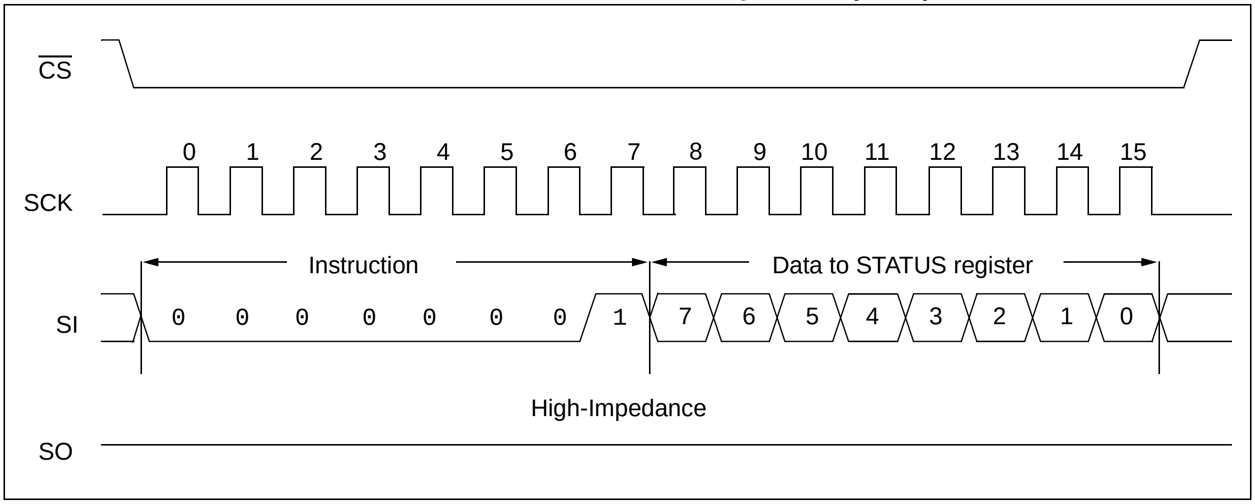
2.6 Write Status Register Instruction (WRSR)

The Write Status Register instruction (WRSR) allows the user to write to the nonvolatile bits in the STATUS register as shown in Table 2-2. See Figure 2-7 for the WRSR timing sequence. Four levels of protection for the array are selectable by writing to the appropriate bits in the STATUS register. The user has the ability to write-protect none, one, two, or all four of the segments of the array as shown in Table 2-3.

TABLE 2-3: ARRAY PROTECTION

BP1	BP0	Array Addresses Write-Protected
0	0	none
0	1	upper 1/4 (C0h-FFh)
1	0	upper 1/2 (80h-FFh)
1	1	all (00h-FFh)

FIGURE 2-7: WRITE STATUS REGISTER TIMING SEQUENCE (WRSR)



2.7 Data Protection

The following protection has been implemented to prevent inadvertent writes to the array:

- The write enable latch is reset on power-up
- A write enable instruction must be issued to set the write enable latch
- After a byte write, page write or STATUS register write, the write enable latch is reset
- $\overline{\text{CS}}$ must be set high after the proper number of clock cycles to start an internal write cycle
- Access to the array during an internal write cycle is ignored and programming is continued

2.8 Power-On State

The 25AA02EXX powers on in the following state:

- The device is in low-power Standby mode ($\overline{\text{CS}}$ = 1)
- The write enable latch is reset
- SO is in high-impedance state
- A high-to-low-level transition on $\overline{\text{CS}}$ is required to enter active state

TABLE 2-4: WRITE-PROTECT FUNCTIONALITY MATRIX

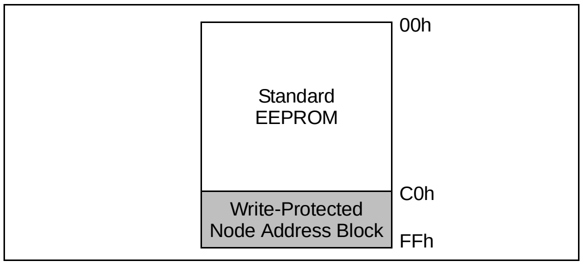
$\overline{\text{WP}}$ (pin 3)	WEL (SR bit 1)	Protected Blocks	Unprotected Blocks	STATUS Register
0 (low)	x	Protected	Protected	Protected
1 (high)	0	Protected	Protected	Protected
1 (high)	1	Protected	Writable	Writable

x = don't care

3.0 PREPROGRAMMED EUI-48™ OR EUI-64™ NODE ADDRESS

The 25AA02EXX is programmed at the factory with a globally unique node address stored in the upper 1/4 of the array and write-protected through the STATUS register. The remaining 1,536 bits are available for application use.

FIGURE 3-1: MEMORY ORGANIZATION



3.1 Factory-Programmed Write Protection

In order to help guard against accidental corruption of the node address, the BP1 and BP0 bits of the STATUS register are programmed at the factory to '0' and '1', respectively, as shown in the following table:

7	6	5	4	3	2	1	0
X	X	X	X	BP1	BP0	WEL	WIP
—	—	—	—	0	1	—	—

This protects the upper 1/4 of the array (0xC0 to 0xFF) from write operations. This array block can be utilized for writing by clearing the BP bits with a Write Status Register (WRSR) instruction. Note that if this is performed, care must be taken to prevent overwriting the node address value.

3.2 EUI-48™ Node Address (25AA02E48)

The 6-byte EUI-48™ node address value of the 25AA02E48 is stored in array locations 0xFA through 0xFF, as shown in Figure 3-2. The first three bytes are the Organizationally Unique Identifier (OUI) assigned to Microchip by the IEEE Registration Authority. The remaining three bytes are the Extension Identifier, and are generated by Microchip to ensure a globally unique, 48-bit value.

3.2.1 ORGANIZATIONALLY UNIQUE IDENTIFIERS (OUIs)

Each OUI provides roughly 16M (2^{24}) addresses. Once the address pool for an OUI is exhausted, Microchip will acquire a new OUI from IEEE to use for programming this model. For more information on past and current OUIs see *"Organizationally Unique Identifiers For Preprogrammed EUI-48 and EUI-64 Address Devices"* Technical Brief (DS90003187).

> **Note:** The OUI will change as addresses are exhausted. Customers are not guaranteed to receive a specific OUI and should design their application to accept new OUIs as they are introduced.

3.2.2 EUI-64™ SUPPORT USING THE 25AA02E48

The preprogrammed EUI-48 node address of the 25AA02E48 can easily be encapsulated at the application level to form a globally unique, 64-bit node address for systems utilizing the EUI-64 standard. This is done by adding 0xFFFE between the OUI and the Extension Identifier, as shown below.

> **Note:** As an alternative, the 25AA02E64 features an EUI-64 node address that can be used in EUI-64 applications directly without the need for encapsulation, thereby simplifying system software. See **Section 3.3 "EUI-64™ Node Address (25AA02E64)"** for details.

FIGURE 3-2: EUI-48 NODE ADDRESS PHYSICAL MEMORY MAP EXAMPLE (25AA02E48)

Description	24-bit Organizationally Unique Identifier			24-bit Extension Identifier		
Data	00h	04h	A3h	12h	34h	56h
Array Address	FAh					FFh

Corresponding EUI-48™ Node Address: 00-04-A3-12-34-56

Corresponding EUI-64™ Node Address After Encapsulation: 00-04-A3-FF-FE-12-34-56

3.3 EUI-64™ Node Address (25AA02E64)

The 8-byte EUI-64™ node address value of the 25AA02E64 is stored in array locations 0xF8 through 0xFF, as shown in Figure 3-3. The first three bytes are the Organizationally Unique Identifier (OUI) assigned to Microchip by the IEEE Registration Authority. The remaining five bytes are the Extension Identifier, and are generated by Microchip to ensure a globally unique, 64-bit value.

Note:	In conformance with IEEE guidelines, Microchip will not use the values 0xFFFE and 0xFFFF for the first two bytes of the EUI-64 Extension Identifier. These two values are specifically reserved to allow applications to encapsulate EUI-48 addresses into EUI-64 addresses.

FIGURE 3-3: EUI-64 NODE ADDRESS PHYSICAL MEMORY MAP EXAMPLE (25AA02E64)

Description	24-bit Organizationally Unique Identifier			40-bit Extension Identifier				
Data	00h	04h	A3h	12h	34h	56h	78h	90h
Array Address	F8h							FFh

Corresponding EUI-64™ Node Address: 00-04-A3-12-34-56-78-90

4.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 4-1.

TABLE 4-1: PIN FUNCTION TABLE

Name	SOIC	SOT-23	Function
$\overline{CS}$	1	5	Chip Select Input
SO	2	4	Serial Data Output
$\overline{WP}$	3	—	Write-Protect Pin
VSS	4	2	Ground
SI	5	3	Serial Data Input
SCK	6	1	Serial Clock Input
$\overline{HOLD}$	7	—	Hold Input
VCC	8	6	Supply Voltage

4.1 Chip Select ($\overline{CS}$)

A low level on this pin selects the device. A high level deselects the device and forces it into Standby mode. However, a programming cycle which is already initiated or in progress will be completed, regardless of the $\overline{CS}$ input signal. If $\overline{CS}$ is brought high during a program cycle, the device will go into Standby mode as soon as the programming cycle is complete. When the device is deselected, SO goes to the high-impedance state, allowing multiple parts to share the same SPI bus. A low-to-high transition on $\overline{CS}$ after a valid write sequence initiates an internal write cycle. After power-up, a low level on $\overline{CS}$ is required prior to any sequence being initiated.

4.2 Serial Output (SO)

The SO pin is used to transfer data out of the 25AA02EXX. During a read cycle, data is shifted out on this pin after the falling edge of the serial clock.

4.3 Write-Protect ($\overline{WP}$)

The $\overline{WP}$ pin is a hardware write-protect input pin. When it is low, all writes to the array or STATUS register are disabled, but any other operations function normally. When $\overline{WP}$ is high, all functions, including nonvolatile writes, operate normally. At any time when $\overline{WP}$ is low, the write enable Reset latch will be reset and programming will be inhibited. However, if a write cycle is already in progress, $\overline{WP}$ going low will not change or disable the write cycle. See Table 2-4 for the Write-Protect Functionality Matrix.

4.4 Serial Input (SI)

The SI pin is used to transfer data into the device. It receives instructions, addresses and data. Data is latched on the rising edge of the serial clock.

4.5 Serial Clock (SCK)

The SCK is used to synchronize the communication between a master and the 25AA02EXX. Instructions, addresses or data present on the SI pin are latched on the rising edge of the clock input, while data on the SO pin is updated after the falling edge of the clock input.

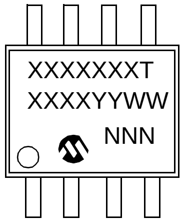
4.6 Hold ($\overline{HOLD}$)

The $\overline{HOLD}$ pin is used to suspend transmission to the 25AA02EXX while in the middle of a serial sequence without having to retransmit the entire sequence again. It must be held high any time this function is not being used. Once the device is selected and a serial sequence is underway, the $\overline{HOLD}$ pin may be pulled low to pause further serial communication without resetting the serial sequence. The $\overline{HOLD}$ pin must be brought low while SCK is low, otherwise the HOLD function will not be invoked until the next SCK high-to-low transition. The 25AA02EXX must remain selected during this sequence. The SI, SCK and SO pins are in a high-impedance state during the time the device is paused and transitions on these pins will be ignored. To resume serial communication, $\overline{HOLD}$ must be brought high while the SCK pin is low, otherwise serial communication will not resume. Lowering the HOLD line at any time will tri-state the SO line.

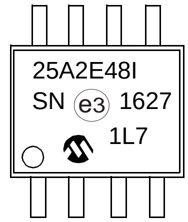
5.0 PACKAGING INFORMATION

5.1 Package Marking Information*

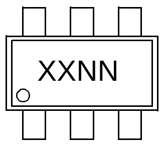
8-Lead SOIC



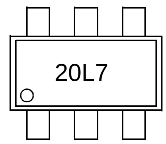
Example



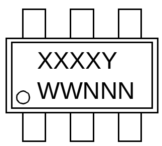
6-Lead SOT-23 (25AA02E48)



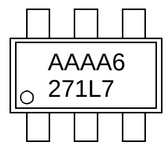
Example



6-Lead SOT-23 (25AA02E64)



Example



Part Number	1st Line Marking Code	
	SOIC	**SOT-23**
25AA02E48	25A2E48I	20NN
25AA02E64	25A2E64I	AAAAY

Legend:

XX...X	Part number or part number code
T	Temperature (I, E)
Y	Year code (last digit of calendar year)
YY	Year code (last 2 digits of calendar year)
WW	Week code (week of January 1 is week ‘01’)
NNN	Alphanumeric traceability code (2 characters for small packages)
(e3)	Pb-free** JEDEC® designator for Matte Tin (Sn)

* Standard OTP marking consists of Microchip part number, year code, week code, and traceability code.

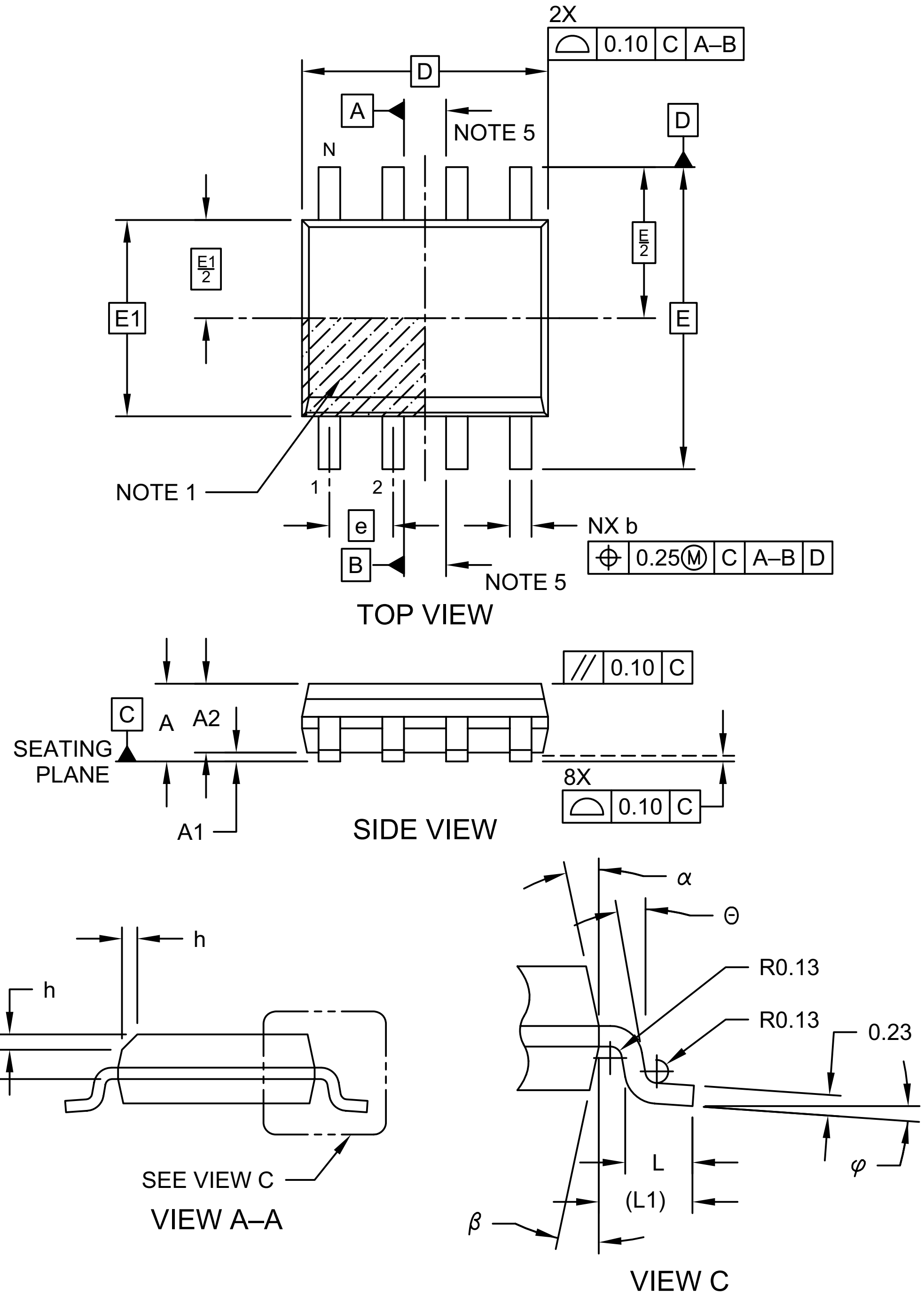
** Please visit www.microchip.com/Pbfree for the latest information on Pb-free conversion.

Note: For very small packages with no room for the Pb-free JEDEC designator (e3), the marking will only appear on the outer carton or reel label.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

8-Lead Plastic Small Outline (SN) - Narrow, 3.90 mm (.150 In.) Body [SOIC]

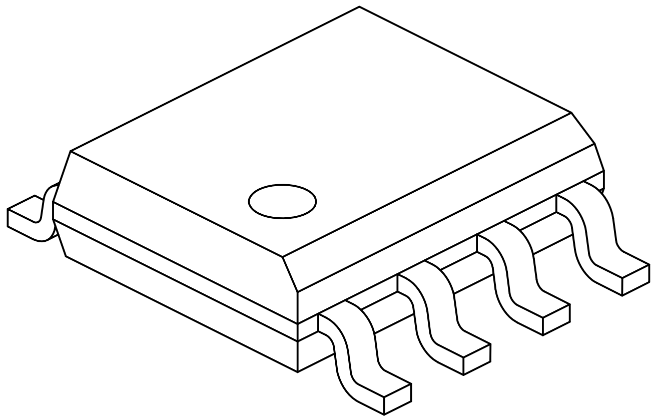
Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing No. C04-057-SN Rev D Sheet 1 of 2

8-Lead Plastic Small Outline (SN) - Narrow, 3.90 mm (.150 In.) Body [SOIC]

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



	Units	MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		8	
Pitch	e		1.27 BSC	
Overall Height	A	-	-	1.75
Molded Package Thickness	A2	1.25	-	-
Standoff §	A1	0.10	-	0.25
Overall Width	E		6.00 BSC	
Molded Package Width	E1		3.90 BSC	
Overall Length	D		4.90 BSC	
Chamfer (Optional)	h	0.25	-	0.50
Foot Length	L	0.40	-	1.27
Footprint	L1		1.04 REF	
Foot Angle	φ	0°	-	8°
Lead Thickness	c	0.17	-	0.25
Lead Width	b	0.31	-	0.51
Mold Draft Angle Top	α	5°	-	15°
Mold Draft Angle Bottom	β	5°	-	15°

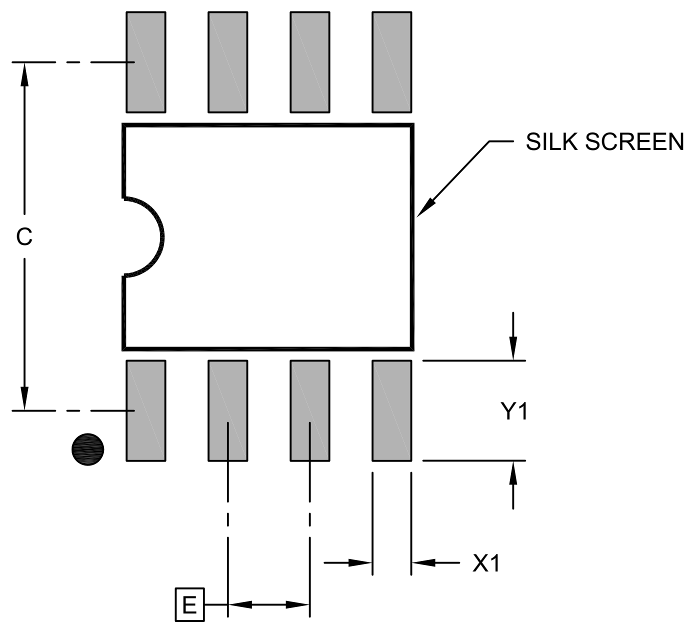
Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.
5. Datums A & B to be determined at Datum H.

Microchip Technology Drawing No. C04-057-SN Rev D Sheet 2 of 2

8-Lead Plastic Small Outline (SN) - Narrow, 3.90 mm Body [SOIC]

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

	Units	MILLIMETERS		
	Dimension Limits	MIN	NOM	MAX
Contact Pitch	E	1.27 BSC		
Contact Pad Spacing	C		5.40	
Contact Pad Width (X8)	X1			0.60
Contact Pad Length (X8)	Y1			1.55

Notes:

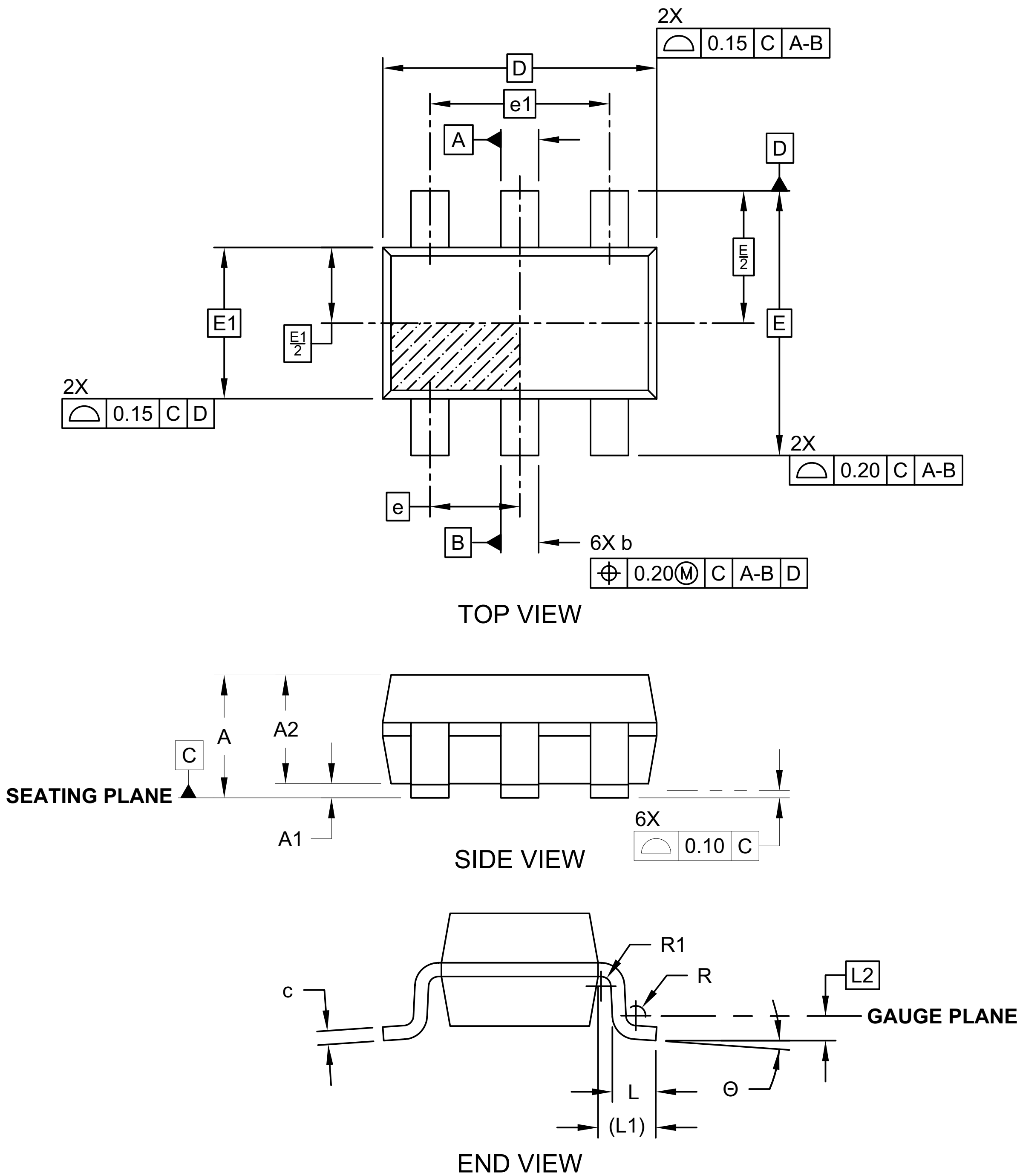
1. Dimensioning and tolerancing per ASME Y14.5M

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-2057-SN Rev B

6-Lead Plastic Small Outline Transistor (OT, OTY) [SOT-23]

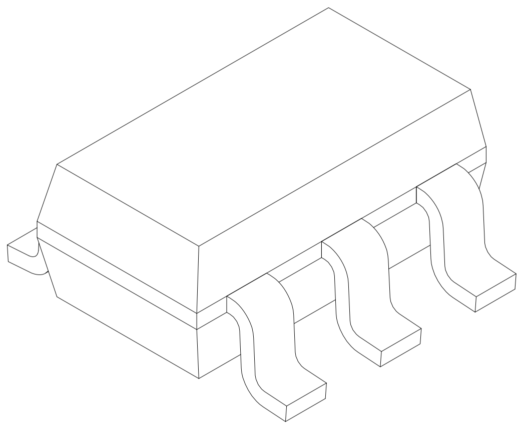
Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing C04-028C (OT) Sheet 1 of 2

6-Lead Plastic Small Outline Transistor (OT, OTY) [SOT-23]

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



	Units	MILLIMETERS		
	Dimension Limits	MIN	NOM	MAX
Number of Leads	N	6		
Pitch	e	0.95 BSC		
Outside lead pitch	e1	1.90 BSC		
Overall Height	A	0.90	-	1.45
Molded Package Thickness	A2	0.89	1.15	1.30
Standoff	A1	0.00	-	0.15
Overall Width	E	2.80 BSC		
Molded Package Width	E1	1.60 BSC		
Overall Length	D	2.90 BSC		
Foot Length	L	0.30	0.45	0.60
Footprint	L1	0.60 REF		
Seating Plane to Gauge Plane	L1	0.25 BSC		
Foot Angle	ϕ	0°	-	10°
Lead Thickness	c	0.08	-	0.26
Lead Width	b	0.20	-	0.51

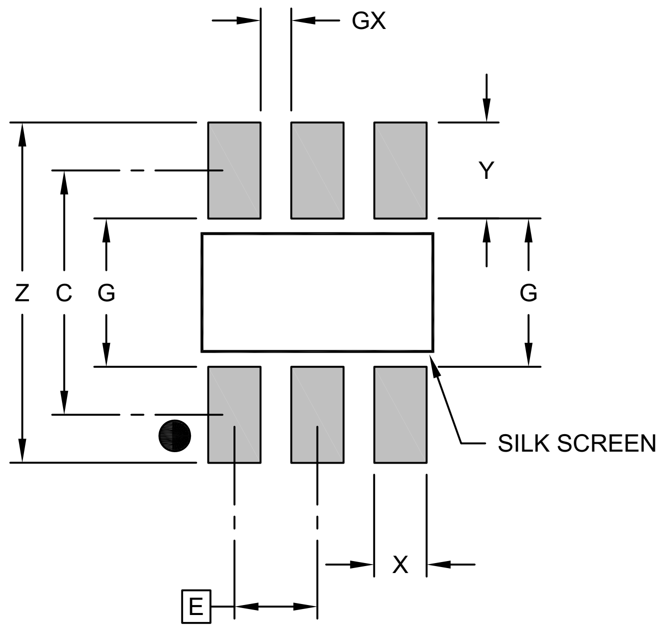
Notes:

1. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.25mm per side.
2. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-028C (OT) Sheet 2 of 2

6-Lead Plastic Small Outline Transistor (OT, OTY) [SOT-23]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	0.95 BSC		
Contact Pad Spacing	C		2.80	
Contact Pad Width (X3)	X			0.60
Contact Pad Length (X3)	Y			1.10
Distance Between Pads	G	1.70		
Distance Between Pads	GX	0.35		
Overall Width	Z			3.90

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2028B (OT)

APPENDIX A: REVISION HISTORY

Revision A (12/08)

Initial release of this document.

Revision B (04/10)

Removed Preliminary status; Revised Section 2.0; Add sentence to Section 3.0; Add SOT-23 Land Pattern.

Revision C (12/2012)

Revised Table 1-2, Parameter 21.

Revision D (4/2013)

Added 25AA02E64 part number.

Revision E (01/2015)

Updated Section 3.0; Updated Product Identification System.

Revision F (07/2016)

Added new OUI (54-10-EC) to list.

Revision G (02/2018)

Added detailed description of OUIs.

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NOTES:

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	[X][(1)]	X	/XX
Device	Tape and Reel Option	Temperature Range	Package

Device:	25AA02E48	=	2 Kbit, 1.8V, 16-Byte Page, SPI Serial EEPROM with EUI-48™ Node Identity
	25AA02E64	=	2 Kbit, 1.8V, 16-Byte Page, SPI Serial EEPROM with EUI-64™ Node Identity
Tape and Reel Option:	Blank	=	Standard packaging (tube or tray)
	T	=	Tape and Reel(1)
Temperature Range:	I	=	-40°C to+85°C
Package:	SN	=	Plastic SOIC (3.90 mm body), 8-lead
	OT	=	SOT-23, 6-lead (Tape and Reel only)

Examples:

a) 25AA02E48-I/SN = 2 Kbit, 16-byte page, 1.8V Serial EEPROM with EUI-48 Node Identity, Industrial temperature, SOIC package.

b) 25AA02E48T-I/SN = 2 Kbit, 16-byte page, 1.8V Serial EEPROM with EUI-48 Node Identity, Tape & Reel, Industrial temp., SOIC package.

c) 25AA02E48T-I/OT = 2 Kbit, 16-byte page, 1.8V Serial EEPROM with EUI-48 Node Identity, Tape & Reel, Industrial temp., SOT-23 package.

d) 25AA02E64-I/SN = 2 Kbit, 16-byte page, 1.8V Serial EEPROM with EUI-64 Node Identity, Industrial temp., SOIC package.

e) 25AA02E64T-I/SN = 2 Kbit, 16-byte page, 1.8V Serial EEPROM with EUI-64 Node Identity, Tape & Reel, Industrial temp., SOIC package.

f) 25AA02E64T-I/OT = 2 Kbit, 16-byte page, 1.8V Serial EEPROM with EUI-64 Node Identity, Tape & Reel, Industrial temp., SOT-23 package.

Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

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