Vishay Siliconix



SPECIFICATIONS (T_A = 25°C UNLESS OTHERWISE NOTED) Limits 2N5565 2N5564 2N5566 Parameter Symbol **Test Conditions** Typ^a Min Max Min Max Min Max Unit Static Gate-Source V_{(BR)GSS} -40 -40 -40 $I_G = -1 \ \mu A, \ V_{DS} = 0 \ V$ -55 Breakdown Voltage v Gate-Source V_{DS} = 15 V, I_D = 1 nA -0.5 -0.5 -3 -0.5 V_{GS(off)} -2 -3 -3 Cutoff Voltage Saturation Drain $V_{DS} = 15 \text{ V}, V_{GS} = 0 \text{ V}$ 20 5 30 5 30 5 30 mA IDSS Currentb $V_{GS} = -20 \text{ V}, \text{ V}_{DS} = 0 \text{ V}$ -100 -100 -100 -5 pA Gate Reverse Current IGSS $T_A = 150^{\circ}C$ -10 -200 -200 -200 nA V_{DG} = 15 V, I_D = 2 mA -3 pА Gate Operating Current^c IG $T_A = 125^{\circ}C$ -1 nA Drain-Source $V_{GS} = 0 V$, $I_D = 1 mA$ 50 100 100 100 Ω r_{DS(on)} **On-Resistance** Gate-Source Voltagec -1.2 V_{DG} = 15 V, I_D = 2 mA VGS V Gate-Source V_{GS(F)} $I_G = 2 \text{ mA}$, $V_{DS} = 0 \text{ V}$ 0.7 1 1 1 Forward Voltage Dynamic Common-Source 9 7.5 12.5 7.5 12.5 7.5 12.5 mS g_{fs} Forward Transconductance V_{DS} = 15 V, I_D = 2 mA Common-Source f = 1 kHz35 45 45 45 μS g_{os} **Output Conductance** V_{DS} = 15 V, I_D = 2 mA f = 100 MHz Common-Source 8.5 7 7 7 mS g_{fs} Forward Transconductanced Common-Source 10 12 12 12 Ciss Input Capacitance $V_{DS} = 15 \text{ V}, \text{ I}_D = 2 \text{ mA}$ f = 1 MHz pF Common-Source з з з 2.5 Reverse Transfer Crss Capacitance Equivalent Input V_{DS} = 15 V, I_D = 2 mA nV/ 12 50 50 50 en Noise Voltage f = 10 Hz√Hz Noise Figure NF R_G = 10 M Ω dB 1 1 1 Matching Differential V_{DG} = 15 V, I_D = 2 mA 5 10 20 mV |V_{GS1}-V_{GS2}| Gate-Source Voltage Gate-Source Voltage $V_{DG} = 15 \text{ V}, \text{ I}_{D} = 2 \text{ mA}$ $T_{A} = -55 \text{ to } 125^{\circ}\text{C}$ $\Delta |V_{GS1} - V_{GS2}|$ μV/ Differential Change 10 25 50 °C ΔT with Temperature Saturation Drain I_{DSS1} V_{DS} = 15 V, V_{GS} = 0 V 0.98 0.95 0.95 1 0.95 1 1 Current Ratioc I_{DSS2} V_{DS} = 15 V, I_D = 2 mA g_{fs1} 0.98 0.90 Transconductance Ratio 0.95 1 0.90 1 1 f = 1 kHzg_{fs2} V_{DG} = 10 to 20 V Common Mode CMRR 76 dB Rejection Ratioc $I_D = 2 \text{ mA}$

Notes

a. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.

NCBD

b. Pulse test: PW \leq 300 μ s duty cycle \leq 3%.

c. This parameter not registered with JEDEC.

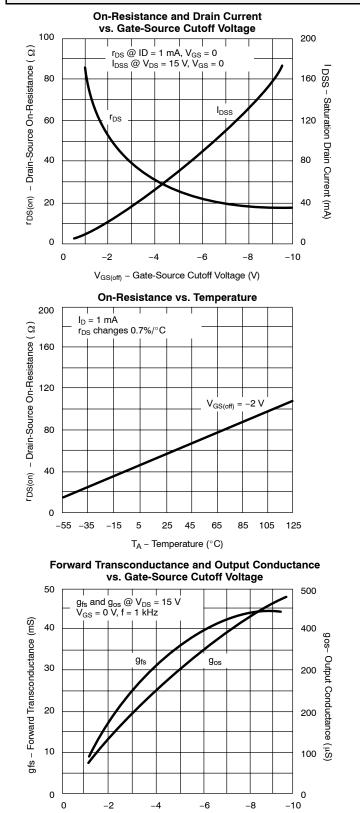
d. Not a production test.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

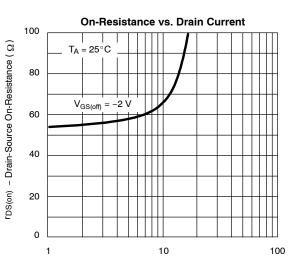


2N5564/5565/5566 Vishay Siliconix

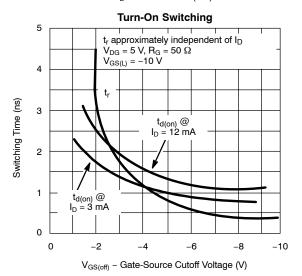
TYPICAL CHARACTERISTICS (T_A = 25°C UNLESS OTHERWISE NOTED)

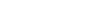


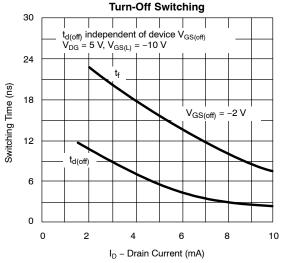
V_{GS(off)} - Gate-Source Cutoff Voltage (V)



I_D – Drain Current (mA)







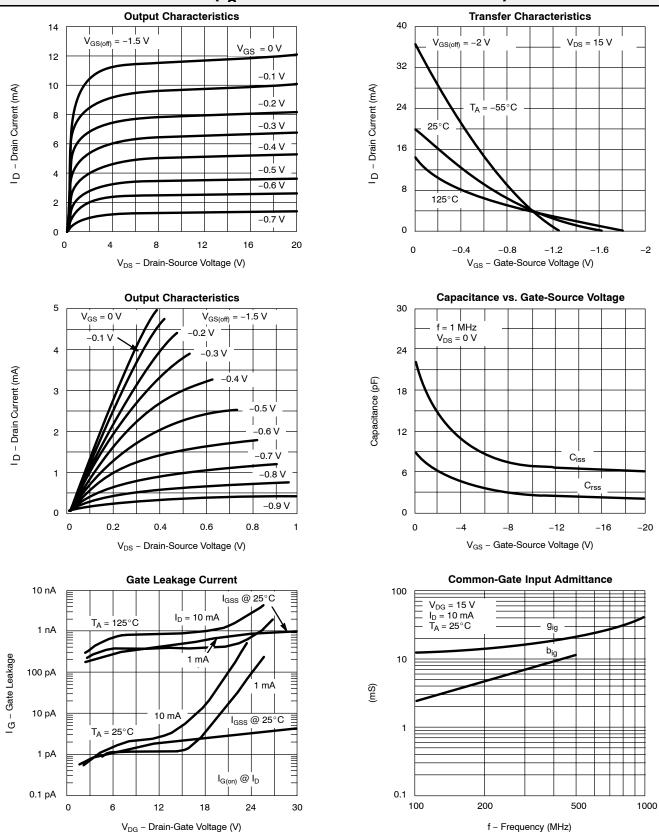
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2N5564/5565/5566

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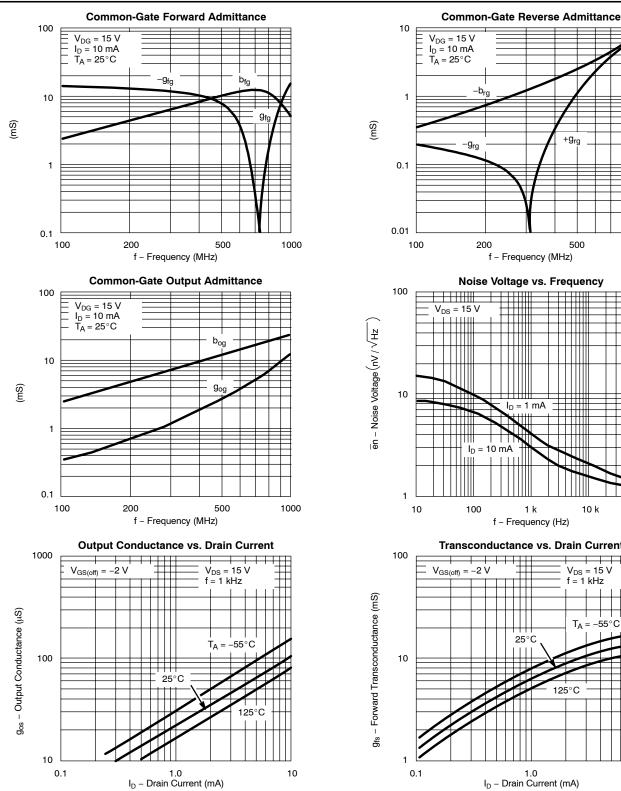


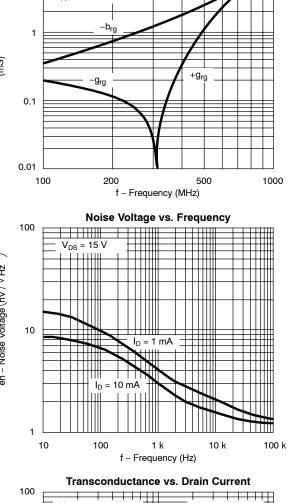
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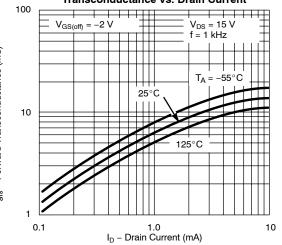
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Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see http://www.vishay.com/ppg?70254.

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