

ELECTRICAL SPECIFICATIONS					
PARAMETER	SYMBOL	TEST CONDITIONS		VALUES	UNITS
Maximum forward voltage drop See fig. 1	$V_{FM}^{(1)}$	1 A	$T_J = 25\text{ }^{\circ}\text{C}$	0.78	V
		2 A		0.89	
		1 A	$T_J = 125\text{ }^{\circ}\text{C}$	0.62	
		2 A		0.72	
Maximum reverse leakage current See fig. 2	$I_{RM}^{(1)}$	$T_J = 25\text{ }^{\circ}\text{C}$	$V_R = \text{Rated } V_R$	0.5	mA
		$T_J = 125\text{ }^{\circ}\text{C}$		1	
Typical junction capacitance	$C_T$	$V_R = 5\text{ V}_{DC}$ , (test signal range 100 kHz to 1 MHz) $25\text{ }^{\circ}\text{C}$		42	pF
Typical series inductance	$L_S$	Measured lead to lead 5 mm from package body		2.0	nH
Maximum voltage rate of charge	dV/dt	Rated $V_R$		10 000	V/ $\mu$ s

**Note**(1) Pulse width < 300  $\mu$ s, duty cycle < 2 %

THERMAL - MECHANICAL SPECIFICATIONS				
PARAMETER	SYMBOL	TEST CONDITIONS	VALUES	UNITS
Maximum junction and storage temperature range	$T_J^{(1)}, T_{Stg}$		- 55 to 175	$^{\circ}\text{C}$
Maximum thermal resistance, junction to lead	$R_{thJL}^{(2)}$	DC operation	36	$^{\circ}\text{C/W}$
Maximum thermal resistance, junction to ambient	$R_{thJA}$		80	
Approximate weight			0.10	g
			0.003	oz.
Marking device		Case style SMB (similar DO-214AA)	V1J	

**Notes**(1)  $\frac{dP_{tot}}{dT_J} < \frac{1}{R_{thJA}}$  thermal runaway condition for a diode on its own heatsink

(2) Mounted 1" square PCB

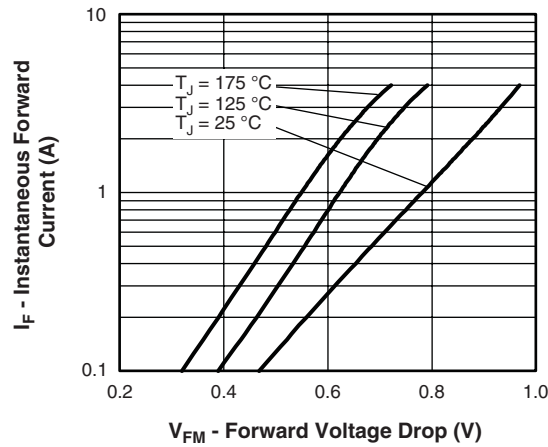


Fig. 1 - Maximum Forward Voltage Drop Characteristics

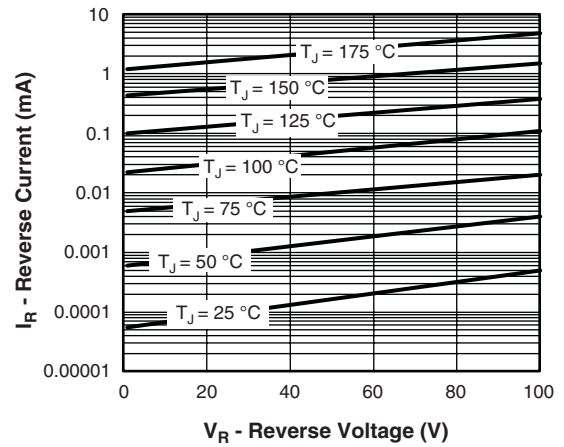


Fig. 2 - Typical Peak Reverse Current vs. Reverse Voltage

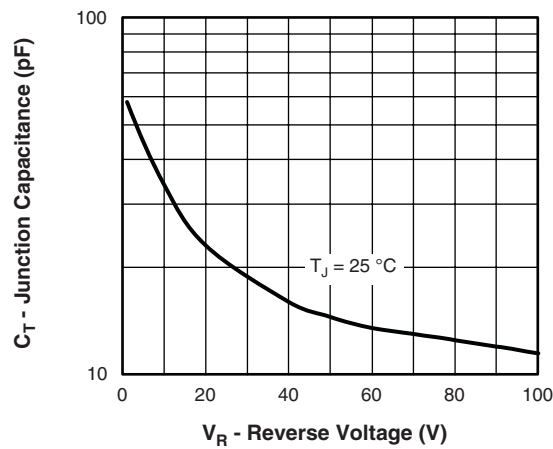


Fig. 3 - Typical Junction Capacitance vs. Reverse Voltage

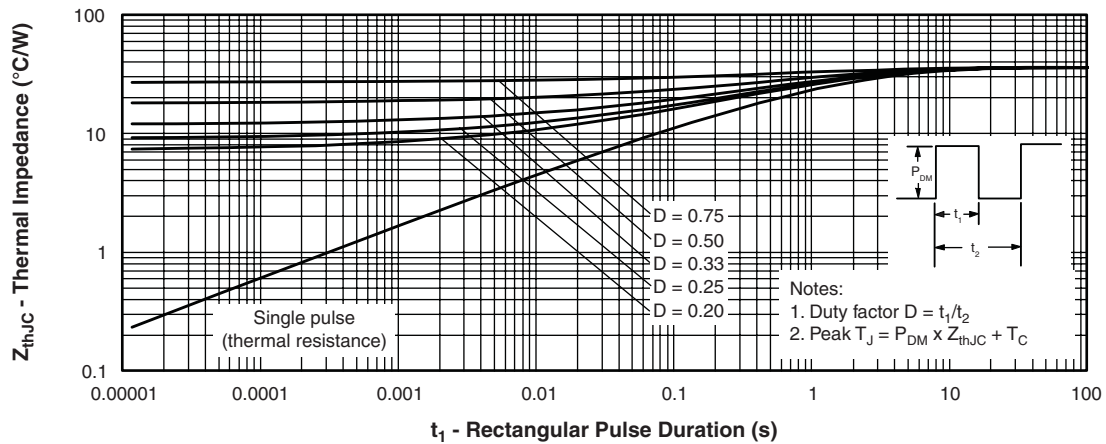


Fig. 4 - Maximum Thermal Impedance  $Z_{thJC}$  Characteristics (Per Leg)

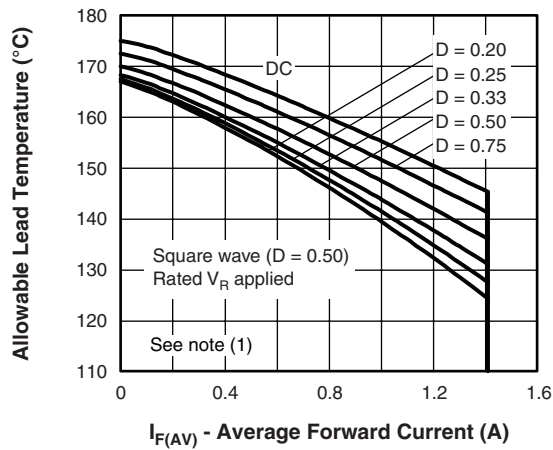


Fig. 5 - Maximum Average Forward Current vs. Allowable Lead Temperature

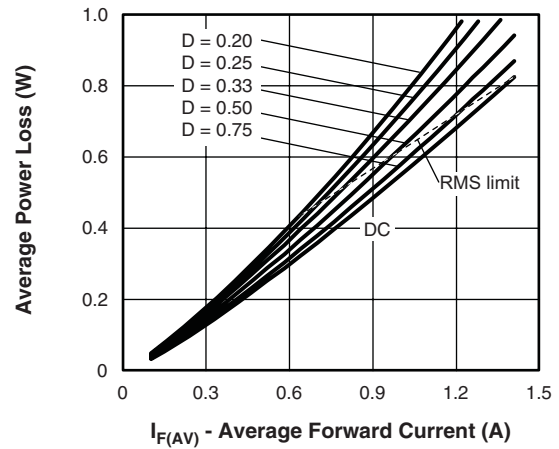


Fig. 6 - Maximum Average Forward Dissipation vs. Average Forward Current

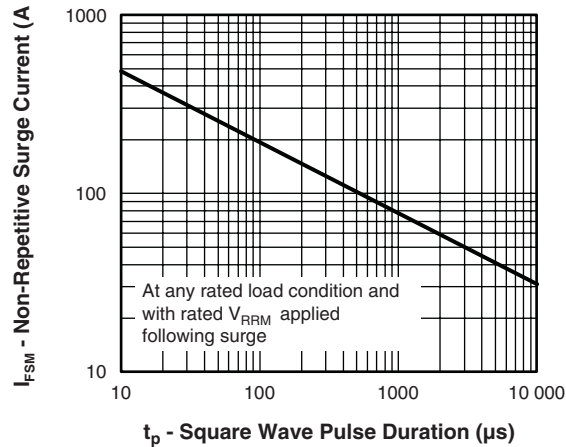


Fig. 7 - Maximum Peak Surge Forward Current vs. Pulse Duration

### Note

- (1) Formula used:  $T_C = T_J - (P_d + P_{dREV}) \times R_{thJC}$ ;  
 $P_d$  = Forward power loss =  $I_{F(AV)} \times V_{FM}$  at  $(I_{F(AV)}/D)$  (see fig. 6);  
 $P_{dREV}$  = Inverse power loss =  $V_{R1} \times I_R (1 - D)$ ;  $I_R$  at  $V_{R1} = 80\%$  rated  $V_R$

**ORDERING INFORMATION TABLE**

Device code	<b>10</b>	<b>B</b>	<b>Q</b>	<b>100</b>	<b>TR</b>	<b>PbF</b>
	①	②	③	④	⑤	⑥

- |          |   |   |
|----------|---|---|
| <b>1</b> | - | Current rating  |
| <b>2</b> | - | B = Single lead diode   |
| <b>3</b> | - | Q = Schottky "Q" series   |
| <b>4</b> | - | Voltage rating (100 = 100 V)  |
| <b>5</b> | - | <ul style="list-style-type: none"><li>• None = Box (1000 pieces)</li><li>• TR = Tape and reel (3000 pieces)</li></ul> |
| <b>6</b> | - | <ul style="list-style-type: none"><li>• None = Standard production</li><li>• PbF = Lead (Pb)-free</li></ul>           |

LINKS TO RELATED DOCUMENTS	
Dimensions	<a href="http://www.vishay.com/doc?95017">http://www.vishay.com/doc?95017</a>
Part marking information	<a href="http://www.vishay.com/doc?95029">http://www.vishay.com/doc?95029</a>
Packaging information	<a href="http://www.vishay.com/doc?95034">http://www.vishay.com/doc?95034</a>
SPICE model	<a href="http://www.vishay.com/doc?95276">http://www.vishay.com/doc?95276</a>



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