TABLE 1-1: DEVICE SELECTION TABLE

Part Number	Vcc Range	Max. Clock Frequency	Page Size	Write-Protect Array	Functional Address Pins	Temp. Range	Packages(5)
128-bit devices							
24AA00	1.7-5.5V	400 kHz(1)	—	None	None	I	P, SN, ST, OT, MC
24LC00	2.5-5.5V	400 kHz(1)				I	
24C00	4.5-5.5V	400 kHz				I, E	
1 Kb devices							
24AA01	1.7-5.5V	400 kHz (2)	8 bytes	Entire Array	None	I	P, SN, ST, MS, OT, MC
24LC01B	2.5-5.5V	400 kHz				I, E	
24AA014	1.7-5.5V	400 kHz(2)	16 bytes	Entire Array	A0, A1, A2	I	P, SN, ST, MS, MC
24LC014	2.5-5.5V	400 kHz				I	
24AA01H(6)	1.7-5.5v	400 kHz(1)	16 bytes	Upper Half	A0, A1, A2	I	P, SN, ST, MS, OT, MC
24LC01H(6)	2.5-5.5v	400 kHz(1)	16 bytes	Upper Half	A0, A1, A2	I, E	P, SN, ST, MS, OT, MC
24C01C	4.5V-5.5V	400 kHz	16 bytes	None	A0, A1, A2	I, E	P, SN, ST, MC
2 Kb devices							
24AA02	1.7-5.5V	400 kHz (2)	8 bytes	Entire Array	None	I	P, SN, ST, MS, OT, MC
24LC02B	2.5-5.5V	400 kHz				I, E	
24AA024	1.7-5.5V	400 kHz(2)	16 bytes	Entire Array	A0, A1, A2	I	P, SN, ST, MS, MC
24LC024	2.5-5.5V	400 kHz				I	
24AA025	1.7-5.5V	400 kHz(2)	16 bytes	None	A0, A1, A2	I	P, SN, ST,MS, MC
24LC025	2.5-5.5V	400 kHz				I	
24AA02H(6)	1.7-5.5v	400 kHz(1)	16 bytes	Upper Half	A0, A1, A2	I	P, SN, ST, MS, OT, MC
24LC02H(6)	2.5-5.5v	400 kHz(1)	16 bytes	Upper Half	A0, A1, A2	I, E	P, SN, ST, MS, OT, MC
24C02C	4.5-5.5V	400 kHz	16 bytes	Upper Half of Array	A0, A1, A2	I, E	P, SN, ST, MC
4 Kb devices							
24AA04	1.7-5.5V	400 kHz (2)	16 bytes	Entire Array	None	I	P, SN, ST, MS, OT, MC
24LC04B	2.5-5.5V	400 kHz				I, E	
8 Kb devices							
24AA08	1.7-5.5V	400 kHz (2)	16 bytes	Entire Array	None	I	P, SN, ST, MS, OT, MC
24LC08B	2.5-5.5V	400 kHz				I, E	
16 Kb devices							
24AA16	1.7-5.5V	400 kHz (2)	16 bytes	Entire Array	None	I	P, SN, ST, MS, OT, MC
24LC16B	2.5-5.5V	400 kHz				I, E	
32 Kb devices							
24AA32A	1.7-5.5V	400 kHz (2)	32 bytes	Entire Array	A0, A1, A2	I	P, SN, SM, ST, MS, MC
24LC32A	2.5-5.5V	400 kHz				I, E	

Note 1: 100 kHz for Vcc <4.5V.

2: 100 kHz for Vcc <2.5V.

3: 400 kHz for Vcc <2.5V.

4: Pins A0 and A1 are no-connects for the 24XX128 and 24XX256 in the MSOP package.

5: P = 8-PDIP, SN = 8-SOIC (3.90 mm JEDEC), ST = 8-TSSOP, OT = 5 or 6-SOT23, MC = 2x3mm DFN, MS = 8-MSOP, SM = 8-SOIC (200 mil EIAJ), MF = 5x6mm DFN.

6: Available Q4 2007.

TABLE 1-1: DEVICE SELECTION TABLE (CONTINUED)

Part Number	Vcc Range	Max. Clock Frequency	Page Size	Write-Protect Array	Functional Address Pins	Temp. Range	Packages(5)
64 Kb devices							
24AA64	1.7-5.5V	400 kHz (2)	32 bytes	Entire Array	A0, A1, A2	I	P, SN, SM, ST, MS, MC
24LC64	2.5-5.5V	400 kHz				I, E	
24FC64	1.7-5.5V	1 MHz(3)				I	
128 Kb devices							
24AA128	1.7-5.5V	400 kHz (2)	64 bytes	Entire Array	A0, A1, A2(4)	I	P, SN, SM, ST, MS, MF
24LC128	2.5-5.5V	400 kHz				I, E	
24FC128	1.7-5.5V	1 MHz(3)				I	
256 Kb devices							
24AA256	1.7-5.5V	400 kHz (2)	64 bytes	Entire Array	A0, A1, A2(4)	I	P, SN, SM, ST, MS, MF
24LC256	2.5-5.5V	400 kHz				I, E	
24FC256	1.7-5.5V	1 MHz(3)				I	
512 Kb devices							
24AA512	1.7-5.5V	400 kHz (2)	128 bytes	Entire Array	A0, A1, A2	I	P, SM, MF,
24LC512	2.5-5.5V	400 kHz				I, E	
24FC512	1.7-5.5V(3)	1 MHz				I	
1024 Kb devices							
24AA1025	1.7-5.5V	400 kHz (2)	128 bytes	Entire Array	A0, A1	I	P, SM
24LC1025	2.5-5.5V	400 kHz				I, E	
24FC1025	1.7-5.5V(3)	1 MHz				I	

Note 1: 100 kHz for Vcc <4.5V.

2: 100 kHz for Vcc <2.5V.

3: 400 kHz for Vcc <2.5V.

4: Pins A0 and A1 are no-connects for the 24XX128 and 24XX256 in the MSOP package.

5: P = 8-PDIP, SN = 8-SOIC (3.90 mm JEDEC), ST = 8-TSSOP, OT = 5 or 6-SOT23, MC = 2x3mm DFN, MS = 8-MSOP, SM = 8-SOIC (200 mil EIAJ), MF = 5x6mm DFN.

6: Available Q4 2007.

2.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings (†)

VCC.....6.5V

All inputs and outputs w.r.t. VSS ..... -0.6V to VCC +1.0V

Storage temperature .....-65°C to +150°C

Ambient temperature with power applied .....-40°C to +125°C

ESD protection on all pins .....≥ 4 kV

† NOTICE: Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

TABLE 2-1: DC CHARACTERISTICS

DC CHARACTERISTICS			**Electrical Characteristics:** Industrial (I): VCC = +1.7V to 5.5V TA = -40°C to +85°C Automotive (E): VCC = +2.5V to 5.5V TA = -40°C to 125°C			
Param. No.	**Sym.**	**Characteristic**	**Min.**	**Max.**	**Units**	**Conditions**
D1	—	A0, A1, A2, SCL, SDA and WP pins:	—	—	—	—
D2	VIH	High-level input voltage	0.7 VCC	—	V	—
D3	VIL	Low-level input voltage	—	0.3 VCC 0.2 VCC	V V	VCC ≥ 2.5V VCC < 2.5V
D4	VHYS	Hysteresis of Schmitt Trigger inputs (SDA, SCL pins)	0.05 VCC	—	V	**(Note 1)**
D5	VOL	Low-level output voltage	—	0.40	V	IOL = 3.0 mA @ VCC = 2.5V
D6	ILI	Input leakage current	—	±1	µA	VIN = VSS or VCC
D7	ILO	Output leakage current	—	±1	µA	VOUT = VSS or VCC
D8	CIN, COUT	Pin capacitance (all inputs/outputs)	—	10	pF	VCC = 5.0V **(Note 1)** TA = 25°C, FCLK = 1 MHz
D9	ICC Read	Operating current	—	500 400 1	µA µA mA	24XX1025 24XX128, 256, 512: All except 24XX128, 256, 512, 1025: (VCC = 5.5V, SCL = 400 kHz)
	ICC Write		—	3 5	mA mA	All except 24XX512 and 24XX1025 24XX512 and 24XX1025 (VCC = 5.5V)
D10	ICCS	Standby current	— — — —	1 5 50 5	µA µA µA µA	All except 24XX1025 24XX1025 24C01C and 24C02C only (TA = -40°C to +85°C) All except 24XX1025 (TA = -40°C to +125°C) SCL = SDA = VCC = 5.5V A0, A1, A2, WP = VSS or VCC

Note 1: This parameter is periodically sampled and not 100% tested.

TABLE 2-2: AC CHARACTERISTICS – ALL EXCEPT 24XX00, 24C01C AND 24C02C

AC CHARACTERISTICS			Electrical Characteristics: Industrial (I): VCC = +1.7V to 5.5V TA = -40°C to +85°C Automotive (E): VCC = +2.5V to 5.5V TA = -40°C to 125°C			
Param. No.	**Sym.**	**Characteristic**	**Min.**	**Max.**	**Units**	**Conditions**
1	FCLK	Clock frequency	— — — —	100 400 400 1000	kHz	1.7V ≤ VCC < 2.5V 2.5V ≤ VCC ≤ 5.5V 1.7V ≤ VCC < 2.5V 24FCXXX 2.5V ≤ VCC ≤ 5.5V 24FCXXX
2	THIGH	Clock high time	4000 600 600 500	— — — —	ns	1.7V ≤ VCC < 2.5V 2.5V ≤ VCC ≤ 5.5V 1.7V ≤ VCC < 2.5V 24FCXXX 2.5V ≤ VCC ≤ 5.5V 24FCXXX
3	TLOW	Clock low time	4700 1300 1300 500	— — — —	ns	1.7V ≤ VCC < 2.5V 2.5V ≤ VCC ≤ 5.5V 1.7V ≤ VCC < 2.5V 24FCXXX 2.5V ≤ VCC ≤ 5.5V 24FCXXX
4	TR	SDA and SCL rise time **(Note 1)**	— — —	1000 300 300	ns	1.7V ≤ VCC < 2.5V 2.5V ≤ VCC ≤ 5.5V 1.7V ≤ VCC ≤ 5.5V 24FCXXX
5	TF	SDA and SCL fall time **(Note 1)**	— —	300 100	ns	All except 24FCXXX 1.7V ≤ VCC ≤ 5.5V 24FCXXX
6	THD:STA	Start condition hold time	4000 600 600 250	— — — —	ns	1.7V ≤ VCC < 2.5V 2.5V ≤ VCC ≤ 5.5V 1.7V ≤ VCC < 2.5V 24FCXXX 2.5V ≤ VCC ≤ 5.5V 24FCXXX
7	TSU:STA	Start condition setup time	4700 600 600 250	— — — —	ns	1.7V ≤ VCC < 2.5V 2.5V ≤ VCC ≤ 5.5V 1.7V ≤ VCC < 2.5V 24FCXXX 2.5V ≤ VCC ≤ 5.5V 24FCXXX
8	THD:DAT	Data input hold time	0	—	ns	**(Note 2)**
9	TSU:DAT	Data input setup time	250 100 100	— — —	ns	1.7V ≤ VCC < 2.5V 2.5V ≤ VCC ≤ 5.5V 1.7V ≤ VCC ≤ 5.5V 24FCXXX
10	TSU:STO	Stop condition setup time	4000 600 600 250	— — — —	ns	1.7 V ≤ VCC < 2.5V 2.5 V ≤ VCC ≤ 5.5V 1.7V ≤ VCC < 2.5V 24FCXXX 2.5 V ≤ VCC ≤ 5.5V 24FCXXX
11	TSU:WP	WP setup time (32K and above only)	4000 600 600	— — —	ns	1.7V ≤ VCC < 2.5V 2.5V ≤ VCC ≤ 5.5V 1.7V ≤ VCC ≤ 5.5V 24FCXXX
12	THD:WP	WP hold time (32K and above only)	4700 1300 1300	— — —	ns	1.7V ≤ VCC < 2.5V 2.5V ≤ VCC ≤ 5.5V 1.7V ≤ VCC ≤ 5.5V 24FCXXX

Note 1: Not 100% tested. CB = total capacitance of one bus line in pF.

2: As a transmitter, the device must provide an internal minimum delay time to bridge the undefined region (minimum 300 ns) of the falling edge of SCL to avoid unintended generation of Start or Stop conditions.

3: This parameter is not tested but ensured by characterization. For endurance estimates in a specific application, please consult the Total Endurance™ Model, which can be obtained from Microchip's web site: www.microchip.com.

4: 24FCXXX denotes the 24FC64, 24FC128, 24FC256, 24FC512 and 24FC1025 devices.

TABLE 2-2: AC CHARACTERISTICS – ALL EXCEPT 24XX00, 24C01C AND 24C02C (CONTINUED)

AC CHARACTERISTICS			Electrical Characteristics: Industrial (I): VCC = +1.7V to 5.5V TA = -40°C to +85°C Automotive (E): VCC = +2.5V to 5.5V TA = -40°C to 125°C			
Param. No.	**Sym.**	**Characteristic**	**Min.**	**Max.**	**Units**	**Conditions**
13	TAA	Output valid from clock **(Note 2)**	— — — —	3500 900 900 400	ns	1.7V ≤ VCC < 2.5V 2.5V ≤ VCC ≤ 5.5V 1.7V ≤ VCC < 2.5V 24FCXXX 2.5V ≤ VCC ≤ 5.5V 24FCXXX
14	TBUF	Bus free time: Time the bus must be free before a new transmission can start	4700 1300 1300 500	— — — —	ns	1.7V ≤ VCC < 2.5V 2.5V ≤ VCC ≤ 5.5V 1.7V ≤ VCC < 2.5V 24FCXXX 2.5V ≤ VCC ≤ 5.5V 24FCXXX
15	TOF	Output fall time from VIH minimum to VIL maximum CB ≤ 100 pF	10 + 0.1CB	250 250	ns	All except 24FCXXX **(Note 1)** 24FCXXX **(Note 1)**
16	TSP	Input filter spike suppression (SDA and SCL pins)	—	50	ns	All except 24FCXXX **(Note 1)**
17	TWC	Write cycle time (byte or page)	—	5	ms	
18	—	Endurance	1,000,000	—	cycles	25°C **(Note 3)**

Note 1: Not 100% tested. CB = total capacitance of one bus line in pF.

2: As a transmitter, the device must provide an internal minimum delay time to bridge the undefined region (minimum 300 ns) of the falling edge of SCL to avoid unintended generation of Start or Stop conditions.

3: This parameter is not tested but ensured by characterization. For endurance estimates in a specific application, please consult the Total Endurance™ Model, which can be obtained from Microchip's web site: www.microchip.com.

4: 24FCXXX denotes the 24FC64, 24FC128, 24FC256, 24FC512 and 24FC1025 devices.

TABLE 2-3: AC CHARACTERISTICS – 24XX00, 24C01C AND 24C02C

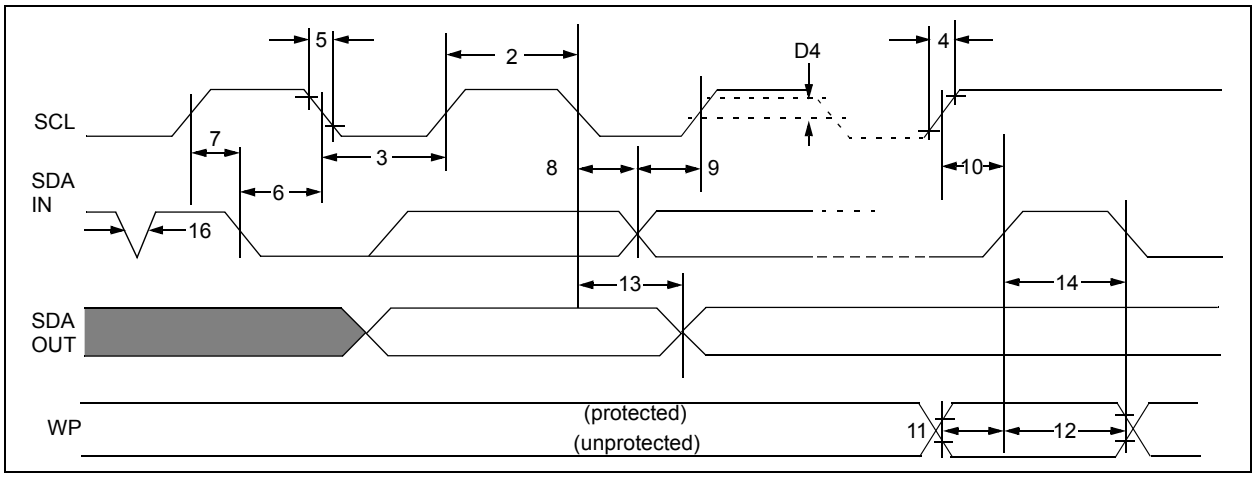
All Parameters apply across all recommended operating ranges unless otherwise noted	Industrial (I): T_A = -40°C to +85°C, V_{CC} = 1.7V to 5.5V Automotive (E): T_A = -40°C to +125°C, V_{CC} = 4.5V to 5.5V				
Parameter	**Symbol**	**Min.**	**Max.**	**Units**	**Conditions**
Clock frequency	F_{CLK}	— — —	100 100 400	kHz	4.5V ≤ Vcc ≤ 5.5V (E Temp range) 1.7V ≤ Vcc ≤ 4.5V 4.5V ≤ Vcc ≤ 5.5V
Clock high time	T_{HIGH}	4000 4000 600	— — —	ns	4.5V ≤ Vcc ≤ 5.5V (E Temp range) 1.7V ≤ Vcc ≤ 4.5V 4.5V ≤ Vcc ≤ 5.5V
Clock low time	T_{LOW}	4700 4700 1300	— — —	ns	4.5V ≤ Vcc ≤ 5.5V (E Temp range) 1.7V ≤ Vcc ≤ 4.5V 4.5V ≤ Vcc ≤ 5.5V
SDA and SCL rise time **(Note 1)**	T_R	— — —	1000 1000 300	ns	4.5V ≤ Vcc ≤ 5.5V (E Temp range) 1.7V ≤ Vcc ≤ 4.5V 4.5V ≤ Vcc ≤ 5.5V
SDA and SCL fall time	T_F	—	300	ns	**(Note 1)**
Start condition hold time	$T_{HD:STA}$	4000 4000 600	— — —	ns	4.5V ≤ Vcc ≤ 5.5V (E Temp range) 1.7V ≤ Vcc ≤ 4.5V 4.5V ≤ Vcc ≤ 5.5V
Start condition setup time	$T_{SU:STA}$	4700 4700 600	— — —	ns	4.5V ≤ Vcc ≤ 5.5V (E Temp range) 1.7V ≤ Vcc ≤ 4.5V 4.5V ≤ Vcc ≤ 5.5V
Data input hold time	$T_{HD:DAT}$	0	—	ns	**(Note 2)**
Data input setup time	$T_{SU:DAT}$	250 250 100	— — —	ns	4.5V ≤ Vcc ≤ 5.5V (E Temp range) 1.7V ≤ Vcc ≤ 4.5V 4.5V ≤ Vcc ≤ 5.5V
Stop condition setup time	$T_{SU:STO}$	4000 4000 600	— — —	ns	4.5V ≤ Vcc ≤ 5.5V (E Temp range) 1.7V ≤ Vcc ≤ 4.5V 4.5V ≤ Vcc ≤ 5.5V
Output valid from clock **(Note 2)**	T_{AA}	— — —	3500 3500 900	ns	4.5V ≤ Vcc ≤ 5.5V (E Temp range) 1.7V ≤ Vcc ≤ 4.5V 4.5V ≤ Vcc ≤ 5.5V
Bus free time: Time the bus must be free before a new transmission can start	T_{BUF}	4700 4700 1300	— — —	ns	4.5V ≤ Vcc ≤ 5.5V (E Temp range) 1.7V ≤ Vcc ≤ 4.5V 4.5V ≤ Vcc ≤ 5.5V
Output fall time from V_{IH} minimum to V_{IL} maximum	T_{OF}	20+0.1 CB	250	ns	**(Note 1)**, CB ≤ 100 pF
Input filter spike suppression (SDA and SCL pins)	T_{SP}	—	50	ns	**(Note 1)**
Write cycle time	T_{WC}	—	4 1.5	ms	24XX00 24C01C, 24C02C
Endurance		1,000,000	—	cycles	**(Note 3)**

Note 1: Not 100% tested. C_B = total capacitance of one bus line in pF.

2: As a transmitter, the device must provide an internal minimum delay time to bridge the undefined region (minimum 300 ns) of the falling edge of SCL to avoid unintended generation of Start or Stop conditions.

3: This parameter is not tested but ensured by characterization. For endurance estimates in a specific application, please consult the Total Endurance™ Model which can be obtained from Microchip's web site: www.microchip.com.

FIGURE 2-1: EXAMPLE BUS TIMING DATA



3.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 3-1.

TABLE 3-1: PIN FUNCTION TABLE

Pin Name	8-Pin PDIP and SOIC	8-Pin TSSOP and MSOP	5-Pin SOT-23 24XX00	5-Pin SOT-23 All except 24XX00	8-Pin 5x6 DFN and 2x3 DFN	Function
A0	1	1(1)	—	—	1	User configurable Chip Select(3)(4)
A1	2	2(1)	—	—	2	User configurable Chip Select(3)(4)
A2	3	3	—	—	3	User configurable Chip Select(3)(4)
VSS	4	4	2	2	4	Ground
SDA	5	5	3	3	5	Serial Data
SCL	6	6	1	1	6	Serial Clock
(NC)	—	—	4	—	—	Not Connected
WP	7(2)	7(2)	—	5	7	Write-Protect Input
VCC	8	8	5	4	8	Power Supply

Note 1: Pins 1 and 2 are not connected for the 24XX128 and 24XX256 MSOP packages.
2: Pin 7 is not used for 24XX00, 24XX025 and 24C01C.
3: Pins A0, A1 and A2 are not used by some devices (no internal connections). See Table 1-1 for details.
4: Pin A2 should be tied to a Logic High in the 24XX1025 for proper operation.

3.1 A0, A1, A2 Chip Address Inputs

The A0, A1 and A2 pins are not used by the 24XX01 through 24XX16 devices.

The A0, A1 and A2 inputs are used by the 24C01C, 24C02C, 24XX014, 24XX024, 24XX025 and the 24XX32 through 24XX1025 for multiple device operations. The levels on these inputs are compared with the corresponding bits in the slave address. The chip is selected if the compare is true.

For the 24XX128 and 24XX256 in the MSOP package only, pins A0 and A1 are not connected.

Up to eight devices (two for the 24XX128 and 24XX256 MSOP package) may be connected to the same bus by using different Chip Select bit combinations.

In most applications, the chip address inputs A0, A1 and A2 are hard-wired to logic '0' or logic '1'. For applications in which these pins are controlled by a microcontroller or other programmable device, the chip address pins must be driven to logic '0' or logic '1' before normal device operation can proceed.

Note:	In the 24XX1025, the A2 pin is not configurable, it must be tied to VCC in order for this device to operate properly.

3.2 Serial Data (SDA)

This is a bidirectional pin used to transfer addresses and data into and out of the device. It is an open drain terminal. Therefore, the SDA bus requires a pull-up resistor to VCC (typical 10 kΩ for 100 kHz, 2 kΩ for 400 kHz and 1 MHz).

For normal data transfer, SDA is allowed to change only during SCL low. Changes during SCL high are reserved for indicating the Start and Stop conditions.

3.3 Serial Clock (SCL)

This input is used to synchronize the data transfer to and from the device.

3.4 Write-Protect (WP)

This pin must be connected to either VSS or VCC. If tied to VSS, write operations are enabled. If tied to VCC, write operations are inhibited but read operations are not affected. See Table 1-1 for the write-protect scheme of each device.

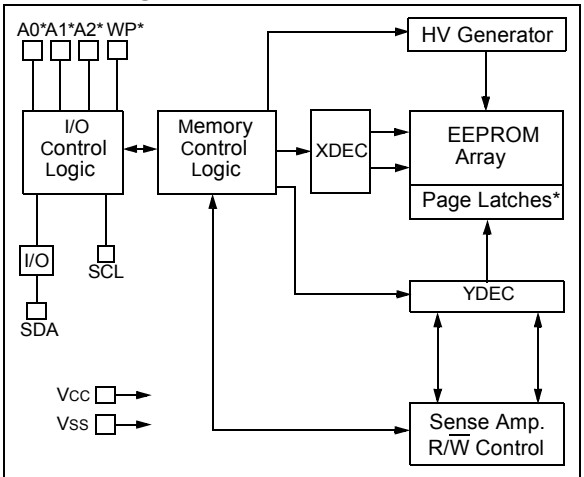
3.5 Power Supply (VCC)

A VCC threshold detect circuit is employed which disables the internal erase/write logic if VCC is below 1.5V at nominal conditions. For the 24C00, 24C01C and 24C02C devices, the erase/write logic is disabled below 3.8V at nominal conditions.

4.0 FUNCTIONAL DESCRIPTION

Each 24XX device supports a bidirectional, 2-wire bus and data transmission protocol. A device that sends data onto the bus is defined as a transmitter, while a device receiving data is defined as a receiver. The bus has to be controlled by a master device which generates the Serial Clock (SCL), controls the bus access and generates the Start and Stop conditions, while the 24XX works as slave. Both master and slave can operate as transmitter or receiver, but the master device determines which mode is activated.

Block Diagram



* A0, A1, A2, WP and page latches are not used by some devices.

See Table 1-1, Device Selection Table, for details.

5.0 BUS CHARACTERISTICS

The following **bus protocol** has been defined:

- Data transfer may be initiated only when the bus is not busy.
- During data transfer, the data line must remain stable whenever the clock line is high. Changes in the data line while the clock line is high will be interpreted as a Start or Stop condition.

Accordingly, the following bus conditions have been defined (Figure 5-1).

5.1 Bus Not Busy (A)

Both data and clock lines remain high.

5.2 Start Data Transfer (B)

A high-to-low transition of the SDA line while the clock (SCL) is high determines a Start condition. All commands must be preceded by a Start condition.

5.3 Stop Data Transfer (C)

A low-to-high transition of the SDA line while the clock (SCL) is high determines a Stop condition. All operations must be ended with a Stop condition.

5.4 Data Valid (D)

The state of the data line represents valid data when, after a Start condition, the data line is stable for the duration of the high period of the clock signal.

The data on the line must be changed during the low period of the clock signal. There is one clock pulse per bit of data.

Each data transfer is initiated with a Start condition and terminated with a Stop condition. The number of data bytes transferred between Start and Stop conditions is determined by the master device.

5.5 Acknowledge

Each receiving device, when addressed, is obliged to generate an acknowledge after the reception of each byte. The master device must generate an extra clock pulse which is associated with this Acknowledge bit.

Note:	During a write cycle, the 24XX will not acknowledge commands.

The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable low during the high period of the acknowledge related clock pulse. Of course, setup and hold times must be taken into account. During reads, a master must signal an end-of-data to the slave by not generating an Acknowledge bit on the last byte that has been clocked out of the slave. In this case, the slave (24XX) will leave the data line high to enable the master to generate the Stop condition (Figure 5-2).

FIGURE 5-1: DATA TRANSFER SEQUENCE ON THE SERIAL BUS

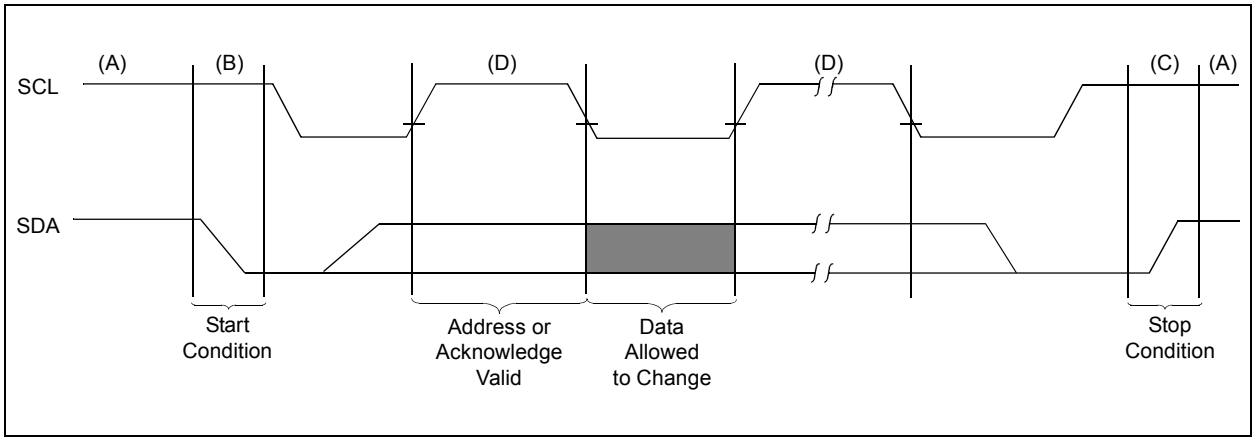
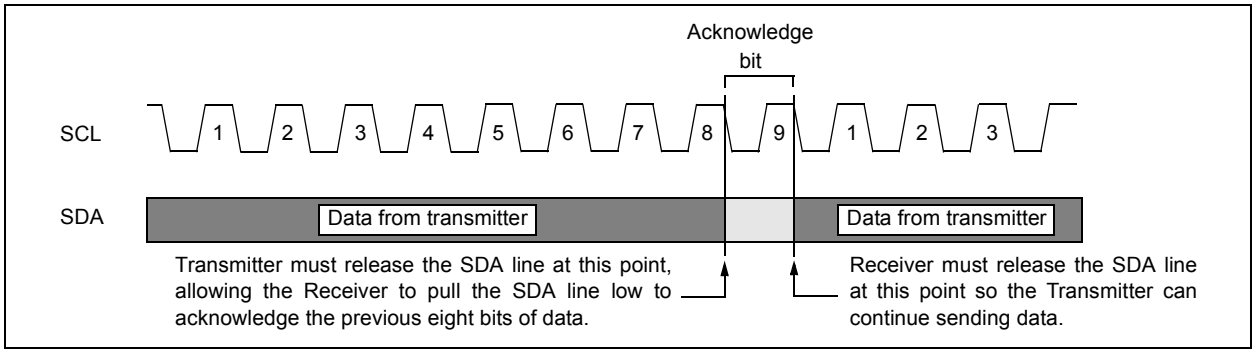


FIGURE 5-2: ACKNOWLEDGE TIMING

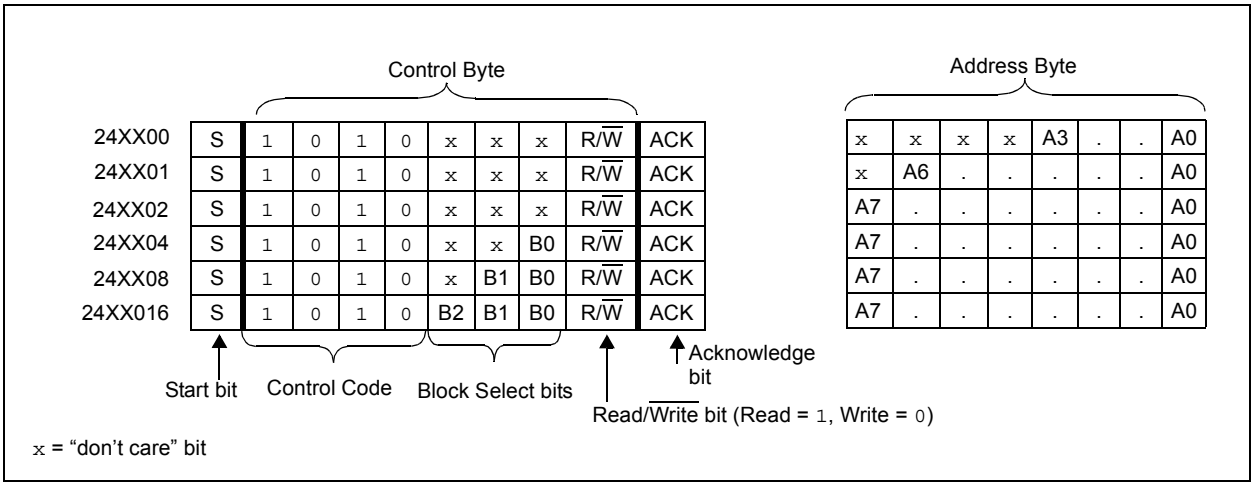


5.6 Device Addressing For Devices Without Functional Address Pins

A control byte is the first byte received following the Start condition from the master device (Figure 5-3). The control byte begins with a four-bit control code. For the 24XX, this is set as '1010' binary for read and write operations. The next three bits of the control byte are the block-select bits (B2, B1, B0). They are used by the master device to select which of the 256-word blocks of memory are to be accessed. These bits are in effect the three Most Significant bits of the word address. Note that B2, B1 and B0 are "don't care" for the 24XX00, the 24XX01 and 24XX02. B2 and B1 are "don't care" for the 24XX04. B2 is "don't care" for the 24XX08.

The last bit of the control byte defines the operation to be performed. When set to '1', a read operation is selected. When set to '0' a write operation is selected. Following the Start condition, the 24XX monitors the SDA bus. Upon receiving a '1010' code, the block select bits and the R/$\overline{W}$ bit, the slave device outputs an Acknowledge signal on the SDA line. The address byte follows the acknowledge.

FIGURE 5-3: CONTROL AND ADDRESS BYTE ASSIGNMENTS FOR DEVICES WITHOUT ADDRESS PINS



5.7 Device Addressing For Devices With Functional Address Pins

A control byte is the first byte received following the Start condition from the master device (Figure 5-4). The control byte begins with a 4-bit control code. For the 24XX, this is set as '1010' binary for read and write operations. The next three bits of the control byte are the Chip Select bits (A2, A1, A0). The Chip Select bits allow the use of up to eight 24XX devices on the same bus and are used to select which device is accessed. The Chip Select bits in the control byte must correspond to the logic levels on the corresponding A2, A1 and A0 pins for the device to respond. These bits are, in effect, the three Most Significant bits of the word address.

For 24XX128 and 24XX256 in the MSOP package, the A0 and A1 pins are not connected. During device addressing, the A0 and A1 Chip Select bits (Figure 5-4) should be set to '0'. Only two 24XX128 or 24XX256 MSOP packages can be connected to the same bus.

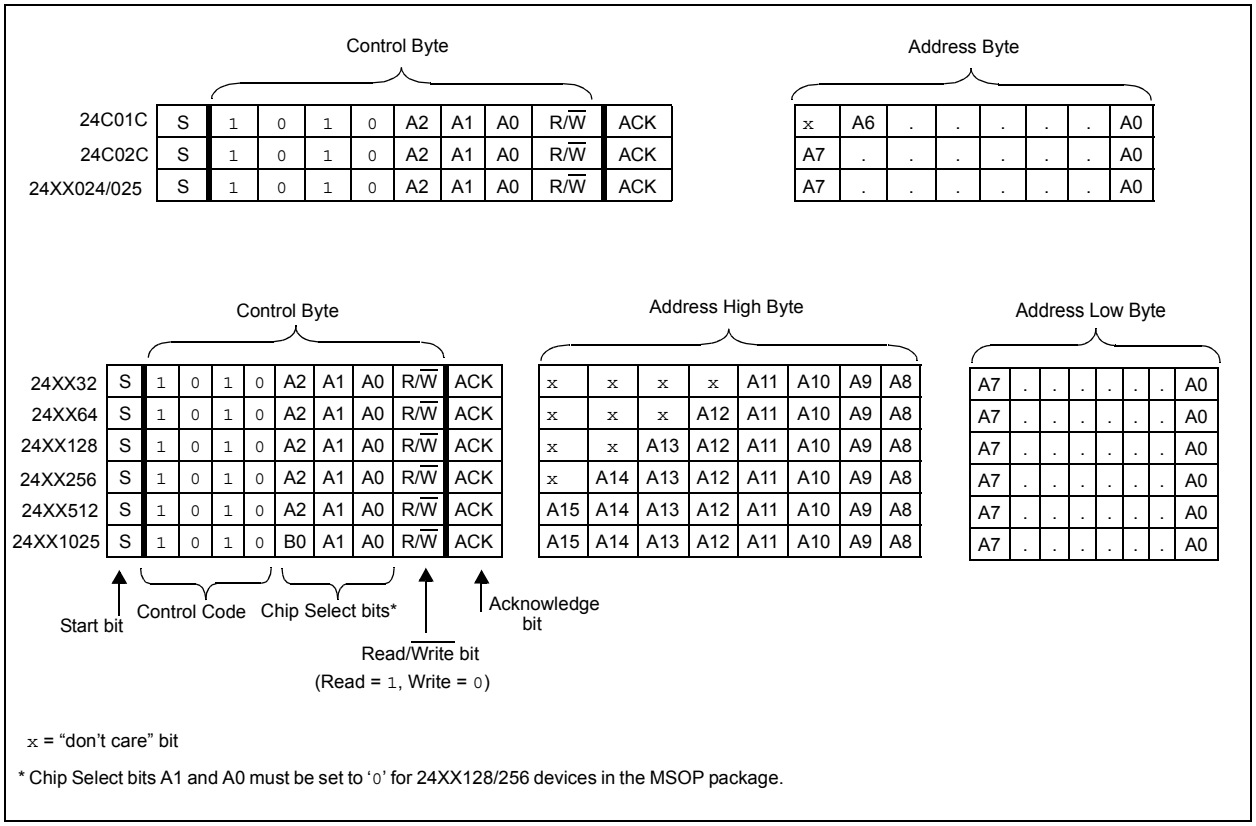
The last bit of the control byte defines the operation to be performed. When set to a '1', a read operation is selected. When set to a '0', a write operation is selected.

For higher density devices (24XX32 through 24XX1025), the next two bytes received define the address of the first data byte. Depending on the product density, not all bits in the address high byte are used. A15, A14, A13 and A12 are "don't care" for 24XX32. A15, A14 and A13 are "don't care" for 24XX64. A15 and A14 are "don't care" for 24XX128. A15 is "don't care" for 24XX256. All address bits are used for the 24XX512 and 24XX1025. The upper address bits are transferred first, followed by the Less Significant bits.

Following the Start condition, the 24XX monitors the SDA bus. Upon receiving a '1010' code, appropriate device select bits and the R/$\overline{W}$ bit, the slave device outputs an Acknowledge signal on the SDA line. The address byte(s) follow the acknowledge.

The 24XX1025 has an internal address boundary limitation that is divided into two segments of 512 Kbits. Block select bit 'B0' is used to control access to each segment. Contiguous writes cannot be performed across this boundary.

FIGURE 5-4: CONTROL AND ADDRESS BYTE ASSIGNMENTS FOR DEVICES WITH ADDRESS PINS



x = "don't care" bit

* Chip Select bits A1 and A0 must be set to '0' for 24XX128/256 devices in the MSOP package.

5.7.1 CONTIGUOUS ADDRESSING ACROSS MULTIPLE DEVICES

Chip Select bits A2, A1 and A0 can be used to expand the contiguous address space by adding up to eight 24XXs on the same bus. Software can use the three address bits of the control byte as the three Most Significant bits of the address byte. For example, in the 24XX32 devices, software can use A0 of the **control byte** as address bit A12; A1 as address bit A13; and A2 as address bit A14 (Table 5-1). It is not possible to sequentially read across device boundaries.

TABLE 5-1: CONTROL BYTE ADDRESS BITS

	Maximum Devices	Maximum Contiguous Address Space	Chip Select Bit A2	Chip Select Bit A1	Chip Select Bit A0
1K (24C01C)	8	8 Kb	A10	A9	A8
1K (24XX014)	8	8 Kb	A10	A9	A8
2K (24C02C)	8	16 Kb	A10	A9	A8
2K (24XX024/025)	8	16 Kb	A10	A9	A8
32K (24XX32)	8	256 Kb	A14	A13	A12
64K (24XX64)	8	512 Kb	A15	A14	A13
128K (24XX128)	8(1)	1 Mb	A16*	A15*	A14
256K (24XX256)	8(1)	2 Mb	A17*	A16*	A15
512K (24XX512)	8	4 Mb	A18	A17	A16
1024K (24XX1025)	4(2)	4 Mb	B0(3)	A17	A16

Note 1: Up to two 24XX128 or 24XX256 devices in the MSOP package can be added for up to 256 kb or 512 kb of address space, respectively. Bits A0 and A1 must be set to '0'.

2: Using the block select bit 'B0', up to four 24XX1025 devices can be cascaded together.

3: For proper operation of the 24XX1025 the A2 pin must be tied to a logic high. Software addressing uses B0 to select between upper and lower 512 Kbit segments of memory.

6.0 WRITE OPERATIONS

6.1 Byte Write

A byte write operation begins with a Start condition from the master followed by the four-bit control code (see Figure 6-1 and Figure 6-2). The next 3 bits are either the Block Address bits (for devices without address pins) or the Chip Select bits (for devices with address pins). Then the master transmitter clocks the R/$\overline{W}$ bit (which is a logic low) onto the bus. The slave then generates an Acknowledge bit during the ninth clock cycle.

The next byte transmitted by the master is the address byte (for 128-bit to 16 Kbit devices) or the high-order address byte (for 32-1024 Kbit devices). For 32 through 1024 Kbit devices, the high-order address byte is followed by the low-order address byte. In either case, each address byte is acknowledged by the 24XX and the address bits are latched into the internal address counter of the 24XX.

For the 24XX00 devices, only the lower four address bits are used by the device. The upper four bits are “don’t cares.”

After receiving the ACK from the 24XX acknowledging the final address byte, the master device transmits the data word to be written into the addressed memory location. The 24XX acknowledges again and the master generates a Stop condition, which initiates the internal write cycle.

If an attempt is made to write to an array with the WP pin held high, the device will acknowledge the command, but no write cycle will occur, no data will be written, and the device will immediately accept a new command. After a byte Write command, the internal address counter will increment to the next address location. During a write cycle, the 24XX will not acknowledge commands.

FIGURE 6-1: BYTE WRITE: 128-BIT TO 16 KBIT DEVICES

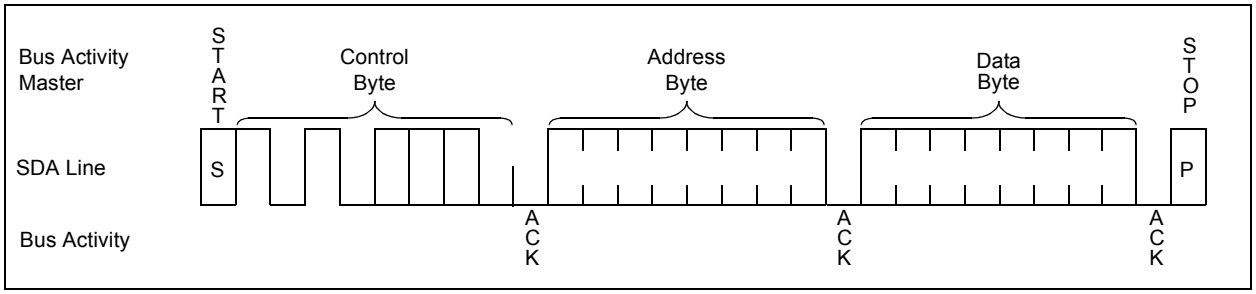
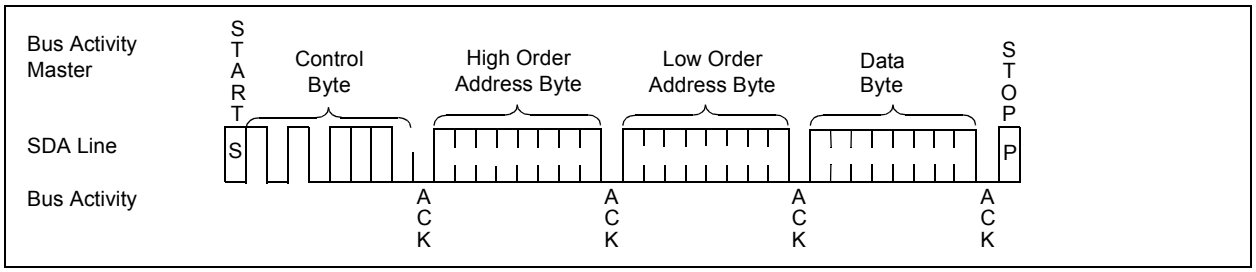


FIGURE 6-2: BYTE WRITE: 32 TO 1024 KBIT DEVICES



6.2 Page Write

The write control byte, word address byte(s), and the first data byte are transmitted to the 24XX in much the same way as in a byte write (see Figure 6-3 and Figure 6-4). The exception is that instead of generating a Stop condition, the master transmits up to one page of bytes(1), which is temporarily stored in the on-chip page buffer. This data is then written into memory once the master has transmitted a Stop condition. Upon receipt of each word, the internal address counter is incremented by one. If the master should transmit more than one page of data prior to generating the Stop condition, the address counter will roll over and the previously received data will be overwritten. As with the byte write operation, once the Stop condition is received, an internal write cycle begins. During the write cycle, the 24XX will not acknowledge commands.

Page writes can be any number of bytes within a page (up to the page size), starting at any address. Only the data bytes being addressed will be changed within the page.

If an attempt is made to write to the array with the WP pin held high, the device will acknowledge the command, but no write cycle will occur, no data will be written and the device will immediately accept a new command.

Note 1: See Device Selection Table 1-1 for the page size of each device.

6.3 Write-Protection

The WP pin allows the user to write-protect the array when the pin is tied to VCC. See Device Selection Table 1-1 for the write-protect scheme of each device. If tied to VSS, the write protection is disabled. Please refer to the product data sheet for complete details.

Note: Page write operations are limited to writing bytes within a single physical page, **regardless** of the number of bytes actually being written. Physical page boundaries start at addresses that are integer multiples of the page buffer size (or 'page size') and end at addresses that are integer multiples of [page size – 1]. If a Page Write command attempts to write across a physical page boundary, the result is that the data wraps around to the beginning of the current page (overwriting data previously stored there), instead of being written to the next page, as might be expected. It is therefore necessary for the application software to prevent page write operations that would attempt to cross a page boundary.

FIGURE 6-3: PAGE WRITE: 1 KB TO 16 KBIT DEVICES

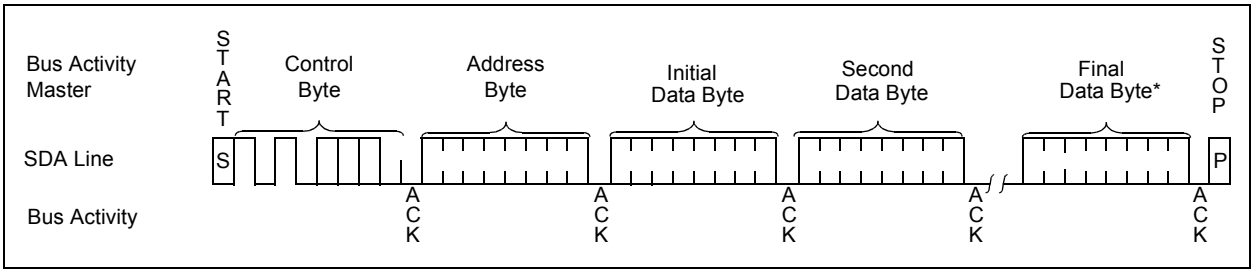
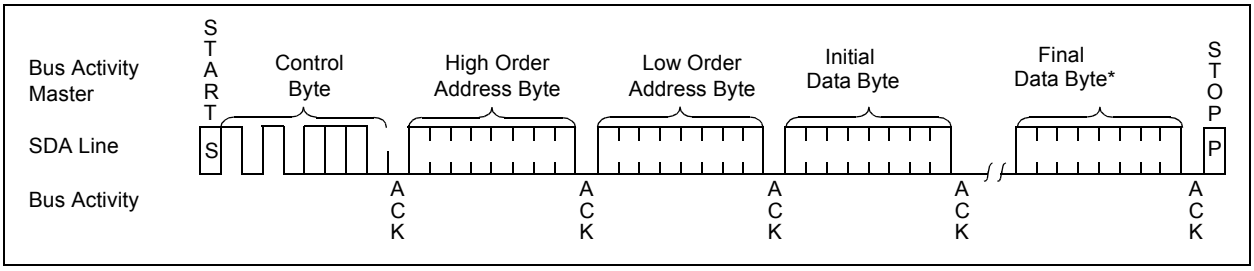


FIGURE 6-4: PAGE WRITE: 32 TO 1024 KBIT DEVICES

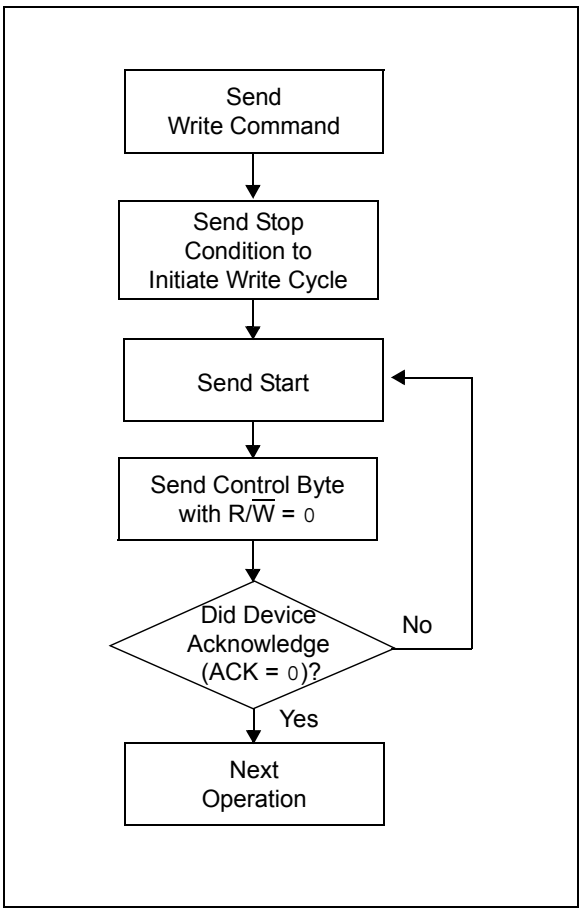


* See Table 1-1 for maximum number of data bytes in a page.

7.0 ACKNOWLEDGE POLLING

Since the device will not acknowledge commands during a write cycle, this can be used to determine when the cycle is complete (This feature can be used to maximize bus throughput). Once the Stop condition for a Write command has been issued from the master, the device initiates the internally timed write cycle. ACK polling can be initiated immediately. This involves the master sending a Start condition, followed by the control byte for a Write command (R/$\overline{W}$ = 0). If the device is still busy with the write cycle, then no ACK will be returned. If no ACK is returned, the Start bit and control byte must be re-sent. If the cycle is complete, then the device will return the ACK and the master can then proceed with the next Read or Write command. See Figure 7-1 for flow diagram.

FIGURE 7-1: ACKNOWLEDGE POLLING FLOW



8.0 READ OPERATION

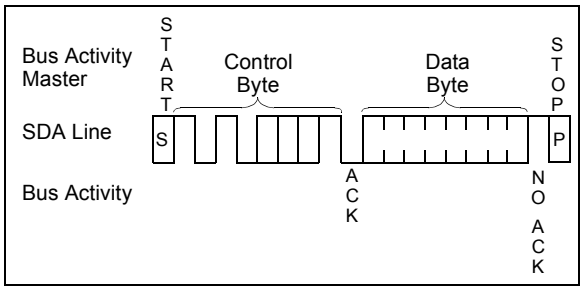
Read operations are initiated in much the same way as write operations with the exception that the R/$\overline{W}$ bit of the control byte is set to '1'. There are three basic types of read operations: current address read, random read and sequential read.

8.1 Current Address Read

The 24XX contains an address counter that maintains the address of the last byte accessed, internally incremented by '1'. Therefore, if the previous read or write operation was to address 'n' (n is any legal address), the next current address read operation would access data from address n + 1.

Upon receipt of the control byte with R/$\overline{W}$ bit set to '1', the 24XX issues an acknowledge and transmits the 8-bit data byte. The master will not acknowledge the transfer, but does generate a Stop condition and the 24XX discontinues transmission (Figure 8-1).

FIGURE 8-1: CURRENT ADDRESS READ



8.2 Random Read

Random read operations allow the master to access any memory location in a random manner. To perform this type of read operation, the byte address must first be set. This is done by sending the byte address to the 24XX as part of a write operation (R/$\overline{W}$ bit set to '0'). Once the byte address is sent, the master generates a Start condition following the acknowledge. This terminates the write operation, but not before the internal address counter is set. The master then issues the control byte again, but with the R/$\overline{W}$ bit set to a '1'. The 24XX will then issue an acknowledge and transmit the 8-bit data byte. The master will not acknowledge the transfer but does generate a Stop condition, which causes the 24XX to discontinue transmission (Figure 8-2 and Figure 8-3). After a random Read command, the internal address counter will increment to the next address location.

FIGURE 8-2: RANDOM READ: 128-BIT TO 16 KBIT DEVICES

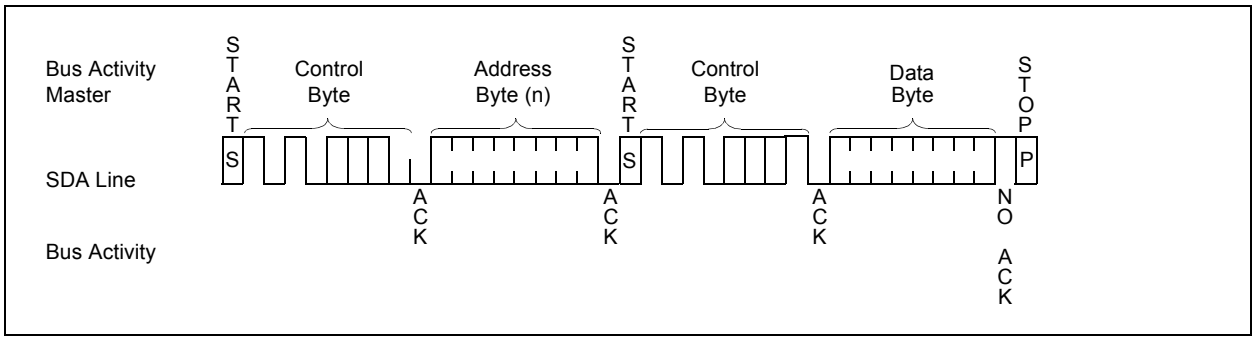
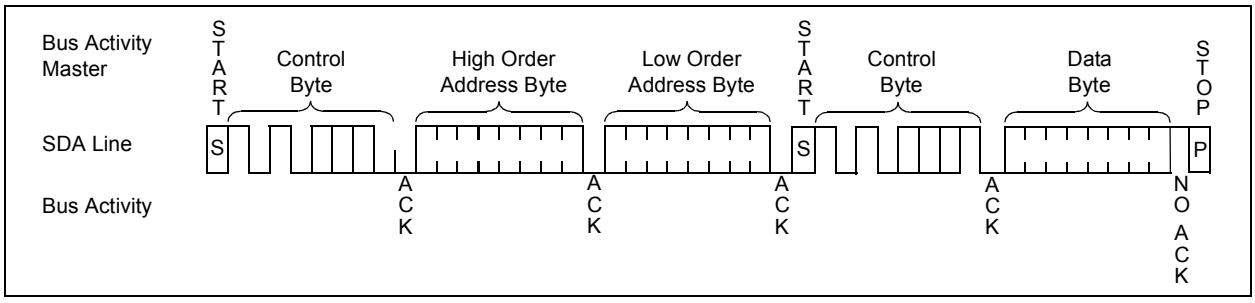


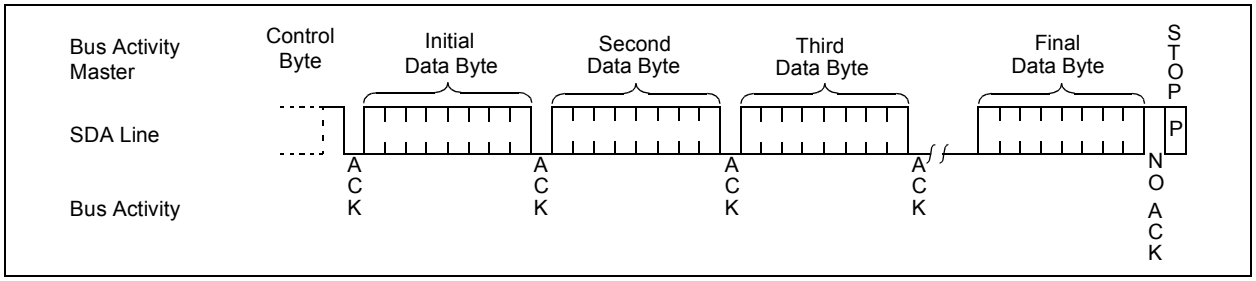
FIGURE 8-3: RANDOM READ: 32 TO 1024 KBIT DEVICES



8.3 Sequential Read

Sequential reads are initiated in the same way as a random read except that after the 24XX transmits the first data byte, the master issues an acknowledge as opposed to the Stop condition used in a random read. This acknowledge directs the 24XX to transmit the next sequentially addressed data byte (Figure 8-4). Following the final byte transmitted to the master, the master will NOT generate an acknowledge but will generate a Stop condition. To provide sequential reads, the 24XX contains an internal Address Pointer which is incremented by one at the completion of each operation. This Address Pointer allows the entire memory contents to be serially read during one operation. If the last address byte in the array is acknowledged, the Address Pointer will roll over to address 0x00.

FIGURE 8-4: SEQUENTIAL READ



APPENDIX A: REVISION HISTORY

Revision A

Original release of document. Combined Serial EEPROM 24XXX device data sheets.

Revision B (02/2007)

Change 1.8V to 1.7V; Removed 14-Lead TSSOP Package; Replaced Package Drawings; Revised Product ID Section. Updates throughout.

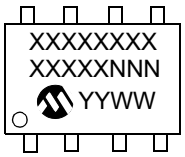
Revision C (07/2007)

Added 24AA1025/LC1025/FC1025 part; Updates throughout; Replaced Package Drawings (Rev. AP).

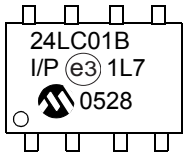
9.0 PACKAGING INFORMATION

9.1 Package Marking Information

8-Lead PDIP



Example:



8-Lead PDIP Package Marking							
Device	**Line 1 Marking**	**Device**	**Line 1 Marking**	**Device**	**Line 1 Marking**	**Device**	**Line 1 Marking**
24AA00	24AA00	24LC00	24LC00	24C00	24C00		
24AA01	24AA01	24LC01B	24LC01B				
24AA014	24AA014	24LC014	24LC014				
				24C01C	24C01C		
24AA02	24AA02	24LC02B	24LC02B				
24AA024	24AA024	24LC024	24LC024				
24AA025	24AA025	24LC025	24LC025				
				24C02C	24C02C		
24AA04	24AA04	24LC04B	24LC04B				
24AA08	24AA08	24LC08B	24LC08B				
24AA16	24AA16	24LC16B	24LC16B				
24AA32A	24AA32A	24LC32A	24LC32A				
24AA64	24AA64	24LC64	24LC64			24FC64	24FC64
24AA128	24AA128	24LC128	24LC128			24FC128	24FC128
24AA256	24AA256	24LC256	24LC256			24FC256	24FC256
24AA512	24AA512	24LC512	24LC512			24FC512	24FC512
24AA1025	24AA1025	24LC1025	24LC1025			24FC1025	24FC1025

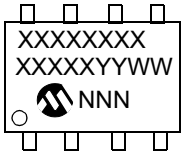
Legend:	XX...X	Part number or part number code
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code (2 characters for small packages)
	(e3)	Pb-free JEDEC designator for Matte Tin (Sn) plated devices

Note: For very small packages with no room for the Pb-free JEDEC designator (e3), the marking will only appear on the outer carton or reel label.

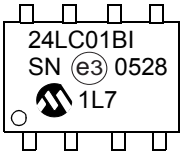
Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

Note: Please visit www.microchip.com/Pbfree for the latest information on Pb-free conversion.

8-Lead SOIC



Example:



8-Lead SOIC Package Marking							
Device	**Line 1 Marking**	**Device**	**Line 1 Marking**	**Device**	**Line 1 Marking**	**Device**	**Line 1 Marking**
24AA00	24AA00T	24LC00	24LC00T	24C00	24C00T		
24AA01	24AA01T	24LC01B	24LC01BT				
24AA014	24AA014T	24LC014	24LC014T				
				24C01C	24C01CT		
24AA02	24AA02T	24LC02B	24LC02BT				
24AA024	24AA024T	24LC024	24LC024T				
24AA025	24AA025T	24LC025	24LC025T				
				24C02C	24C02CT		
24AA04	24AA04T	24LC04B	24LC04BT				
24AA08	24AA08T	24LC08B	24LC08BT				
24AA16	24AA16T	24LC16B	24LC16BT				
24AA32A	24AA32AT	24LC32A	24LC32AT				
24AA64	24AA64T	24LC64	24LC64T			24FC64	24FC64T
24AA128	24AA128T	24LC128	24LC128T			24FC128	24FC128T
24AA256	24AA256T	24LC256	24LC256T			24FC256	24FC256T
24AA512	24AA512T	24LC512	24LC512T			24FC512	24FC512T
24AA1025	24AA1025	24LC1025	24LC1025			24FC1025	24FC1025

Note: T = Temperature range: I = Industrial, E = Extended

Legend:		
	XX...X	Part number or part number code
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code (2 characters for small packages)
	e3	Pb-free JEDEC designator for Matte Tin (Sn) plated devices

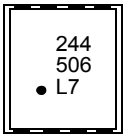
Note: For very small packages with no room for the Pb-free JEDEC designator e3, the marking will only appear on the outer carton or reel label.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

Note: Please visit www.microchip.com/Pbfree for the latest information on Pb-free conversion.

8-Lead 2x3 DFN

Example:



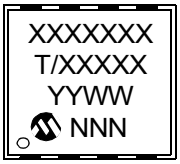
8-Lead 2x3mm DFN Package Marking							
Device	**Industrial Line 1 Marking**	**Device**	**Industrial Line 1 Marking**	**E-Temp Line 1 Marking**	**Device**	**Industrial Line 1 Marking**	**E-Temp Line 1 Marking**
24AA00	201	24LC00	204	205	24C00	207	208
24AA01	211	24LC01B	214	215			
24AA014	2N1	24LC014	2N4	2N5			
					24C01C	2N7	2N8
24AA02	221	24LC02B	224	225			
24AA024	2P1	24LC024	2P4	2P5			
24AA025	2R1	24LC025	2R4	2R5			
					24C02C	2P7	2P8
24AA04	231	24LC04B	234	235			
24AA08	241	24LC08B	244	245			
24AA16	251	24LC16B	254	255			
24AA32A	261	24LC32A	264	265			
24AA64	271	24LC64	274	275	24FC64	27A	27B

Legend:	XX...X	Part number or part number code
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code (2 characters for small packages)
	(e3)	Pb-free JEDEC designator for Matte Tin (Sn) plated devices

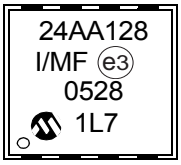
Note: For very small packages with no room for the Pb-free JEDEC designator (e3), the marking will only appear on the outer carton or reel label.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

8-Lead DFN



Example:



8-Lead 5x6mm DFN Package Marking					
Device	**Line 1 Marking**	**Device**	**Line 1 Marking**	**Device**	**Line 1 Marking**
24AA128	24AA128	24LC128	24LC128	24FC128	24FC128
24AA256	24AA256	24LC256	24LC256	24FC256	24FC256
24AA512	24AA512	24LC512	24LC512	24FC512	24FC512

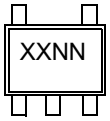
Note: Temperature range (T) listed on second line. I = Industrial, E = Extended

Legend:	XX...X	Part number or part number code
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code (2 characters for small packages)
	(e3)	Pb-free JEDEC designator for Matte Tin (Sn) plated devices

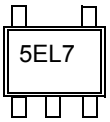
Note: For very small packages with no room for the Pb-free JEDEC designator (e3), the marking will only appear on the outer carton or reel label.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

5-Lead SOT-23



Example:



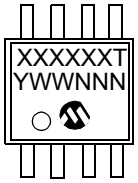
5-Lead SOT-23 Package Marking										
Device	**Comm. Marking**	**Indust. Marking**	**Device**	**Comm. Marking**	**Indust. Marking**	**E-Temp Marking**	**Device**	**Comm. Marking**	**Indust. Marking**	**E-Temp Marking**
24AA00	A0NN	B0NN	24LC00	L0NN	M0NN	N0NN	24C00	C0NN	D0NN	E0NN
24AA01	A1NN	B1NN	24LC01B	L1NN	M1NN	N1NN				
24AA02	A2NN	B2NN	24LC02B	L2NN	M2NN	N2NN				
24AA04	A3NN	B3NN	24LC04B	L3NN	M3NN	N3NN				
24AA08	A4NN	B4NN	24LC08B	L4NN	M4NN	N4NN				
24AA16	A5NN	B5NN	24LC16B	L5NN	M5NN	N5NN				

Legend:	XX...X	Part number or part number code
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code (2 characters for small packages)
	(e3)	Pb-free JEDEC designator for Matte Tin (Sn) plated devices

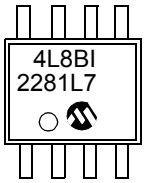
Note: For very small packages with no room for the Pb-free JEDEC designator (e3), the marking will only appear on the outer carton or reel label.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

8-Lead MSOP (150 mil)



Example:



8-Lead MSOP Package Marking							
Device	**Line 1 Marking**	**Device**	**Line 1 Marking**	**Device**	**Line 1 Marking**	**Device**	**Line 1 Marking**
24AA01	4A01T	24LC01B	4L1BT				
24AA014	4A14T	24LC014	4L14T				
				24C01C	4C1CT		
24AA02	4A02T	24LC02B	4L2BT				
24AA024	4A24T	24LC024	4L24T				
24AA025	4A25T	24LC025	4L25T				
				24C02C	4C2CT		
24AA04	4A04T	24LC04B	4L4BT				
24AA08	4A08T	24LC08B	4L8BT				
24AA16	4A16T	24LC16B	4L16T				
24AA32A	4A32AT	24LC32A	4L32AT				
24AA64	4A64T	24LC64	4L64T			24FC64	4F64T
24AA128	4A128T	24LC128	4L128T			24FC128	4F128T
24AA256	4A256T	24LC256	4L256T			24FC256	4F256T

Note: T = Temperature range: I = Industrial, E = Extended

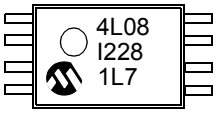
Legend:	XX...X	Part number or part number code
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code (2 characters for small packages)
	(e3)	Pb-free JEDEC designator for Matte Tin (Sn) plated devices

Note: For very small packages with no room for the Pb-free JEDEC designator (e3), the marking will only appear on the outer carton or reel label.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

8-Lead TSSOP

Example:



8-Lead TSSOP Package Marking							
Device	**Line 1 Marking**	**Device**	**Line 1 Marking**	**Device**	**Line 1 Marking**	**Device**	**Line 1 Marking**
24AA00	4A00	24LC00	4L00	24C00	4C00		
24AA01	4A01	24LC01B	4L1B				
24AA014	4A14	24LC014	4L14				
				24C01C	4C1C		
24AA02	4A02	24LC02B	4L02				
24AA024	4A24	24LC024	4L24				
24AA025	4A25	24LC025	4L25				
				24C02C	4C2C		
24AA04	4A04	24LC04B	4L04				
24AA08	4A08	24LC08B	4L08				
24AA16	4A16	24LC16B	4L16				
24AA32A	4AA	24LC32A	4LA				
24AA64	4AB	24LC64	4LB			24FC64	4FB
24AA128	4AC	24LC128	4LC			24FC128	4FC
24AA256	4AD	24LC256	4LD			24FC256	4FD

Note: T = Temperature range: I = Industrial, E = Extended

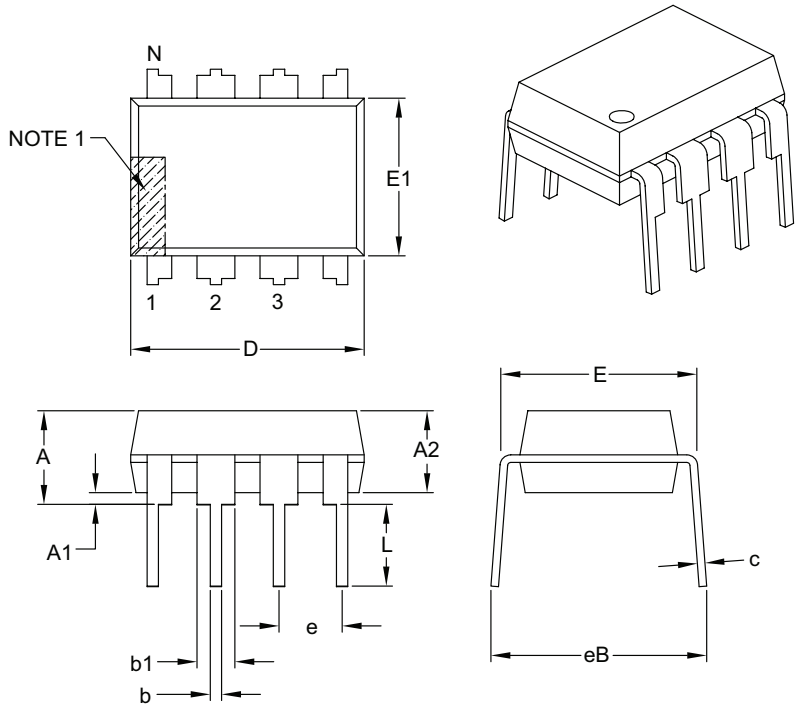
Legend:	XX...X	Part number or part number code
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code (2 characters for small packages)
	(e3)	Pb-free JEDEC designator for Matte Tin (Sn) plated devices

Note: For very small packages with no room for the Pb-free JEDEC designator (e3), the marking will only appear on the outer carton or reel label.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

8-Lead Plastic Dual In-Line (P) – 300 mil Body [PDIP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		INCHES		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		8	
Pitch	e		.100 BSC	
Top to Seating Plane	A	–	–	.210
Molded Package Thickness	A2	.115	.130	.195
Base to Seating Plane	A1	.015	–	–
Shoulder to Shoulder Width	E	.290	.310	.325
Molded Package Width	E1	.240	.250	.280
Overall Length	D	.348	.365	.400
Tip to Seating Plane	L	.115	.130	.150
Lead Thickness	c	.008	.010	.015
Upper Lead Width	b1	.040	.060	.070
Lower Lead Width	b	.014	.018	.022
Overall Row Spacing §	eB	–	–	.430

Notes:

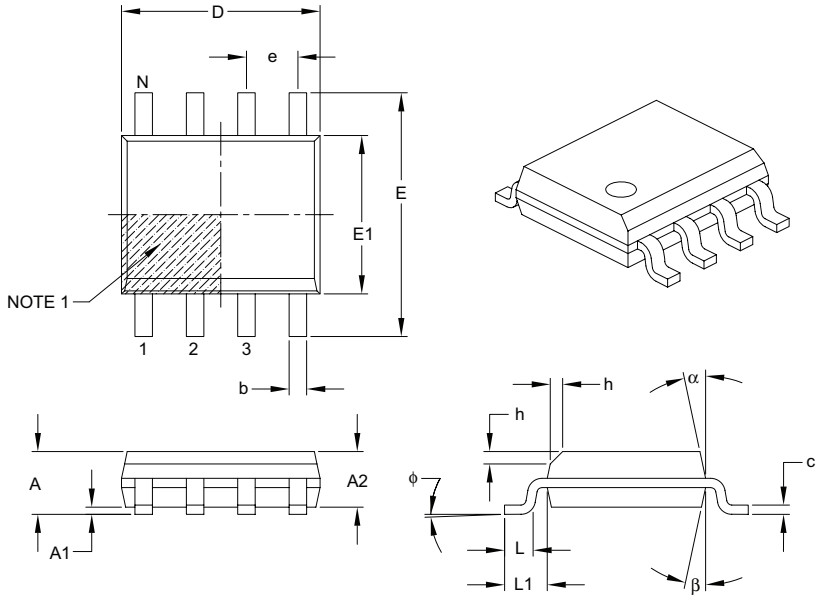
1. Pin 1 visual index feature may vary, but must be located with the hatched area.
2. § Significant Characteristic.
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" per side.
4. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-018B

8-Lead Plastic Small Outline (SN) – Narrow, 3.90 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		8	
Pitch	e		1.27 BSC	
Overall Height	A	–	–	1.75
Molded Package Thickness	A2	1.25	–	–
Standoff §	A1	0.10	–	0.25
Overall Width	E		6.00 BSC	
Molded Package Width	E1		3.90 BSC	
Overall Length	D		4.90 BSC	
Chamfer (optional)	h	0.25	–	0.50
Foot Length	L	0.40	–	1.27
Footprint	L1		1.04 REF	
Foot Angle	ϕ	0°	–	8°
Lead Thickness	c	0.17	–	0.25
Lead Width	b	0.31	–	0.51
Mold Draft Angle Top	α	5°	–	15°
Mold Draft Angle Bottom	β	5°	–	15°

Notes:

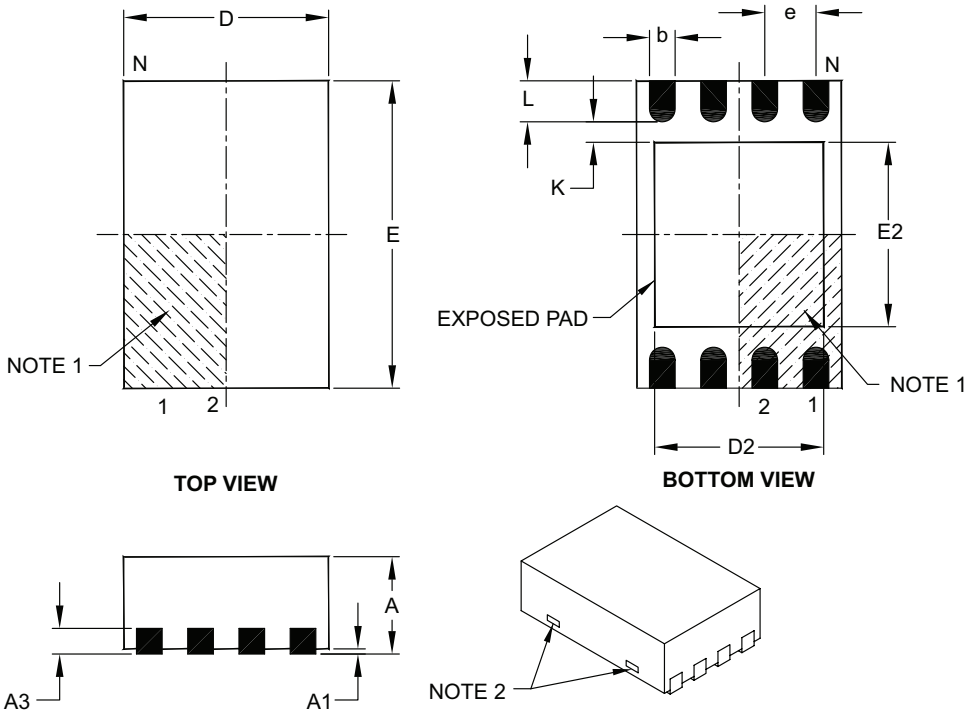
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic.
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15 mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-057B

8-Lead Plastic Dual Flat, No Lead Package (MC) – 2x3x0.9 mm Body [DFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		8	
Pitch	e		0.50 BSC	
Overall Height	A	0.80	0.90	1.00
Standoff	A1	0.00	0.02	0.05
Contact Thickness	A3		0.20 REF	
Overall Length	D		2.00 BSC	
Overall Width	E		3.00 BSC	
Exposed Pad Length	D2	1.30	–	1.75
Exposed Pad Width	E2	1.50	–	1.90
Contact Width	b	0.18	0.25	0.30
Contact Length	L	0.30	0.40	0.50
Contact-to-Exposed Pad	K	0.20	–	–

Notes:

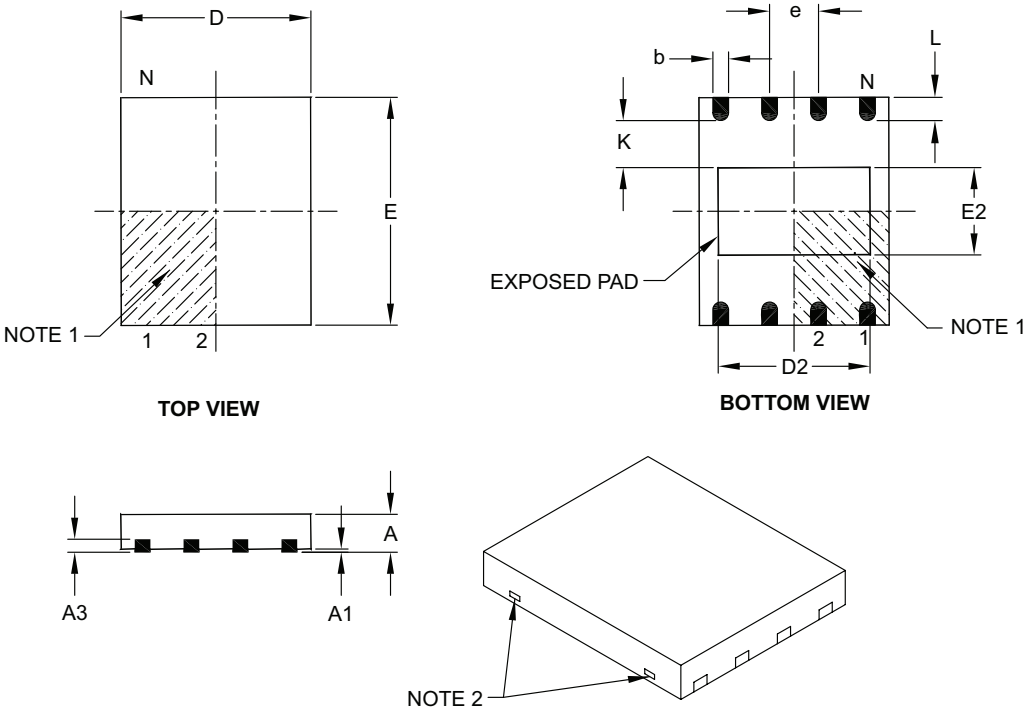
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package may have one or more exposed tie bars at ends.
3. Package is saw singulated.
4. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-123B

8-Lead Plastic Dual Flat, No Lead Package (MF) – 6x5 mm Body [DFN-S]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		8	
Pitch	e		1.27 BSC	
Overall Height	A	0.80	0.85	1.00
Standoff	A1	0.00	0.01	0.05
Contact Thickness	A3		0.20 REF	
Overall Length	D		5.00 BSC	
Overall Width	E		6.00 BSC	
Exposed Pad Length	D2	3.90	4.00	4.10
Exposed Pad Width	E2	2.20	2.30	2.40
Contact Width	b	0.35	0.40	0.48
Contact Length	L	0.50	0.60	0.75
Contact-to-Exposed Pad	K	0.20	–	–

Notes:

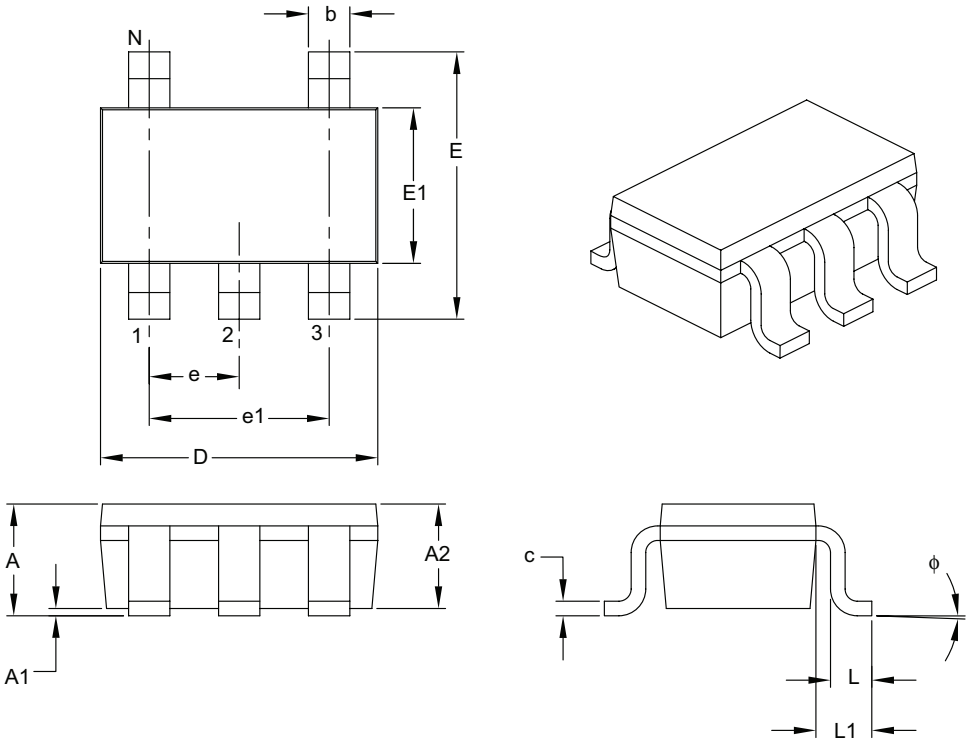
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package may have one or more exposed tie bars at ends.
3. Package is saw singulated.
4. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-122B

5-Lead Plastic Small Outline Transistor (OT) [SOT-23]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		5	
Lead Pitch	e		0.95 BSC	
Outside Lead Pitch	e1		1.90 BSC	
Overall Height	A	0.90	–	1.45
Molded Package Thickness	A2	0.89	–	1.30
Standoff	A1	0.00	–	0.15
Overall Width	E	2.20	–	3.20
Molded Package Width	E1	1.30	–	1.80
Overall Length	D	2.70	–	3.10
Foot Length	L	0.10	–	0.60
Footprint	L1	0.35	–	0.80
Foot Angle	ϕ	0°	–	30°
Lead Thickness	c	0.08	–	0.26
Lead Width	b	0.20	–	0.51

Notes:

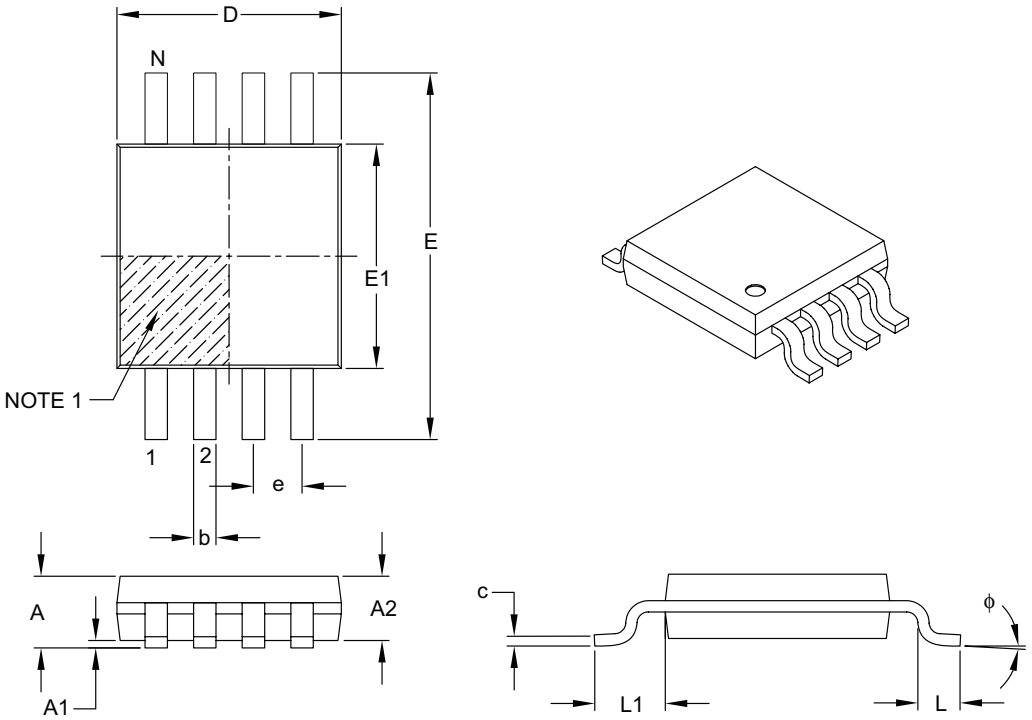
1. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.127 mm per side.
2. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-091B

8-Lead Plastic Micro Small Outline Package (MS) [MSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		8	
Pitch	e		0.65 BSC	
Overall Height	A	–	–	1.10
Molded Package Thickness	A2	0.75	0.85	0.95
Standoff	A1	0.00	–	0.15
Overall Width	E		4.90 BSC	
Molded Package Width	E1		3.00 BSC	
Overall Length	D		3.00 BSC	
Foot Length	L	0.40	0.60	0.80
Footprint	L1		0.95 REF	
Foot Angle	ϕ	0°	–	8°
Lead Thickness	c	0.08	–	0.23
Lead Width	b	0.22	–	0.40

Notes:

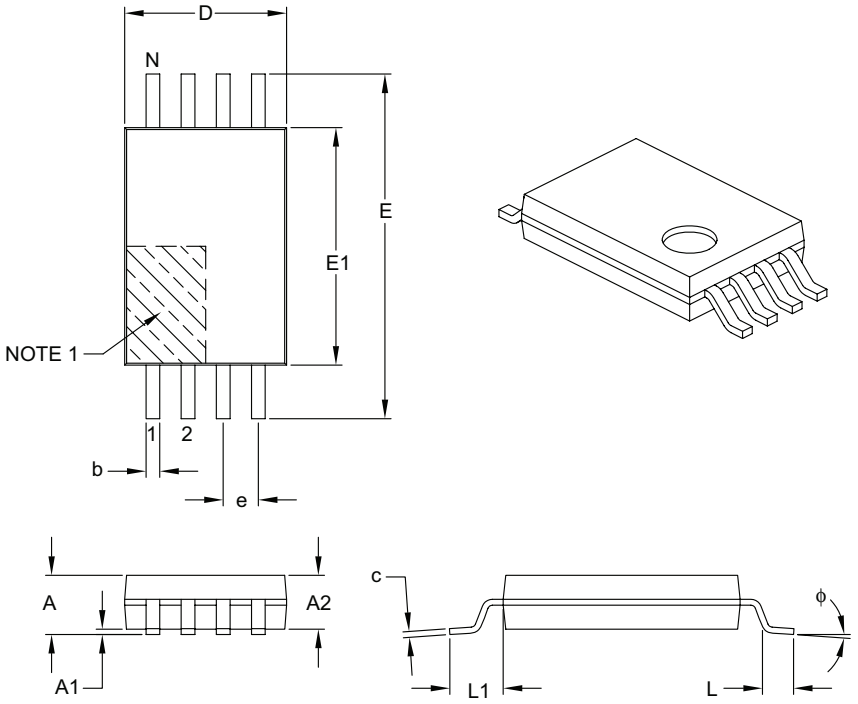
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15 mm per side.
3. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-111B

8-Lead Plastic Thin Shrink Small Outline (ST) – 4.4 mm Body [TSSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		8	
Pitch	e		0.65 BSC	
Overall Height	A	–	–	1.20
Molded Package Thickness	A2	0.80	1.00	1.05
Standoff	A1	0.05	–	0.15
Overall Width	E		6.40 BSC	
Molded Package Width	E1	4.30	4.40	4.50
Molded Package Length	D	2.90	3.00	3.10
Foot Length	L	0.45	0.60	0.75
Footprint	L1		1.00 REF	
Foot Angle	ϕ	0°	–	8°
Lead Thickness	c	0.09	–	0.20
Lead Width	b	0.19	–	0.30

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15 mm per side.
3. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-086B

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PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	X	X	/XX
Device Part Number (Table 1-1)	Packaging Medium	Temperature Range	Package

Device:	See Table 1-1		
Temperature Range:	I	=	-40°C to +85°C
	E	=	-40°C to +125°C
Packaging Medium:	T	=	Tape and Reel
	Blank	=	Tube
Package:	P	=	Plastic DIP (300 mil body), 8-lead
	SN	=	Plastic SOIC (3.90 mm body), 8-lead
	SM	=	Plastic SOIC (208 mil body), 8-lead
	ST	=	Plastic TSSOP (4.4 mm), 8-lead
	MS	=	MSOP (3.0 mm), 8-lead
	OT	=	SOT-23, 5-lead (Tape and Reel only)
	MC	=	2x3 mm DFN, 8-lead (Tape and Reel only)
	MF	=	5x6 mm DFN, 8-lead

Examples:

a) 24AA014-I/SN: 1 Kbit, Industrial Temperature, 1.7V, SOIC package

b) 24AA02T-I/OT: 2 Kbit, Industrial Temperature, 1.7V, SOT-23 package, Tape and Reel

c) 24LC16B-I/P: 16 Kbit, Industrial Temperature, 2.5V, PDIP package

d) 24LC32A-E/MS: 32 Kbit, Extended Temperature, 2.5V, MSOP package

e) 24LC64T-I/MC: 64 Kbit, Industrial Temperature, 2.5V 2x3 mm DFN package, Tape and Reel

f) 24FC512T-I/SM: 512 Kbit, Industrial Temperature, 1 MHz, SOIC package, Tape and Reel

NOTES:

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- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
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Korea - Seoul
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