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## Block Diagram

## 2 Block Diagram

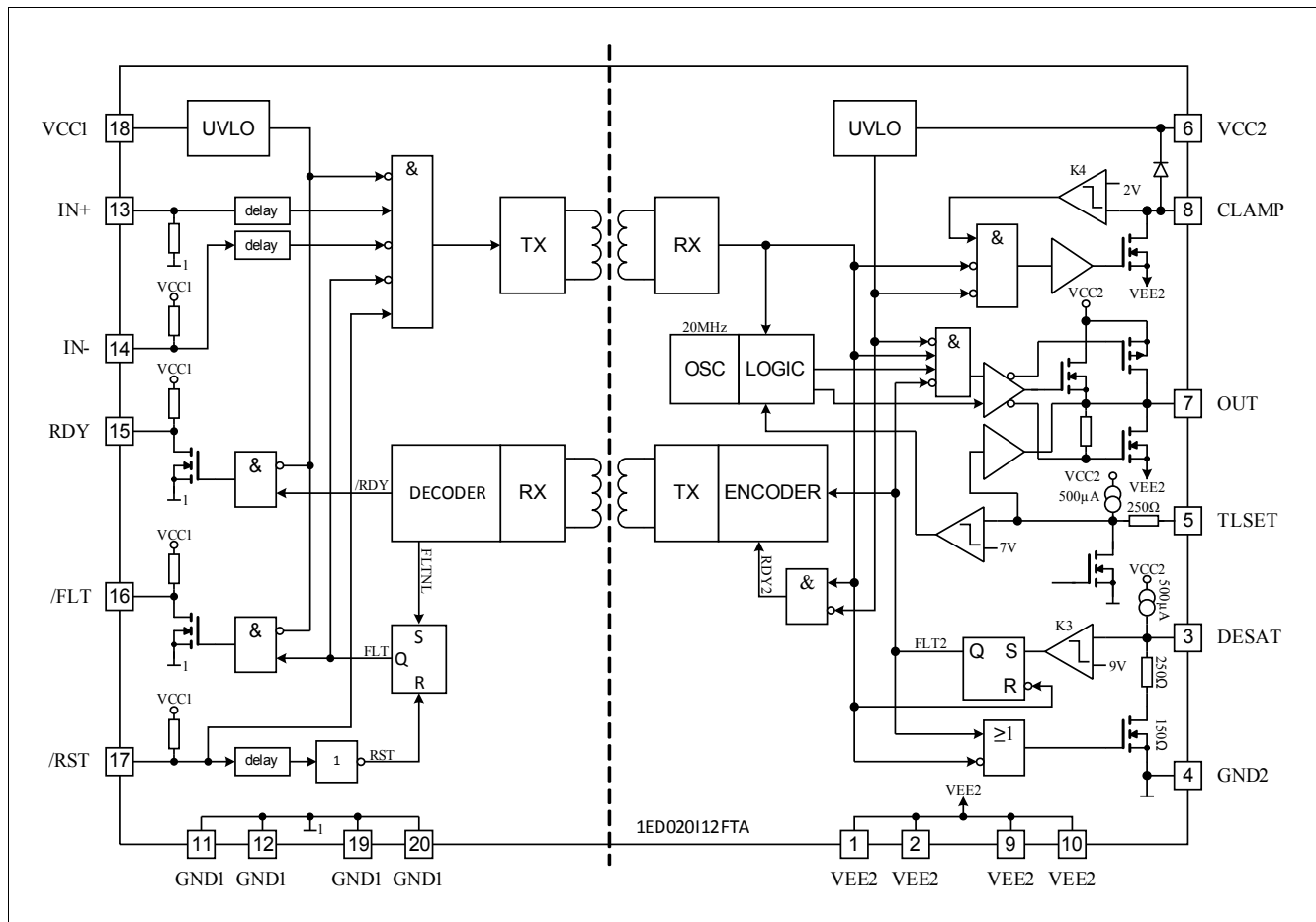


Figure 2-1 Block Diagram 1ED020I12FTA

## 3 Pin Configuration and Functionality

### 3.1 Pin Configuration

Table 3-1 Pin Configuration

Pin No.	Name	Function
1	VEE2	Negative power supply output side
2	VEE2	Negative power supply output side
3	DESAT	Desaturation protection
4	GND2	Signal ground output side
5	TLSET	Two level set
6	VCC2	Positive power supply output side
7	OUT	Driver output
8	CLAMP	Miller clamping
9	VEE2	Negative power supply output side
10	VEE2	Negative power supply output side
11	GND1	Ground input side
12	GND1	Ground input side
13	IN+	Non inverted driver input
14	IN-	Inverted driver input
15	RDY	Ready output
16	FLT	Fault output, low active
17	RST	Reset input, low active
18	VCC1	Positive power supply input side
19	GND1	Ground input side
20	GND1	Ground input side

## Pin Configuration and Functionality

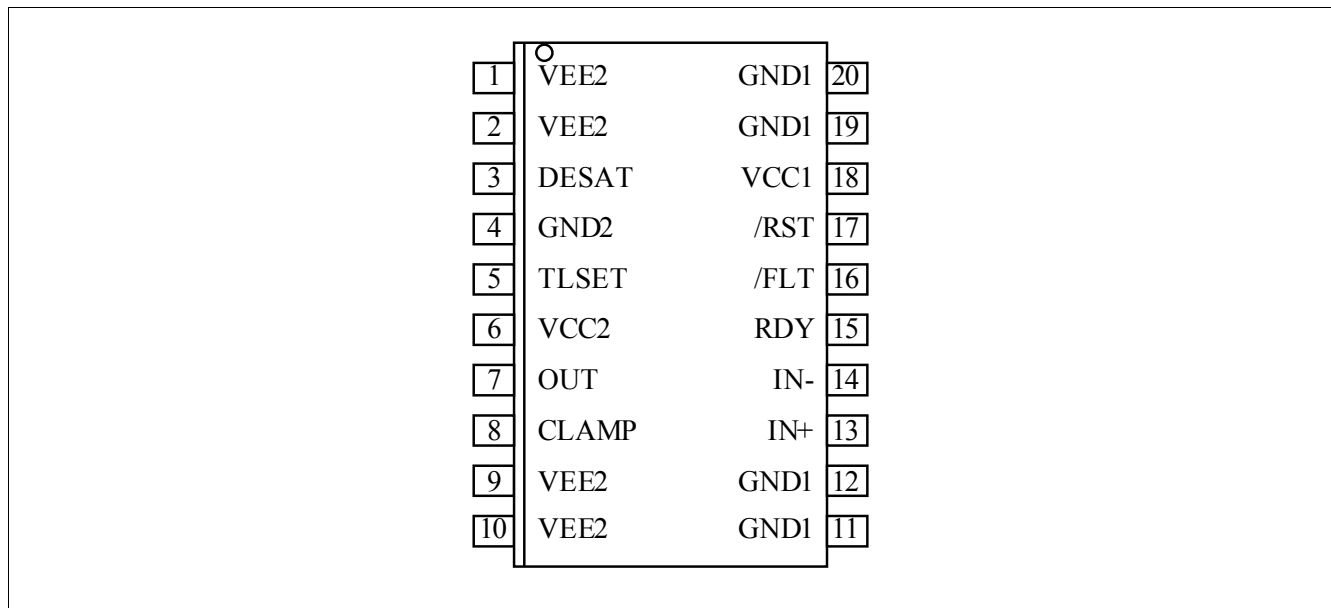


Figure 3-1 Pin Configuration PG-DSO-20 (top view)

### 3.2 Pin Functionality

#### GND1

Ground connection of the input side.

#### IN+ Non Inverting Driver Input

IN+ control signal for the driver output if IN- is set to low. (The IGBT is on if IN+ = high and IN- = low)

A minimum pulse width is defined to make the IC robust against glitches at IN+. An internal Pull-Down-Resistor ensures IGBT Off-State.

#### IN- Inverting Driver Input

IN- control signal for driver output if IN+ is set to high. (IGBT is on if IN- = low and IN+ = high)

A minimum pulse width is defined to make the IC robust against glitches at IN-. An internal Pull-Up-Resistor ensures IGBT Off-State.

#### /RST Reset Input

**Function 1:** Enable/shutdown of the input chip. (The IGBT is off if /RST = low). A minimum pulse width is defined to make the IC robust against glitches at /RST.

**Function 2:** Resets the DESAT-FAULT-state of the chip if /RST is low for a time  $T_{RST}$ . An internal Pull-Up-Resistor is used to ensure /FLT status output.

#### /FLT Fault Output

Open-drain output to report a desaturation error of the IGBT (FLT is low if desaturation occurs)

#### RDY Ready Status

Open-drain output to report the correct operation of the device (RDY = high if both chips are above the UVLO level and the internal chip transmission is faultless).

## Pin Configuration and Functionality

### VCC1

5 V power supply of the input chip

### VEE2

Negative power supply pins of the output chip. If no negative supply voltage is available, all VEE2 pins have to be connected to GND2.

### DESAT Desaturation Detection Input

Monitoring of the IGBT saturation voltage ( $V_{CE}$ ) to detect desaturation caused by short circuits. If OUT is high,  $V_{CE}$  is above a defined value and a certain blanking time has expired, the desaturation protection is activated and the IGBT is switched off. The blanking time is adjustable by an external capacitor.

### CLAMP Miller Clamping

Ties the gate voltage to ground after the IGBT has been switched off at a defined voltage to avoid a parasitic switch-on of the IGBT. During turn-off, the gate voltage is monitored and the clamp output is activated when the gate voltage goes below 2 V below VEE2.

### GND2 Reference Ground

Reference ground of the output chip.

### OUT Driver Output

Output pin to drive an IGBT. The voltage is switched between VEE2 and VCC2. In normal operating mode Vout is controlled by IN+, IN- and /RST. During error mode (UVLO, internal error or DESAT) Vout is set to VEE2 independent of the input control signals.

### VCC2

Positive power supply pin of the output side.

### TLSET Two Level Turn Off Adjust

Circuitry at TLSET adjust the two level turn off time with an external capacitor to GND2 and the two level voltage with an external Zener diode to GND2, for wave forms please see [Figure 7-4](#).



## 4 Functional Description

### 4.1 Introduction

The 1ED020I12FTA is an advanced IGBT gate driver for motor drives typical greater 10 kW. Control and protection functions are included to make possible the design of high reliability systems.

The device consists of two galvanic separated parts. The input chip can be directly connected to a standard 5 V DSP or microcontroller with CMOS in/output and the output chip is connected to the high voltage side.

An effective active Miller clamp function avoids the need of negative gate driving in some applications and allows the use of a simple bootstrap supply for the high side driver.

A rail-to-rail driver output enables the user to provide easy clamping of the IGBTs gate voltage during short circuit of the IGBT. So an increase of short circuit current due to the feedback via the Miller capacitance can be avoided. Further, a rail-to-rail output reduces power dissipation.

The device also includes an IGBT desaturation protection with a FAULT status output.

A two-level turn-off feature with adjustable delay protects against excessive overvoltage at turn-off in case of overcurrent or short circuit condition. The same delay is applied at turn-on to prevent pulse width distortion.

A READY status output reports if the device is supplied and operates correctly.

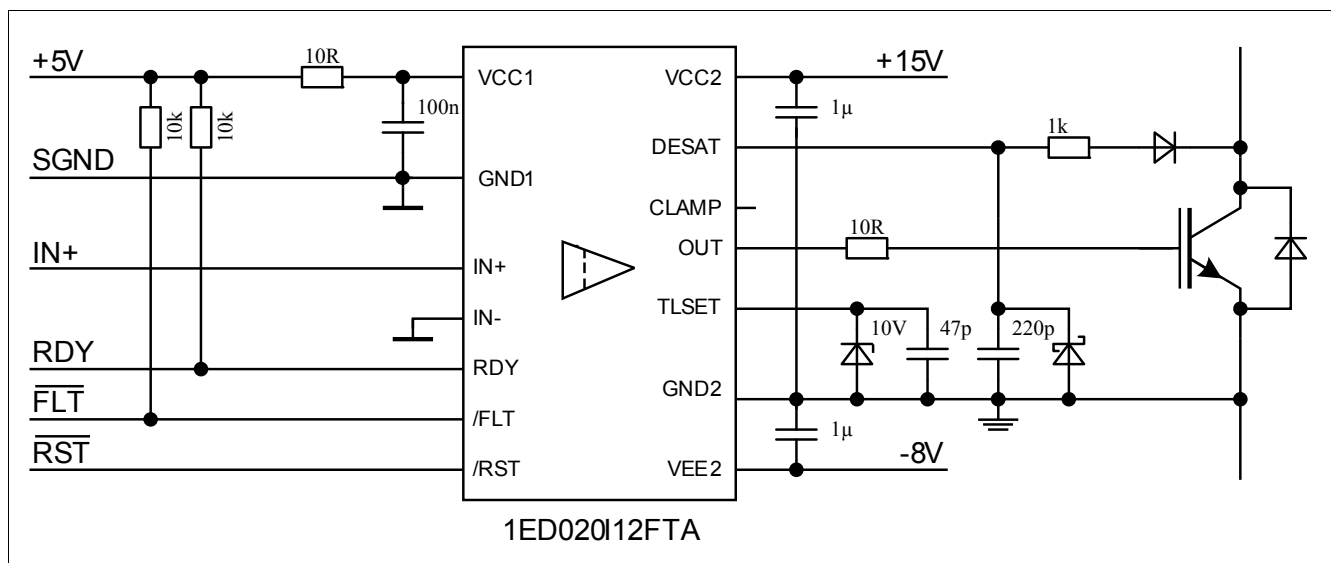


Figure 4-1 Application Example Bipolar Supply

### 4.2 Supply

The driver 1ED020I12FTA is designed to support two different supply configurations, bipolar supply and unipolar supply.

In bipolar supply the driver is typically supplied with a positive voltage of 15V at VCC2 and a negative voltage of -8V at VEE2, refer to [Figure 4-1](#). Negative supply prevents a dynamic turn on due to the additional charge which is generated from IGBT input capacitance times negative supply voltage. If an appropriate negative supply voltage is used, connecting CLAMPxx to IGBT gate is redundant and therefore typically not necessary.

For unipolar supply configuration the driver is typically supplied with a positive voltage of 15V at VCC2. Erratically dynamic turn on of the IGBT could be prevented with active Miller clamp function, so CLAMP output is directly connected to IGBT gate, refer to [Figure 4-2](#).

## Functional Description

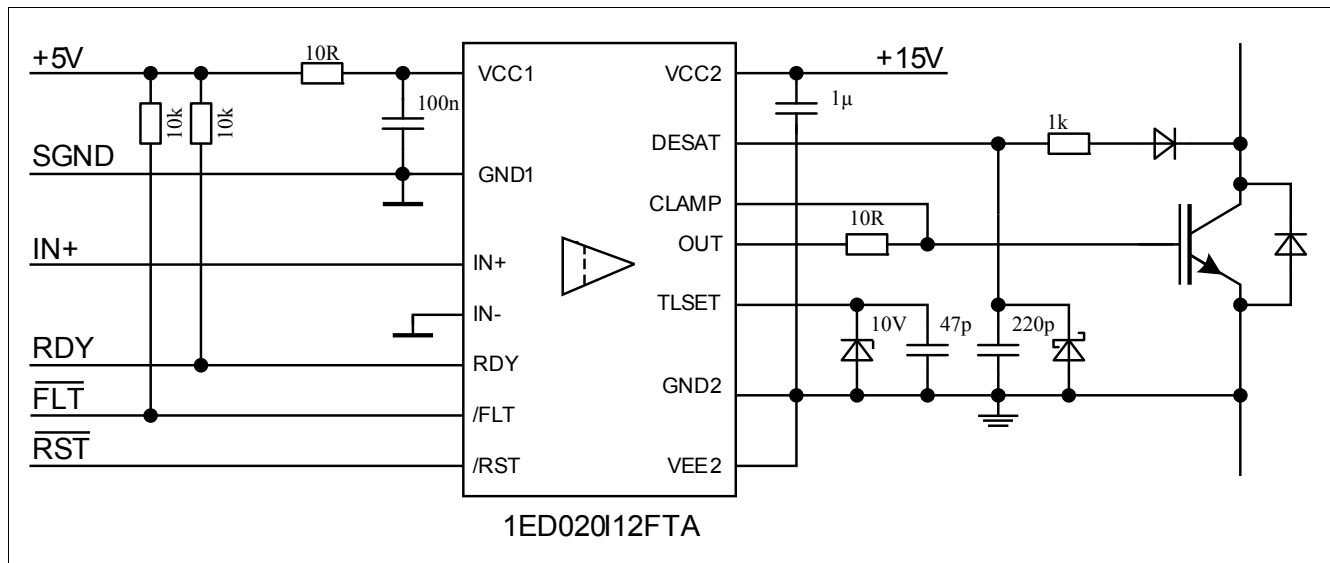


Figure 4-2 Application Example Unipolar Supply

## 4.3 Internal Protection Features

### 4.3.1 Undervoltage Lockout (UVLO)

To ensure correct switching of IGBTs the device is equipped with an undervoltage lockout for both chips, refer to [Figure 7-8](#) and [Figure 7-9](#).

If the power supply voltage  $V_{VCC1}$  of the input chip drops below  $V_{UVLOL1}$  a turn-off signal is sent to the output chip before power-down. The IGBT is switched off and the signals at IN+ and IN- are ignored as long as  $V_{VCC1}$  reaches the power-up voltage  $V_{UVLOH1}$ .

If the power supply voltage  $V_{VCC2}$  of the output chip goes down below  $V_{UVLOL2}$  the IGBT is switched off and signals from the input chip are ignored as long as  $V_{VCC2}$  reaches the power-up voltage  $V_{UVLOH2}$ . VEE2 is not monitored, otherwise negative supply voltage range from 0 V to -12 V would not be possible.

### 4.3.2 READY Status Output

The READY output at pin /RDY shows the status of three internal protection features.

- UVLO of the input chip
- UVLO of the output chip after a short delay
- Internal signal transmission after a short delay

It is not necessary to reset the READY signal since its state only depends on the status of the former mentioned protection signals.

### 4.3.3 Watchdog Timer

During normal operation the internal signal transmission is monitored by a watchdog timer. If the transmission fails for a given time, the IGBT is switched off and the READY output reports an internal error.

### 4.3.4 Active Shut-Down

The Active Shut-Down feature ensures a safe IGBT off-state if the output chip is not connected to the power supply, IGBT gate is clamped at OUT to VEE2.

#### 4.4 Non-Inverting and Inverting Inputs

There are two possible input modes to control the IGBT. At non-inverting mode IN+ controls the driver output while IN- is set to low. At inverting mode IN- controls the driver output while IN+ is set to high, refer to [Figure 7-2](#). A minimum input pulse width is defined to filter occasional glitches.

#### 4.5 Driver Output

The output driver section uses only MOSFETs to provide a rail-to-rail output. This feature permits that tight control of gate voltage during on-state and short circuit can be maintained as long as the drivers supply is stable. Due to the low internal voltage drop, switching behaviour of the IGBT is predominantly governed by the gate resistor. Furthermore, it reduces the power to be dissipated by the driver.

#### 4.6 Two-Level Turn-Off

The Two-Level Turn-OFF introduces a second turn off voltage level at the driver output in between ON- and OFF-level, refer to [Figure 7-3](#). This additional level ensures lower  $V_{CE}$  overshoots at turn off by reducing gate emitter voltage of the IGBT at short circuits or over current events. The  $V_{GE}$  level is adjusting the current of the IGBT at the end two level turn off interval, the required timing is depending on stray inductance and over current at beginning of two level turn off interval.

Reference voltage level and hold up time could be adjusted at TLSET pin. The reference voltage is set by the required Zener diode connected between pin TLSET and GND2. The holdup time is set by the capacitor connected to the same pin TLSET and GND2.

The hold time can be adjusted during switch on using the whole capacitance connected at pin TLSET including capacitor, parasitic wiring capacitance and junction capacitance of Zener diode. When a switch on signal is given the IC starts to discharge  $C_{TLSET}$ . Discharging  $C_{TLSET}$  is stopped after 500 ns. Then  $C_{TLSET}$  is charged with an internal charge current  $I_{TLSET}$ . When the voltage of the capacitor  $C_{TLSET}$  exceeds 7 V a second current source starts charging  $C_{TLSET}$  up to  $V_{ZDIODE}$ . At the end of this discharge-charge cycle the gate driver is switched on.

The time between IN initiated switch-on signal (minus an internal propagation delay of approximately 200 ns) and switch-on of the gate drive is sampled and stored digitally. It represents the two level turn off set time  $T_{TLSET}$  during switch-off. Due to digitalization the  $t_{pdon}$  time can vary in time steps of 50 ns.

If switch off is initiated from IN+, IN- or /RST signal, the gate driver is switched off immediately after internal propagation delay of approximately 200 ns and  $V_{OUT}$  begins to decrease to the second gate voltage level.

For switch off initiated by DESAT, the gate driver switch off is delayed by desaturation sense to OUT delay, afterwards  $V_{OUT}$  begins to decrease to the second gate voltage level.

For reaching second gate voltage level the output voltage  $V_{OUT}$  is sensed and compared with the Zener voltage  $V_{ZDIODE}$ . When  $V_{OUT}$  falls below the reference voltage  $V_{ZDIODE}$  of the Zener diode the switch off process is interrupted and  $V_{OUT}$  is adjusted to  $V_{ZDIODE}$ . OUT is switched to VEE2 after the holdup time has passed.

The Two-Level Turn-OFF function cannot be disabled.

## 4.7 Minimal On Time / Off Time

The 1ED020I12FTA driver requires minimal on and off time for proper operation in the application. Minimal on time must be greater than the adjustable two level plateau time  $T_{TLSET}$ ; shorter on times will be suppressed by generating of the plateau time refer to [Figure 7-5](#). Due to the short on time, the voltage at TLSET pin does not reach the comparator threshold; therefore the driver does not turn on. A similar principle takes place for off time. Minimal off time must be greater than  $T_{TLSET}$ ; shorter off times will be suppressed, which means OUT stays on refer to [Figure 7-6](#). A two level turn off plateau cannot be shortened by the driver. If the driver has entered the turn off sequence it cannot switch off due to the fact, that the driver has already entered the shut off mode. But if the driver input signal is turned on again, it will leave the lower level after  $T_{TLSET}$  time by switching OUT to high, refer to [Figure 7-7](#).

## 4.8 External Protection Features

### 4.8.1 Desaturation Protection

A desaturation protection ensures the protection of the IGBT at short circuit. When the DESAT voltage goes up and reaches 9 V, the output is driven low, refer to [Figure 7-4](#). Further, the FAULT output is activated. A programmable blanking time is used to allow enough time for IGBT saturation. Blanking time is provided by a highly precise internal current source and an external capacitor.

### 4.8.2 Active Miller Clamp

In a half bridge configuration the switched off IGBT tends to dynamically turn on during turn on phase of the opposite IGBT. A Miller clamp allows sinking the Miller current across a low impedance path in this high  $dV/dt$  situation. Therefore in many applications, the use of a negative supply voltage can be avoided.

During turn-off, the gate voltage is monitored and the clamp output is activated when the gate voltage goes below typical 2 V (related to VEE2). The clamp is designed for a Miller current up to 2 A.

### 4.8.3 Short Circuit Clamping

During short circuit the IGBTs gate voltage tends to rise because of the feedback via the Miller capacitance. An additional protection circuit connected to OUT and CLAMP limits this voltage to a value slightly higher than the supply voltage. A current of maximum 500 mA for 10  $\mu$ s may be fed back to the supply through one of this paths. If higher currents are expected or a tighter clamping is desired external Schottky diodes may be added.

## 4.9 RESET

The reset input has two functions.

Firstly, /RST is in charge of setting back the FAULT output. If /RST is low longer than a given time, /FLT will be cleared at the rising edge of /RST, refer to [Figure 7-4](#); otherwise, it will remain unchanged. Moreover, it works as enable/shutdown of the input logic, refer to [Figure 7-2](#).

## Electrical Parameters

### 5 Electrical Parameters

#### 5.1 Absolute Maximum Ratings

*Note: Absolute maximum ratings are defined as ratings, which when being exceeded may lead to destruction of the integrated circuit. Unless otherwise noted all parameters refer to GND1.*

**Table 5-1 Absolute Maximum Ratings**

Parameter	Symbol	Values		Unit	Note
		Min.	Max.		
Positive power supply output side	$V_{VCC2}$	-0.3	20	V	1)
Negative power supply output side	$V_{VEE2}$	-12	0.3	V	1)
Maximum power supply voltage output side ( $V_{VCC2} - V_{VEE2}$ )	$V_{max2}$	–	28	V	–
Gate driver output	$V_{OUT}$	$V_{VEE2}-0.3$	$V_{VCC2}+0.3$	V	–
Gate driver high output maximum current	$I_{OUT}$	–	2.4	A	$t = 2 \mu s$
Gate & Clamp driver low output maximum current	$I_{OUT}$	–	2.4	A	$t = 2 \mu s$
Maximum short circuit clamping time	$t_{CLP}$	–	10	$\mu s$	$I_{CLAMP/OUT} = 500 \text{ mA}$
Positive power supply input side	$V_{VCC1}$	-0.3	6.5	V	–
Logic input voltages ( $IN+$ , $IN-$ , $RST$ )	$V_{LogicIN}$	-0.3	6.5	V	–
Opendrain Logic output voltage ( $\overline{FLT}$ )	$V_{FLT\#}$	-0.3	6.5	V	–
Opendrain Logic output voltage (RDY)	$V_{RDY}$	-0.3	6.5	V	–
Opendrain Logic output current ( $\overline{FLT}$ )	$I_{FLT\#}$	–	10	mA	–
Opendrain Logic output current (RDY)	$I_{RDY}$	–	10	mA	–
Pin DESAT voltage	$V_{DESAT}$	-0.3	$V_{VCC2} + 0.3$	V	1)
Pin CLAMP voltage	$V_{CLAMP}$	-0.3	$V_{VCC2} + 0.3^{2)}$	V	3)
Junction temperature	$T_J$	-40	150	$^{\circ}C$	–
Storage temperature	$T_S$	-55	150	$^{\circ}C$	–
Power dissipation, per input part	$P_{D, IN}$	–	100	mW	4) @ $T_A = 25^{\circ}C$
Power dissipation, per output part	$P_{D, OUT}$	–	700	mW	4) @ $T_A = 25^{\circ}C$
Thermal resistance (Input part)	$R_{THJA, IN}$	–	139	K/W	4) @ $T_A = 25^{\circ}C$
Thermal resistance (Output chip active)	$R_{THJA, OUT}$	–	117	K/W	4) @ $T_A = 25^{\circ}C$
ESD Capability	$V_{ESD}$	–	1.5	kV	Human Body Model <sup>5)</sup>

1) With respect to GND2.

2) May be exceeded during short circuit clamping.

## Electrical Parameters

- 3) With respect to VEE2.
- 4) Output IC power dissipation is derated linearly at 8.5 mW/°C above 68°C. Input IC power dissipation does not require derating. See [Figure 9-1](#) for reference layouts for these thermal data. Thermal performance may change significantly with layout and heat dissipation of components in close proximity.
- 5) According to EIA/JESD22-A114-B (discharging a 100 pF capacitor through a 1.5 kΩ series resistor).

## 5.2 Operating Parameters

*Note: Within the operating range the IC operates as described in the functional description. Unless otherwise noted all parameters refer to GND1.*

**Table 5-2 Operating Parameters**

Parameter	Symbol	Values		Unit	Note
		Min.	Max.		
Positive power supply output side	$V_{VCC2}$	13	20	V	1)
Negative power supply output side	$V_{VEE2}$	-12	0	V	1)
Maximum power supply voltage output side ( $V_{VCC2} - V_{VEE2}$ )	$V_{max2}$	–	28	V	–
Positive power supply input side	$V_{VCC1}$	4.5	5.5	V	–
Logic input voltages (IN+, IN-, RST)	$V_{LogicIN}$	-0.3	5.5	V	–
Pin CLAMP voltage	$V_{CLAMP}$	$V_{VEE2} - 0.3$	$V_{VCC2}^{2)}$	V	–
Pin DESAT voltage	$V_{DESAT}$	-0.3	$V_{VCC2}$	V	1)
Pin TLSET voltage	$V_{TLSET}$	-0.3	$V_{VCC2}$	V	1)
Ambient temperature	$T_A$	-40	125	°C	–
Common mode transient immunity <sup>3)</sup>	$ dV_{ISO}/dt $	–	50	kV/μs	@ 500 V

1) With respect to GND2.

2) May be exceeded during short circuit clamping.

3) The parameter is not subject to production test - verified by design/characterization

## 5.3 Recommended Operating Parameters

*Note: Unless otherwise noted all parameters refer to GND1.*

**Table 5-3 Recommended Operating Parameters**

Parameter	Symbol	Value	Unit	Note
Positive power supply output side	$V_{VCC2}$	15	V	1)
Negative power supply output side	$V_{VEE2}$	-8	V	1)
Positive power supply input side	$V_{VCC1}$	5	V	–

1) With respect to GND2.

## Electrical Parameters

### 5.4 Electrical Characteristics

*Note: The electrical characteristics include the spread of values in supply voltages, load and junction temperatures given below. Typical values represent the median values at  $T_A = 25^\circ\text{C}$ . Unless otherwise noted all voltages are given with respect to their respective GND (GND1 for pins 11 to 20, GND2 for pins 1 to 10).*

#### 5.4.1 Voltage Supply

Table 5-4 Voltage Supply

Parameter	Symbol	Values			Unit	Note
		Min.	Typ.	Max.		
UVLO Threshold Input Chip	$V_{UVLOH1}$	–	4.1	4.3	V	–
	$V_{UVLOL1}$	3.5	3.8	–	V	–
UVLO Hysteresis Input Chip ( $V_{UVLOH1} - V_{UVLOL1}$ )	$V_{HYS1}$	0.15	–	–	V	–
UVLO Threshold Output Chip	$V_{UVLOH2}$	–	12.0	12.6	V	–
	$V_{UVLOL2}$	10.4	11.0	–	V	–
UVLO Hysteresis Output Chip ( $V_{UVLOH1} - V_{UVLOL1}$ )	$V_{HYS2}$	0.7	0.9	–	V	–
Quiescent Current Input Chip	$I_{Q1}$	–	7	9	mA	$V_{VCC1} = 5\text{ V}$ IN+ = High, IN- = Low =>OUT = High, RDY = High, /FLT = High
Quiescent Current Output Chip	$I_{Q2}$	–	4.5	6	mA	$V_{VCC2} = 15\text{ V}$ $V_{VEE2} = -8\text{ V}$ IN+ = High, IN- = Low =>OUT = High, RDY = High, /FLT = High

Electrical Parameters

5.4.2 Logic Input and Output

Table 5-5 Logic Input and Output

Parameter	Symbol	Values			Unit	Note
		Min.	Typ.	Max.		
IN+, IN-, $\overline{\text{RST}}$ Low Input Voltage	$V_{\text{IN+L}},$ $V_{\text{IN-L}},$ $V_{\text{RSTL\#}}$	–	–	1.5	V	–
IN+, IN-, $\overline{\text{RST}}$ High Input Voltage	$V_{\text{IN+H}},$ $V_{\text{IN-H}},$ $V_{\text{RSTH\#}}$	3.5	–	–	V	–
IN-, $\overline{\text{RST}}$ Input Current	$I_{\text{IN-}}, I_{\text{RST\#}}$	–	100	400	$\mu\text{A}$	$V_{\text{IN-}} = \text{GND1}$ $V_{\text{RST\#}} = \text{GND1}$
IN+ Input Current	$I_{\text{IN+}},$	–	100	400	$\mu\text{A}$	$V_{\text{IN+}} = \text{VCC1}$
RDY, $\overline{\text{FLT}}$ Pull Up Current	$I_{\text{PRDY}}, I_{\text{PFLT\#}}$	–	100	400	$\mu\text{A}$	$V_{\text{RDY}} = \text{GND1}$ $V_{\text{FLT\#}} = \text{GND1}$
Input Pulse Suppression IN+, IN-	$T_{\text{MININ+}},$ $T_{\text{MININ-}}$	30	40	–	ns	–
Input Pulse Suppression $\overline{\text{RST}}$ for ENABLE/SHUTDOWN	$T_{\text{MINRST}}$	30	40	–	ns	–
Pulse Width $\overline{\text{RST}}$ for Resetting $\overline{\text{FLT}}$	$T_{\text{RST}}$	800	–	–	ns	–
$\overline{\text{FLT}}$ Low Voltage	$V_{\text{FLT L}}$	–	–	300	mV	$I_{\text{SINK(FLT\#)}} = 5 \text{ mA}$
RDY Low Voltage	$V_{\text{RDY L}}$	–	–	300	mV	$I_{\text{SINK(RDY)}} = 5 \text{ mA}$



## Electrical Parameters

### 5.4.3 Gate Driver

Table 5-6 Gate Driver

Parameter	Symbol	Values			Unit	Note
		Min.	Typ.	Max.		
High Level Output Voltage	$V_{OUTH1}$	$V_{VCC2}-1.2$	$V_{VCC2}-0.8$	–	V	$I_{OUTH} = -20 \text{ mA}$
	$V_{OUTH2}$	$V_{VCC2}-2.5$	$V_{VCC2}-2.0$	–	V	$I_{OUTH} = -200 \text{ mA}$
	$V_{OUTH3}$	$V_{VCC2}-9$	$V_{VCC2}-5$	–	V	$I_{OUTH} = -1 \text{ A}$
	$V_{OUTH4}$	–	$V_{VCC2}-10$	–	V	$I_{OUTH} = -2 \text{ A}$
High Level Output Peak Current	$I_{OUTH}$	-1.5	-2.0	–	A	IN+ = High, IN- = Low; OUT = High
Low Level Output Voltage	$V_{OUTL1}$	–	$V_{VEE2}+0.04$	$V_{VEE2}+0.09$	V	$I_{OUTL} = 20 \text{ mA}$
	$V_{OUTL2}$	–	$V_{VEE2}+0.3$	$V_{VEE2}+0.85$	V	$I_{OUTL} = 200 \text{ mA}$
	$V_{OUTL3}$	–	$V_{VEE2}+2.1$	$V_{VEE2}+5.0$	V	$I_{OUTL} = 1 \text{ A}$
	$V_{OUTL4}$	–	$V_{VEE2}+7$	–	V	$I_{OUTL} = 2 \text{ A}$
Low Level Output Peak Current	$I_{OUTL}$	1.5	2.0	–	A	IN+ = Low, IN- = Low; OUT = Low, $V_{VCC2} = 15 \text{ V}$ , $V_{VEE2} = -8 \text{ V}$

### 5.4.4 Active Miller Clamp

Table 5-7 Active Miller Clamp

Parameter	Symbol	Values			Unit	Note
		Min.	Typ.	Max.		
Low Level Clamp Voltage	$V_{CLAMPL1}$	–	$V_{VEE2}+0.03$	$V_{VEE2}+0.08$	V	$I_{OUTL} = 20 \text{ mA}$
	$V_{CLAMPL2}$	–	$V_{VEE2}+0.3$	$V_{VEE2}+0.8$	V	$I_{OUTL} = 200 \text{ mA}$
	$V_{CLAMPL3}$	–	$V_{VEE2}+1.9$	$V_{VEE2}+4.8$	V	$I_{OUTL} = 1 \text{ A}$
Low Level Clamp Current	$I_{CLAMPL}$	2	–	–	A	<sup>1)</sup>
Clamp Threshold Voltage	$V_{CLAMP}$	1.6	2.1	2.4	V	Related to VEE2

1) The parameter is not subject to production test - verified by design/characterization

## Electrical Parameters

### 5.4.5 Short Circuit Clamping

Table 5-8 Short Circuit Clamping

Parameter	Symbol	Values			Unit	Note
		Min.	Typ.	Max.		
Clamping voltage (OUT) ( $V_{OUT} - V_{VCC2}$ )	$V_{CLPout}$	–	0.8	1.3	V	IN+ = High, IN- = Low, OUT = High $I_{OUT} = 500$ mA (pulse test, $t_{CLPmax} = 10$ $\mu$ s)
Clamping voltage (CLAMP) ( $V_{VCLAMP} - V_{VCC2}$ )	$V_{CLPclamp}$	–	1.3	–	V	IN+ = High, IN- = Low, OUT = High $I_{CLAMP} = 500$ mA (pulse test, $t_{CLPmax} = 10$ $\mu$ s)
Clamping voltage (CLAMP)	$V_{CLPclamp}$	–	0.7	1.1	V	IN+ = High, IN- = Low, OUT = High $I_{CLAMP} = 20$ mA

### 5.4.6 Dynamic Characteristics

Dynamic characteristics are measured with  $V_{VCC1} = 5$  V,  $V_{VCC2} = 15$  V and  $V_{VEE2} = -8$  V.

Table 5-9 Dynamic Characteristics

Parameter	Symbol	Values			Unit	Note
		Min.	Typ.	Max.		
IN+, IN- Input to output propagation delay ON and OFF	$T_{PDON}$	1.5	1.75	2.0	$\mu$ s	$C_{TLSET} = 0$ pF, $C_{LOAD} = 100$ pF, $T_A = 25^\circ$ C
N+, IN- Input to output propagation delay distortion ( $T_{PDOFF} - T_{PDON}$ )	$T_{PDISTO}$	-50	0	50	ns	$C_{TLSET} = 0$ pF, $C_{LOAD} = 100$ pF, $T_A = 25^\circ$ C
N+, IN- Input to output propagation delay ON and OFF	$T_{PDONt}$	1.5	1.9	2.3	$\mu$ s	$C_{TLSET} = 0$ pF, $C_{LOAD} = 100$ pF, $T_A = 125^\circ$ C
N+, IN- Input to output propagation delay distortion ( $T_{PDOFF} - T_{PDON}$ )	$T_{PDISTOt}$	-20	45	70	ns	$C_{TLSET} = 0$ pF, $C_{LOAD} = 100$ pF, $T_A = 125^\circ$ C
IN+, IN- Input to output propagation delay ON and OFF	$T_{PDONt}$	1.45	1.75	2.05	$\mu$ s	$C_{TLSET} = 0$ pF, $C_{LOAD} = 100$ pF, $T_A = -40^\circ$ C
IN+ Input to output propagation delay distortion ( $T_{PDOFF} - T_{PDON}$ )	$T_{PDISTOt}$	-60	-5	50	ns	$C_{TLSET} = 0$ pF, $C_{LOAD} = 100$ pF, $T_A = -40^\circ$ C

## Electrical Parameters

Table 5-9 Dynamic Characteristics (cont'd)

Parameter	Symbol	Values			Unit	Note
		Min.	Typ.	Max.		
Rise Time	$T_{RISE}$	10	30	60	ns	$C_{LOAD} = 1 \text{ nF}$ , $V_L 10\%$ , $V_H 90\%$
		150	400	800	ns	$C_{LOAD} = 34 \text{ nF}$ $V_L 10\%$ , $V_H 90\%$
Fall Time	$T_{FALL}$	10	20	40	ns	$C_{LOAD} = 1 \text{ nF}$ $V_L 10\%$ , $V_H 90\%$
		100	250	500	ns	$C_{LOAD} = 34 \text{ nF}$ $V_L 10\%$ , $V_H 90\%$

## 5.4.7 Desaturation Protection

Table 5-10 Desaturation Protection

Parameter	Symbol	Values			Unit	Note
		Min.	Typ.	Max.		
Blanking Capacitor Charge Current	$I_{DESATC}$	450	500	550	$\mu\text{A}$	$V_{VCC2} = 15 \text{ V}$ , $V_{VEE2} = -8 \text{ V}$ $V_{DESAT} = 2 \text{ V}$
Blanking Capacitor Discharge Current	$I_{DESATD}$	11	15	–	mA	$V_{VCC2} = 15 \text{ V}$ , $V_{VEE2} = -8 \text{ V}$ $V_{DESAT} = 6 \text{ V}$
Desaturation Reference Level	$V_{DESAT}$	8.5	9	9.5	V	$V_{VCC2} = 15 \text{ V}$
Desaturation Sense to OUT TLTO	$T_{DESATOUT}$	–	250	320	ns	$V_{OUT} = 90\%$ $C_{LOAD} = 1 \text{ nF}$
Desaturation Sense to FLT Low Delay	$T_{DESATFLT}$	–	–	2.25	$\mu\text{s}$	$V_{FLT\#} = 10\%$ ; $I_{FLT\#} = 5 \text{ mA}$
Desaturation Low Voltage	$V_{DESATL}$	40	70	110	mV	IN+=Low, IN-=Low, OUT=Low

Electrical Parameters

### 5.4.8 Active Shut Down

Table 5-11 Active Shut Down

Parameter	Symbol	Values			Unit	Note
		Min.	Typ.	Max.		
Active Shut Down Voltage	$V_{ACTSD}^{1)}$	–	–	2.0	V	$I_{OUT} = -200 \text{ mA}$ , $V_{CC2}$ open

1) With reference to VEE2

### 5.4.9 Two-level Turn-off

Table 5-12 Two-level Turn-off

Parameter	Symbol	Values			Unit	Note
		Min.	Typ.	Max.		
External reference voltage range (Zener-Diode)	$V_{ZDIODE}$	7.5	–	$V_{CC2}-0.5$	V	–
Reference Voltage for setting two-level delay time	$V_{TLSET}$	6.6	7	7.3	V	–
Current for setting two-level delay time and external reference voltage (Zener-Diode)	$I_{TLSET}$	420	500	550	$\mu\text{A}$	$V_{TLSET} = 10 \text{ V}$
External Capacitance Range	$C_{TLSET}$	0	–	220	pF	–

## Insulation Characteristics

### 6 Insulation Characteristics

Insulation characteristics are guaranteed only within the safety maximum ratings which must be ensured by protective circuits in application. Surface mount classification is class A in accordance with CECC00802.

This coupler is suitable for “basic insulation” only within the safety ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits.

#### 6.1 Certified according to DIN EN 60747-5-2 (VDE 0884 Teil 2): 2003-01. Basic Insulation

**Table 6-1** Certified according to DIN EN 60747-5-2

Description	Symbol	Characteristic	Unit
Installation classification per EN 60664-1, Table 1 for rated mains voltage $\leq 150 V_{RMS}$ for rated mains voltage $\leq 300 V_{RMS}$ for rated mains voltage $\leq 600 V_{RMS}$		I-IV I-III I-II	–
Climatic Classification		40/125/21	–
Pollution Degree (EN 60664-1)		2	–
Minimum External Clearance	CLR	8	mm
Minimum External Creepage	CPG	8	mm
Minimum Comparative Tracking Index	CTI	175	–
Maximum Repetitive Insulation Voltage	$V_{IORM}$	1420	$V_{PEAK}$
Highest Allowable Overvoltage	$V_{IOTM}$	6000	$V_{PEAK}$
Maximum Surge Insulation Voltage	$V_{IOSM}$	6000	V

#### 6.2 Recognized under UL 1577

**Table 6-2** Recognized under UL 1577

Description	Symbol	Characteristic	Unit
Insulation Withstand Voltage / 1 min	$V_{ISO}$	3750	$V_{rms}$
Insulation Test Voltage / 1 s	$V_{ISO}$	4500	$V_{rms}$

#### 6.3 Reliability

For Qualification Report please contact your local Infineon Technologies office.

## Timing Diagrams

### 7 Timing Diagrams

All diagrams related to the Two-level switch-off feature

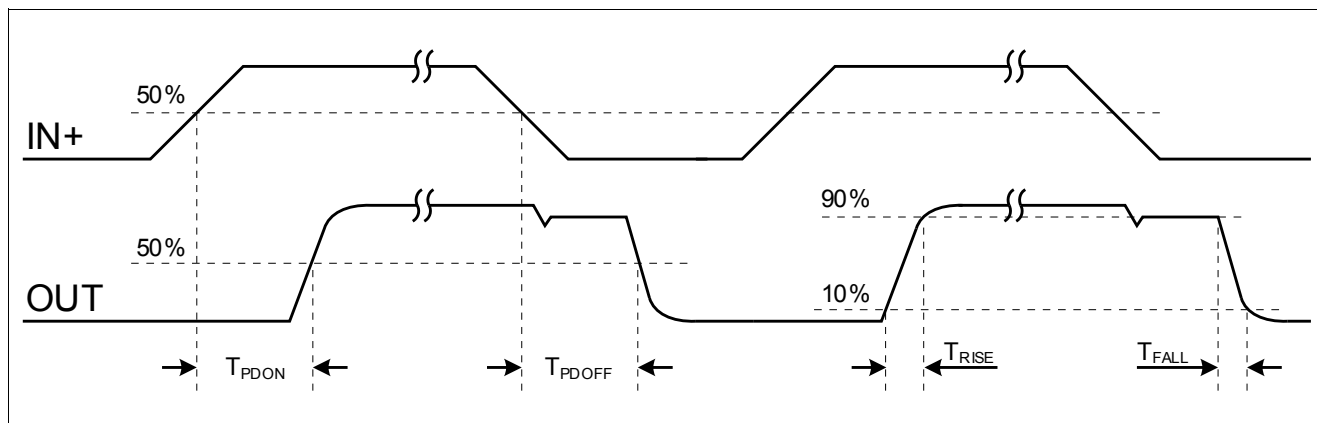


Figure 7-1 Propagation Delay, Rise and Fall Time

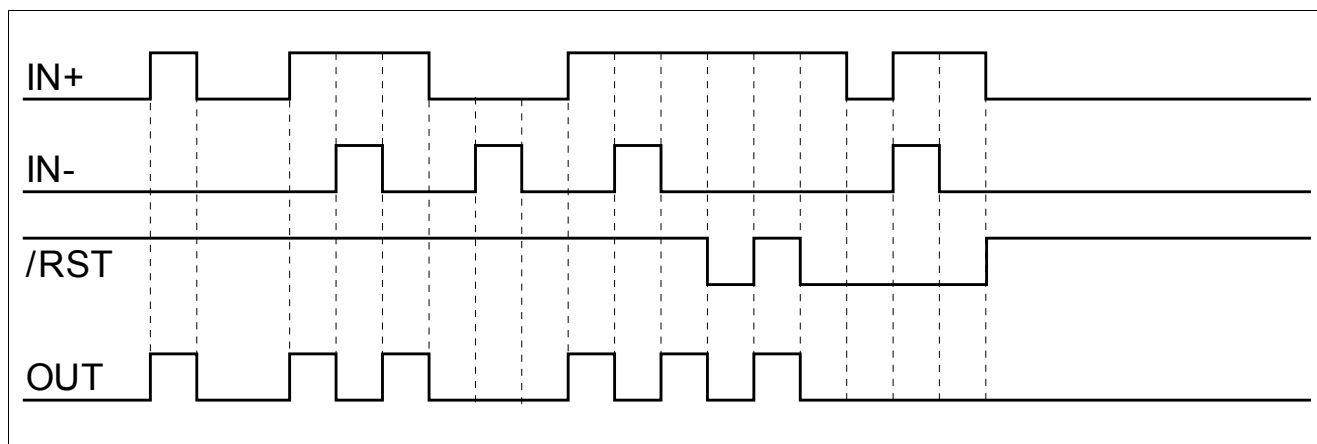


Figure 7-2 Principle Switching Behavior

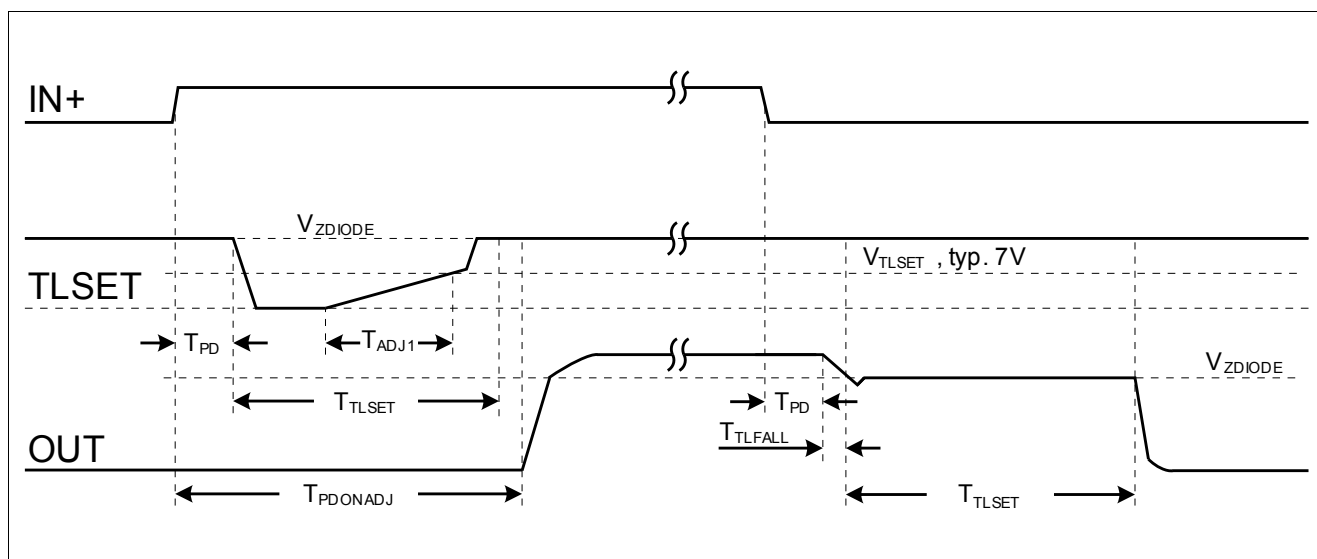


Figure 7-3 Typical Switching Behavior

Timing Diagrams

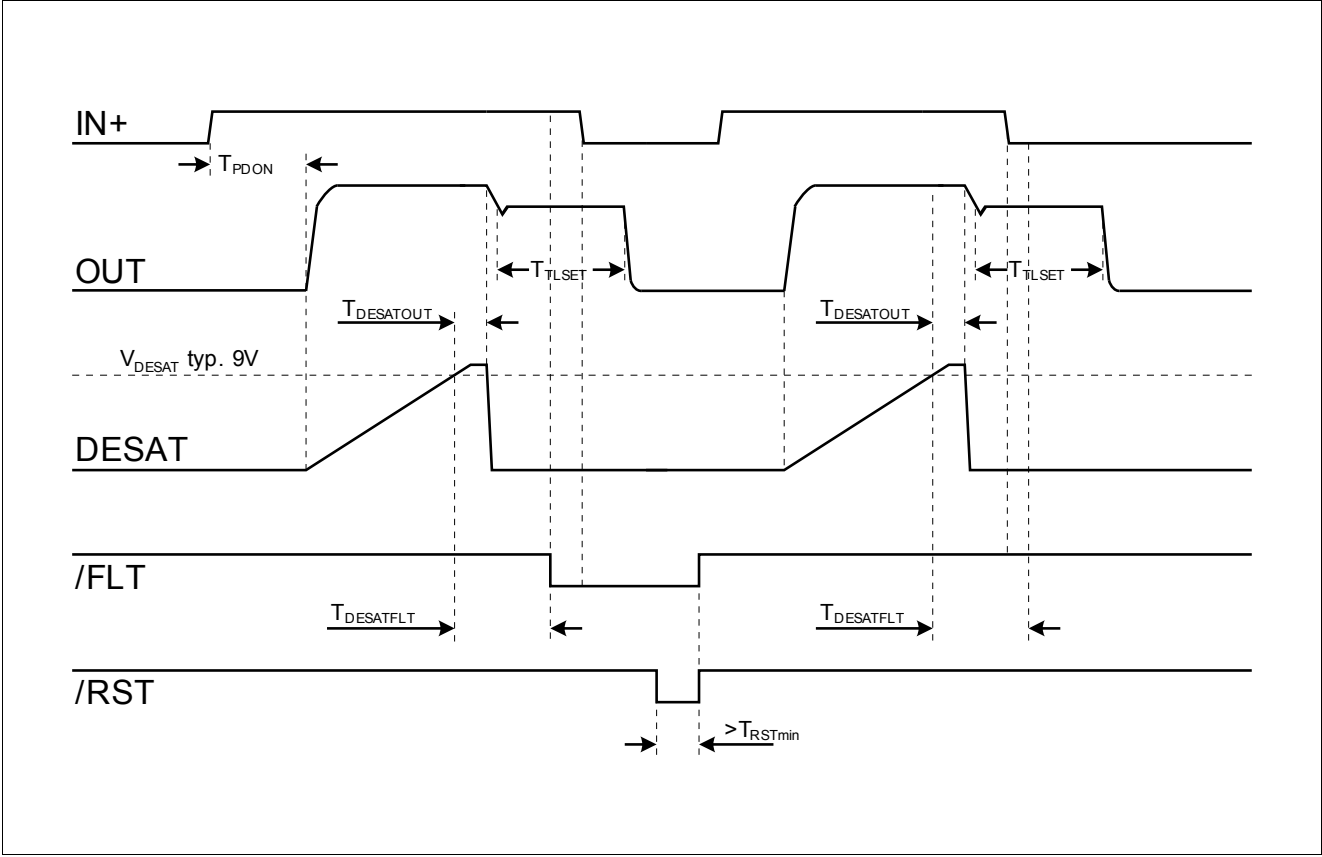


Figure 7-4 DESAT Switch-OFF Behavior

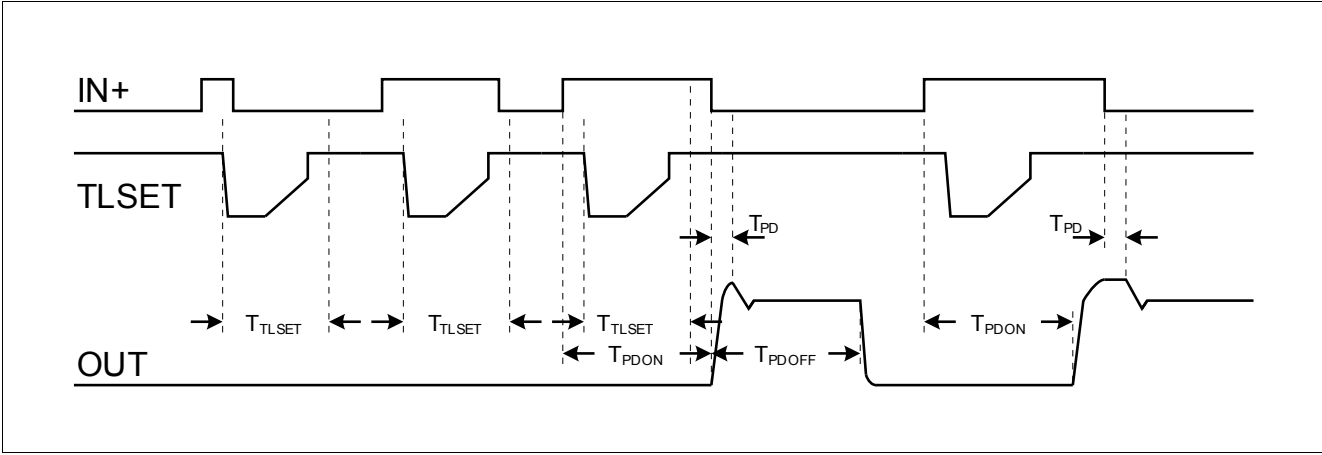


Figure 7-5 Short Switch ON Pulses

Timing Diagrams

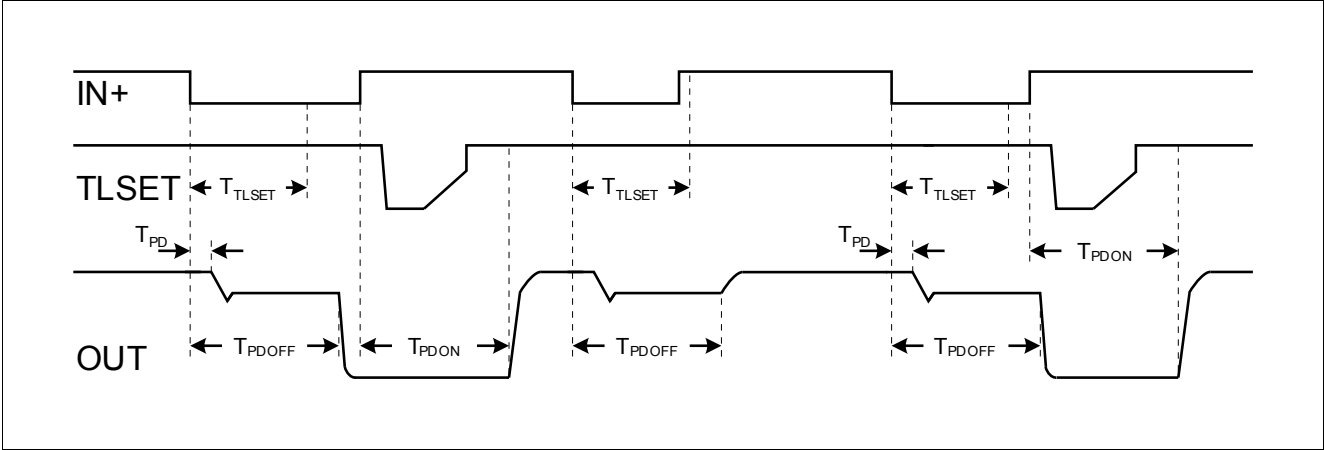


Figure 7-6 Short Switch OFF Pulses

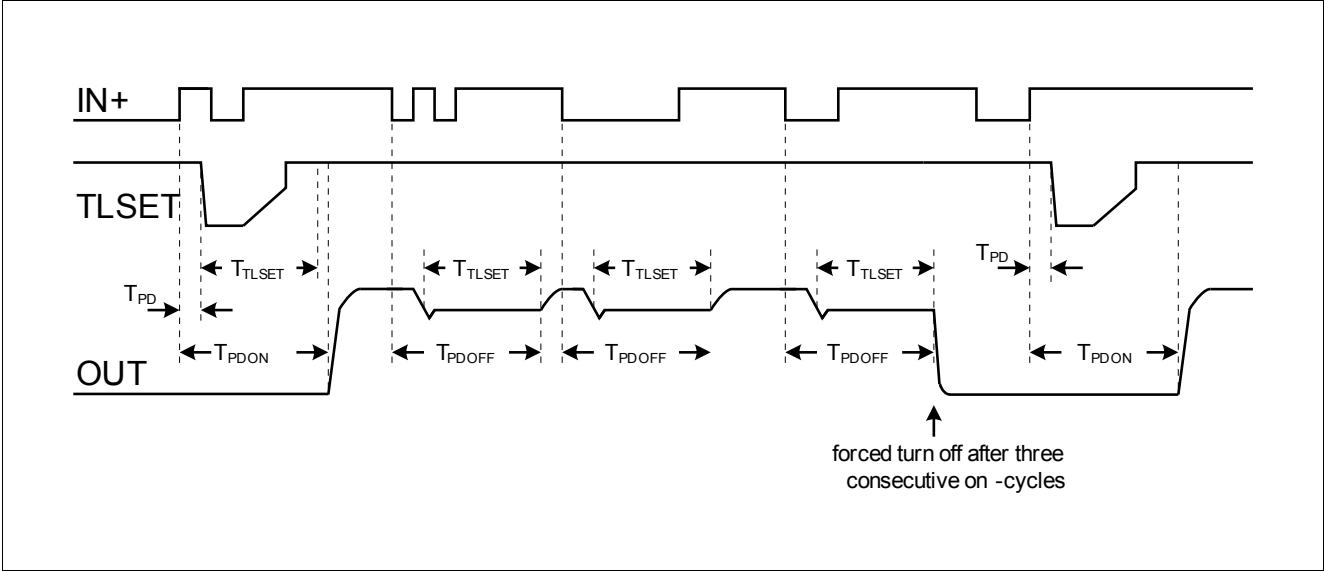


Figure 7-7 Short Switch OFF Pulses, Ringing Suppression



Timing Diagrams

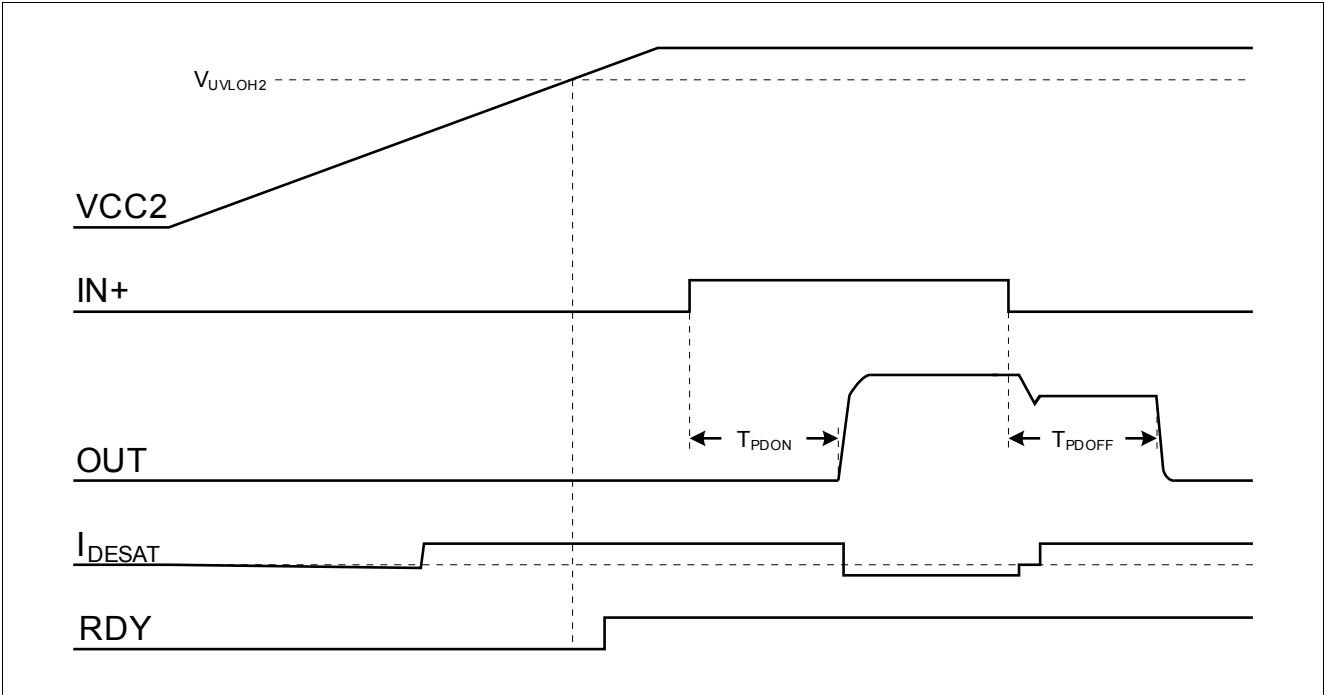


Figure 7-8 VCC2 Ramp Up

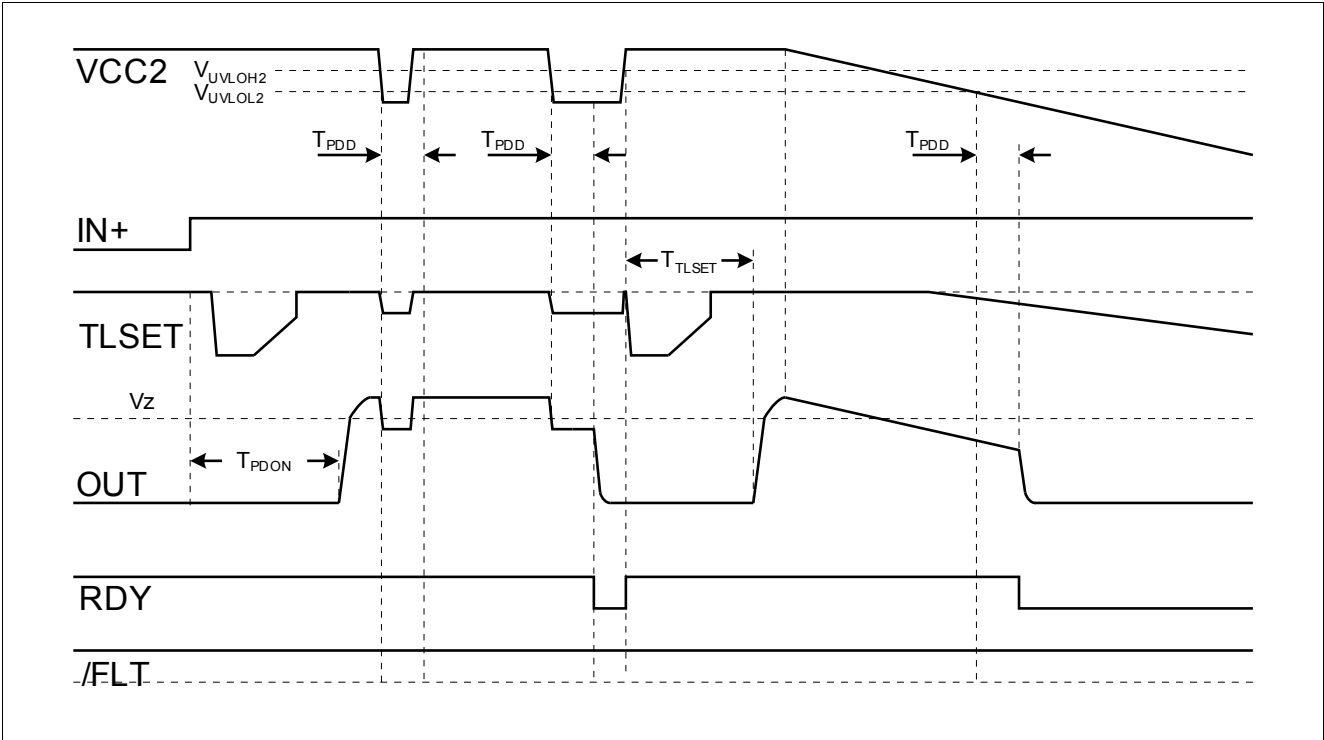


Figure 7-9 VCC2 Ramp Down and VCC2 Drop

Timing Diagrams

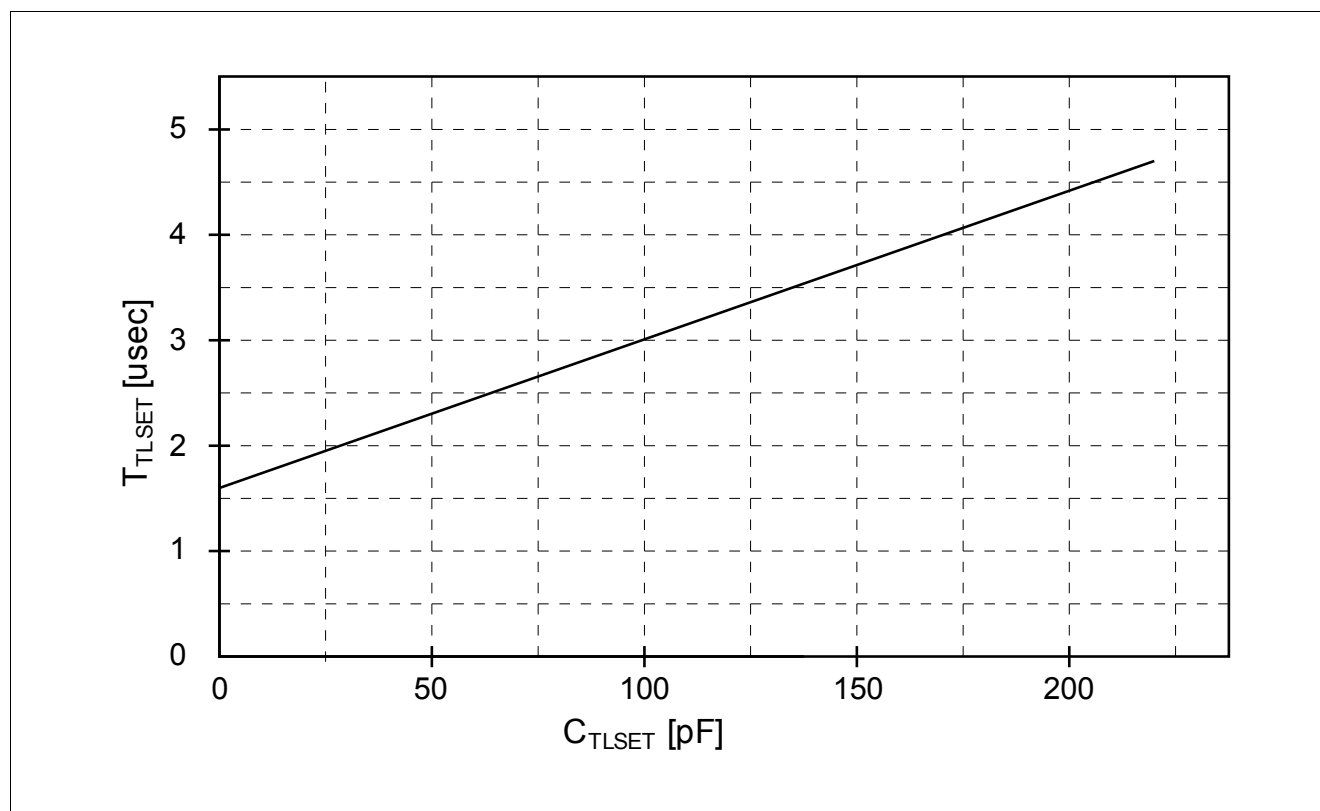


Figure 7-10 Typical  $T_{TLSET}$  Time over  $C_{TLSET}$  Capacitance

## 8 Package Outlines

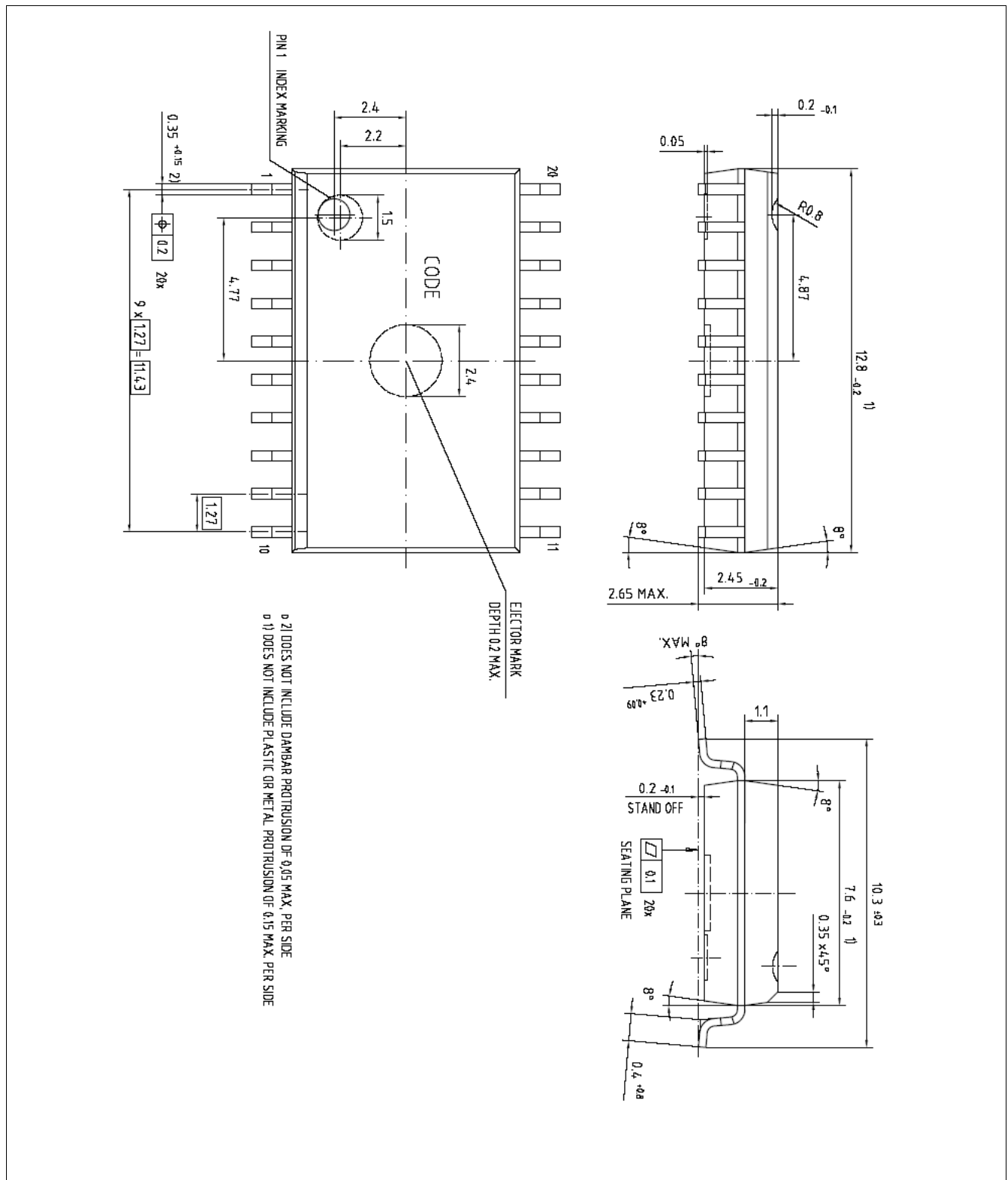
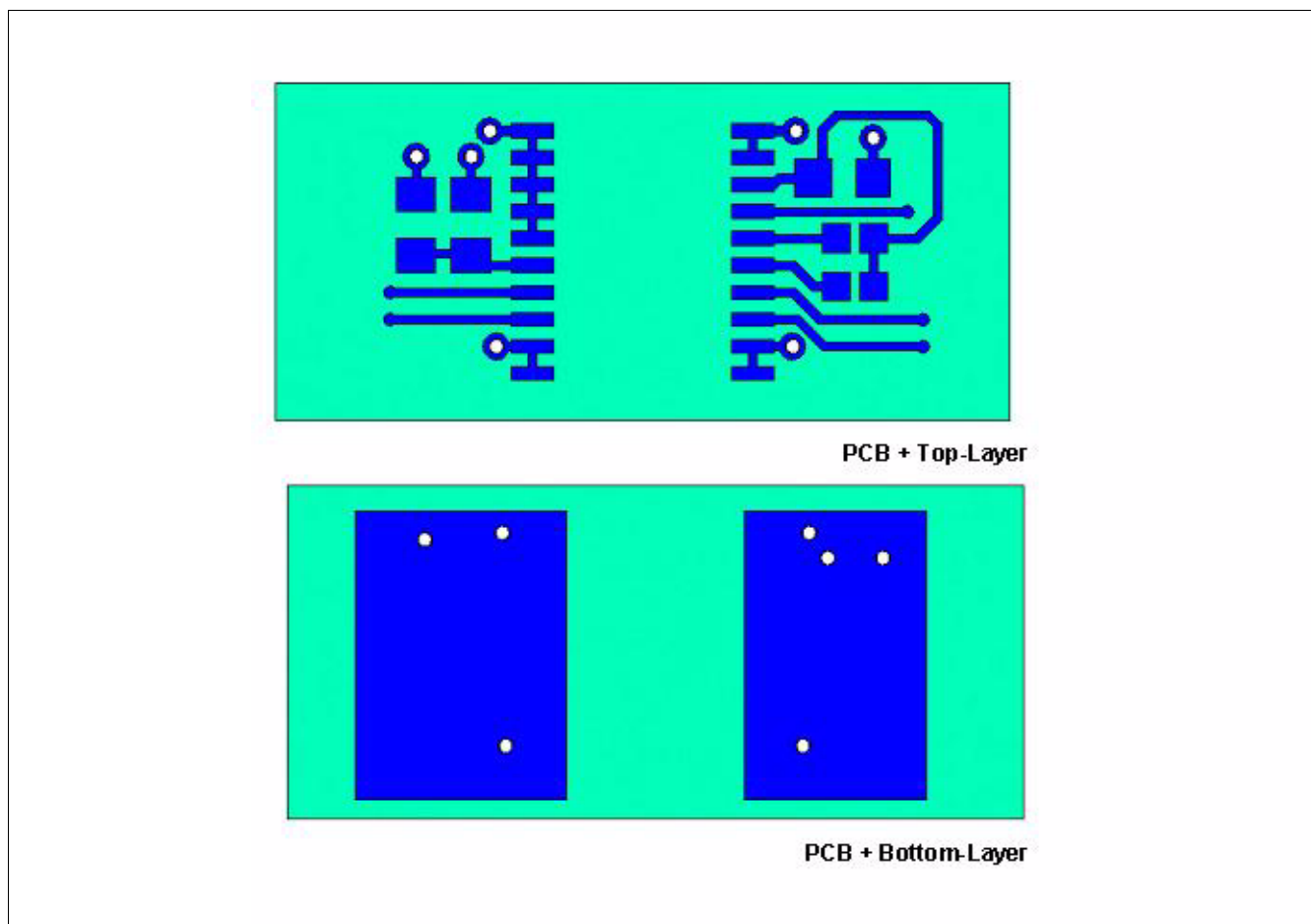


Figure 8-1 PG-DSO-20 (Plastic (Green) Dual Small Outline Package)

## 9 Application Notes

### 9.1 Reference Layout for Thermal Data

The PCB layout shown in **Figure 9-1** represents the reference layout used for the thermal characterisation. Pins 11, 12, 19 and 20 (GND1) and pins 1, 2, 9 and 10 (VEE2) require ground plane connections for achieving maximum power dissipation. The 1ED020I12FTA is conceived to dissipate most of the heat generated through this pins.



**Figure 9-1** Reference Layout for Thermal Data (Copper thickness 102 µm)

### 9.2 Printed Circuit Board Guidelines

Following factors should be taken into account for an optimum PCB layout.

- Sufficient spacing should be kept between high voltage isolated side and low voltage side circuits.
- The same minimum distance between two adjacent high-side isolated parts of the PCB should be maintained to increase the effective isolation and reduce parasitic coupling.
- In order to ensure low supply ripple and clean switching signals, bypass capacitor trace lengths should be kept as short as possible.
- Lowest trace length for VEE2 to GND2 decoupling could be achieved with capacitor closed to pins 2 and 4.

## Revision History

Page or Item	Subjects (major changes since previous revision)
<b>Rev. 3.0, 2016-04-05</b>	
All	Update latest template
<a href="#">Page 8</a>	removed Target Application Figure
<a href="#">Page 14</a>	Editorial changes, typos: - Symbol changed from Vmax2 to Vcc2 in Gate driver output - Pin CLAMP voltage unit changed from °C to V - Desaturation protection filter time changed
<a href="#">Page 6</a>	Updated Block Diagram
<a href="#">Page 14</a> , <a href="#">Page 15</a> , <a href="#">Page 16</a> , <a href="#">Page 17</a> , <a href="#">Page 18</a> , <a href="#">Page 19</a> , <a href="#">Page 20</a> , <a href="#">Page 21</a>	removed "Test Condition" from table header

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