1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings(†)

VCC 7.0V

All inputs and outputs w.r.t. VSS .... -0.6V to VCC +1.0V

Storage temperature ....-65°C to +150°C

Ambient temperature with power applied ....-65°C to +125°C

ESD protection on all pins ....≥ 4 kV

† NOTICE: Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

TABLE 1-1: DC CHARACTERISTICS

All parameters apply across the specified operating ranges unless otherwise noted.	VCC = +4.5V to +5.5V Commercial (C): TA = 0°C to +70°C Industrial (I): TA = -40°C to +85°C Automotive (E): TA = -40°C to +125°C				
Parameter	**Symbol**	**Min.**	**Max.**	**Units**	**Conditions**
SCL and SDA pins:					
High-level input voltage	VIH	0.7 VCC	—	V	
Low-level input voltage	VIL		.3 VCC	V	
Hysteresis of Schmitt Trigger inputs	VHYS	0.05 VCC	—	V	**(Note)**
Low-level output voltage	VOL		.40	V	IOL = 3.0 mA, VCC = 4.5V
Input leakage current	ILI	—	±1	µA	VIN = VSS or VCC, WP = Vss
Output leakage current	ILO	—	±1	µA	VOUT = VSS or VCC
Pin capacitance (all inputs/outputs)	CIN, COUT	—	10	pF	VCC = 5.0V **(Note)** TA = 25°C, f = 1 MHz
Operating current	ICC Read	—	1	mA	VCC = 5.5V, SCL = 400 kHz
	ICC Write	—	3	mA	VCC = 5.5V
Standby current	ICCS	—	50	µA	VCC = 5.5V, SDA = SCL = VCC WP = VSS

Note: This parameter is periodically sampled and not 100% tested.

TABLE 1-2: AC CHARACTERISTICS

All parameters apply across the specified operating ranges unless otherwise noted.	Vcc = 4.5V to 5.5V Commercial (C): TA- = 0°C to +70°C Industrial (I): TA- = -40°C to +85°C Automotive (E): TA- = -40°C to +125°C

Parameter	Symbol	Tamb > +85°C		-40°C ≤ Tamb ≤ +85°C		Units	Remarks
		Min.	Max.	Min.	Max.		
Clock frequency	FCLK	—	100	—	400	kHz	
Clock high time	THIGH	4000	—	600	—	ns	
Clock low time	TLOW	4700	—	1300	—	ns	
SDA and SCL rise time	TR	—	1000	—	300	ns	**(Note 1)**
SDA and SCL fall time	TF	—	300	—	300	ns	**(Note 1)**
Start condition hold time	THD:STA	4000	—	600	—	ns	After this period the first clock pulse is generated
Start condition setup time	TSU:STA	4700	—	600	—	ns	Only relevant for repeated Start condition
Data input hold time	THD:DAT	0	—	0	—	ns	**(Note 2)**
Data input setup time	TSU:DAT	250	—	100	—	ns	
Stop condition setup time	TSU:STO	4000	—	600	—	ns	
Output valid from clock	TAA	—	3500	—	900	ns	**(Note 2)**
Bus free time	TBUF	4700	—	1300	—	ns	Time the bus must be free before a new transmission can start
Output fall time from VIH minimum to VIL maximum	TOF	—	250	20 +0.1 C_B	250	ns	**(Note 1)**, $C_B \leq 100$ pF
Input filter spike suppression (SDA and SCL pins)	TSP	—	50	—	50	ns	**(Note 3)**
Write cycle time	TWR	—	1.5	—	1	ms	Byte or Page mode
Endurance		1M	—	1M	—	cycles	25°C, VCC = 5.0V, Block mode **(Note 4)**

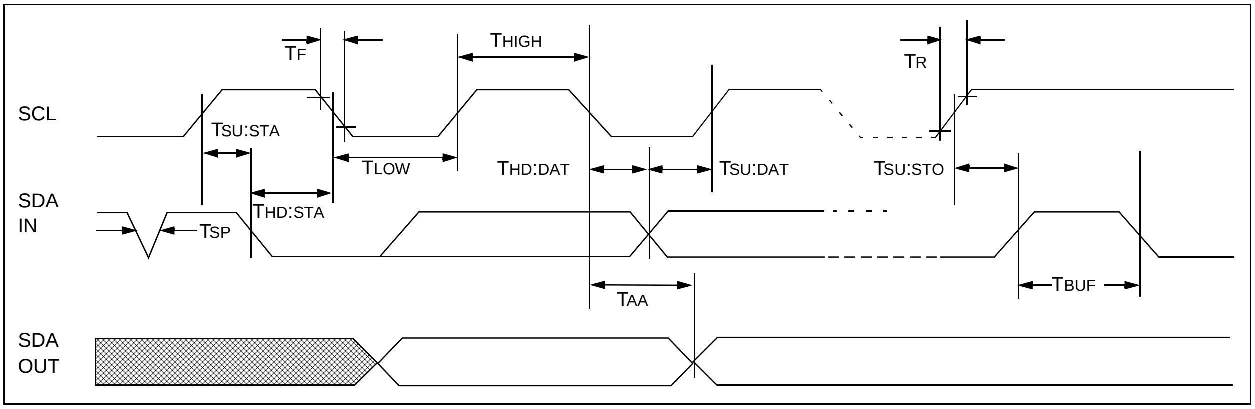
Note 1: Not 100% tested. C_B = total capacitance of one bus line in pF.

2: As a transmitter, the device must provide an internal minimum delay time to bridge the undefined region (minimum 300 ns) of the falling edge of SCL to avoid unintended generation of Start or Stop conditions.

3: The combined TSP and VHYS specifications are due to Schmitt Trigger inputs which provide improved noise spike suppression. This eliminates the need for a TI specification for standard operation.

4: This parameter is not tested but ensured by characterization. For endurance estimates in a specific application, please consult the Total Endurance™ Model which can be obtained from Microchip's web site at www.microchip.com.

FIGURE 1-1: BUS TIMING DATA



2.0 PIN DESCRIPTIONS

2.1 SDA Serial Data

This is a bidirectional pin used to transfer addresses and data into and data out of the device. It is an open drain terminal, therefore the SDA bus requires a pull-up resistor to VCC (typical 10 kΩ for 100 kHz, 2 kΩ for 400 kHz).

For normal data transfer SDA is allowed to change only during SCL low. Changes during SCL high are reserved for indicating the Start and Stop conditions.

2.2 SCL Serial Clock

This input is used to synchronize the data transfer from and to the device.

2.3 A0, A1, A2

The levels on these inputs are compared with the corresponding bits in the slave address. The chip is selected if the compare is true.

Up to eight 24C01C devices may be connected to the same bus by using different Chip Select bit combinations. These inputs must be connected to either VCC or VSS.

2.4 Test

This pin is utilized for testing purposes only. It may be tied high, tied low or left floating.

2.5 Noise Protection

The 24C01C employs a VCC threshold detector circuit which disables the internal erase/write logic if the VCC is below 3.8 volts at nominal conditions.

The SCL and SDA inputs have Schmitt Trigger and filter circuits which suppress noise spikes to assure proper device operation even on a noisy bus.

3.0 FUNCTIONAL DESCRIPTION

The 24C01C supports a bidirectional 2-wire bus and data transmission protocol. A device that sends data onto the bus is defined as transmitter, and a device receiving data as receiver. The bus has to be controlled by a master device which generates the Serial Clock (SCL), controls the bus access, and generates the Start and Stop conditions, while the 24C01C works as slave. Both master and slave can operate as transmitter or receiver, but the master device determines which mode is activated.

4.0 BUS CHARACTERISTICS

The following **bus protocol** has been defined:

- Data transfer may be initiated only when the bus is not busy.
- During data transfer, the data line must remain stable whenever the clock line is high. Changes in the data line while the clock line is high will be interpreted as a Start or Stop condition.

Accordingly, the following bus conditions have been defined (Figure 4-1).

4.1 Bus Not Busy (A)

Both data and clock lines remain high.

4.2 Start Data Transfer (B)

A high-to-low transition of the SDA line while the clock (SCL) is high determines a Start condition. All commands must be preceded by a Start condition.

4.3 Stop Data Transfer (C)

A low-to-high transition of the SDA line while the clock (SCL) is high determines a Stop condition. All operations must be ended with a Stop condition.

4.4 Data Valid (D)

The state of the data line represents valid data when, after a Start condition, the data line is stable for the duration of the high period of the clock signal.

The data on the line must be changed during the low period of the clock signal. There is one bit of data per clock pulse.

Each data transfer is initiated with a Start condition and terminated with a Stop condition. The number of the data bytes transferred between the Start and Stop conditions is determined by the master device and is theoretically unlimited, although only the last sixteen will be stored when doing a write operation. When an overwrite does occur it will replace data in a first-in first-out fashion.

4.5 Acknowledge

Each receiving device, when addressed, is required to generate an acknowledge after the reception of each byte. The master device must generate an extra clock pulse which is associated with this Acknowledge bit.

Note: The 24C01C does not generate any Acknowledge bits if an internal programming cycle is in progress.

The device that acknowledges has to pull down the SDA line during the Acknowledge clock pulse in such a way that the SDA line is stable low during the high period of the acknowledge related clock pulse. Of course, setup and hold times must be taken into account. A master must signal an end of data to the slave by not generating an Acknowledge bit on the last byte that has been clocked out of the slave. In this case, the slave must leave the data line high to enable the master to generate the Stop condition (Figure 4-2).

FIGURE 4-1: DATA TRANSFER SEQUENCE ON THE SERIAL BUS CHARACTERISTICS

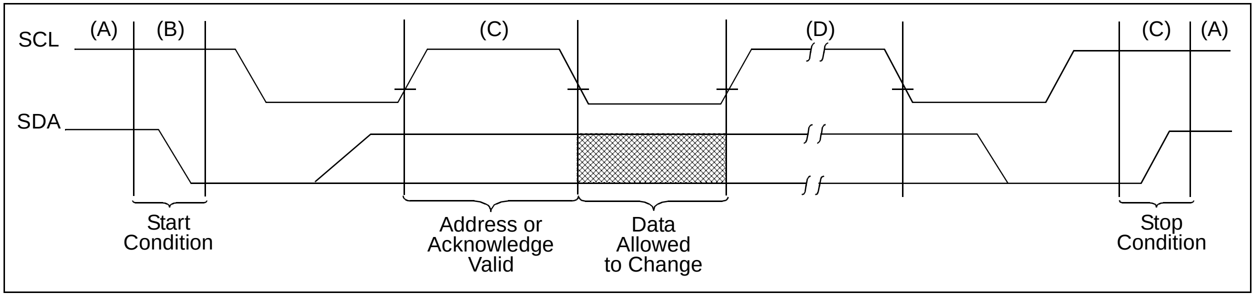
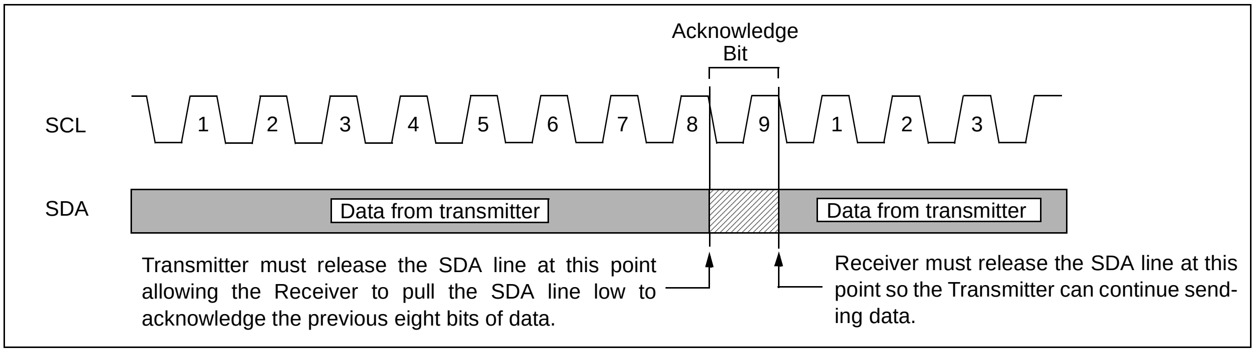


FIGURE 4-2: ACKNOWLEDGE TIMING



Transmitter must release the SDA line at this point allowing the Receiver to pull the SDA line low to acknowledge the previous eight bits of data.

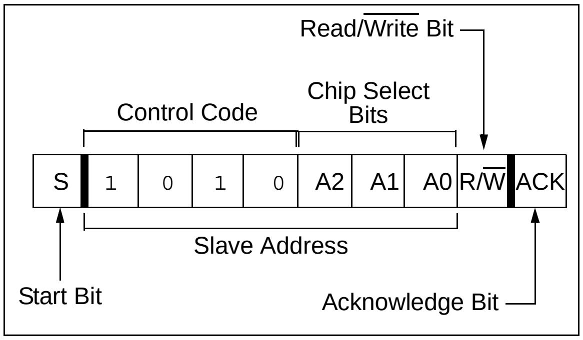
Receiver must release the SDA line at this point so the Transmitter can continue sending data.

5.0 DEVICE ADDRESSING

A control byte is the first byte received following the Start condition from the master device (Figure 5-1). The control byte consists of a four-bit control code; for the 24C01C this is set as ‘`1010`’ binary for read and write operations. The next three bits of the control byte are the Chip Select bits (A2, A1, A0). The Chip Select bits allow the use of up to eight 24C01C devices on the same bus and are used to select which device is accessed. The Chip Select bits in the control byte must correspond to the logic levels on the corresponding A2, A1 and A0 pins for the device to respond. These bits are in effect the three Most Significant bits of the word address.

The last bit of the control byte defines the operation to be performed. When set to a ‘`1`’ a read operation is selected, and when set to a ‘`0`’ a write operation is selected. Following the Start condition, the 24C01C monitors the SDA bus checking the control byte being transmitted. Upon receiving a ‘`1010`’ code and appropriate Chip Select bits, the slave device outputs an Acknowledge signal on the SDA line. Depending on the state of the R/$\overline{W}$ bit, the 24C01C will select a read or write operation.

FIGURE 5-1: CONTROL BYTE FORMAT



5.1 Contiguous Addressing Across Multiple Devices

The Chip Select bits A2, A1, A0 can be used to expand the contiguous address space for up to 8K bits by adding up to eight 24C01C devices on the same bus. In this case, software can use A0 of the control byte as address bit A8, A1 as address bit A9, and A2 as address bit A10. It is not possible to write or read across device boundaries.

6.0 WRITE OPERATIONS

6.1 Byte Write

Following the Start signal from the master, the device code(4 bits), the Chip Select bits (3 bits), and the R/$\overline{W}$ bit, which is a logic low, is placed onto the bus by the master transmitter. The device will acknowledge this control byte during the ninth clock pulse. The next byte transmitted by the master is the word address and will be written into the Address Pointer of the 24C01C. After receiving another Acknowledge signal from the 24C01C the master device will transmit the data word to be written into the addressed memory location. The 24C01C acknowledges again and the master generates a Stop condition. This initiates the internal write cycle, and during this time the 24C01C will not generate Acknowledge signals (Figure 6-1).

6.2 Page Write

The write control byte, word address and the first data byte are transmitted to the 24C01C in the same way as in a byte write. But instead of generating a Stop condition, the master transmits up to 15 additional data bytes to the 24C01C which are temporarily stored in the on-chip page buffer and will be written into the memory after the master has transmitted a Stop condition.

After the receipt of each word, the four lower order Address Pointer bits are internally incremented by one. The higher order four bits of the word address remains constant. If the master should transmit more than 16 bytes prior to generating the Stop condition, the address counter will roll over and the previously received data will be overwritten. As with the byte write operation, once the Stop condition is received an internal write cycle will begin (Figure 6-2).

Note:	Page write operations are limited to writing bytes within a single physical page, regardless of the number of bytes actually being written. Physical page boundaries start at addresses that are integer multiples of the page buffer size (or 'page size') and end at addresses that are integer multiples of [page size – 1]. If a Page Write command attempts to write across a physical page boundary, the result is that the data wraps around to the beginning of the current page (overwriting data previously stored there), instead of being written to the next page as might be expected. It is therefore necessary for the application software to prevent page write operations that would attempt to cross a page boundary.

FIGURE 6-1: BYTE WRITE

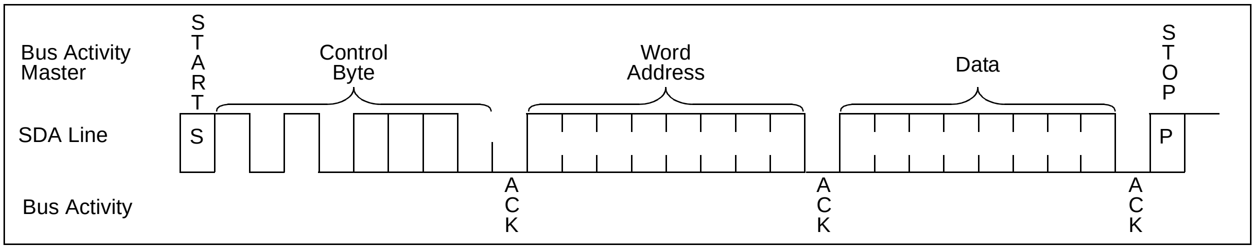
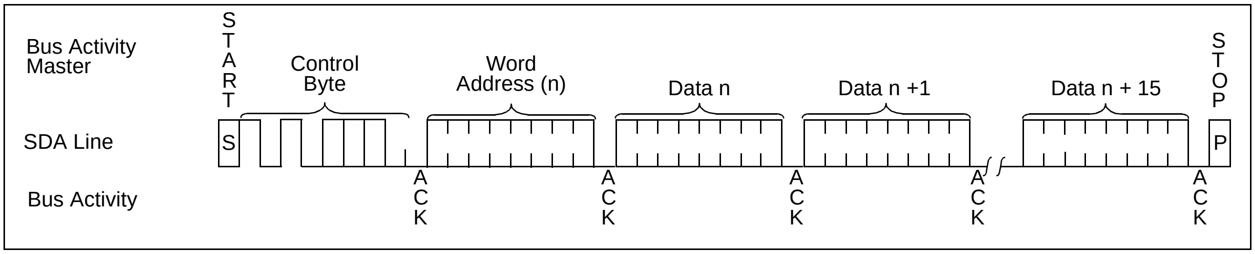


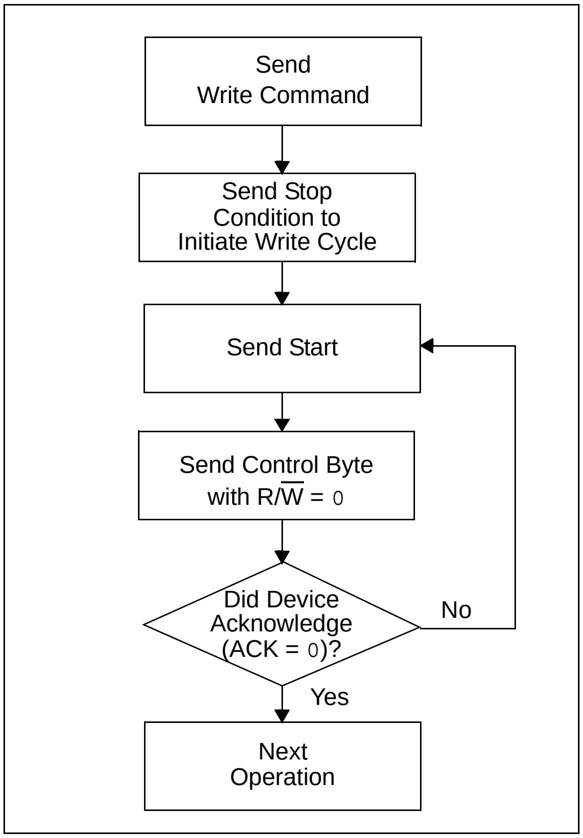
FIGURE 6-2: PAGE WRITE



7.0 ACKNOWLEDGE POLLING

Since the device will not acknowledge during a write cycle, this can be used to determine when the cycle is complete (this feature can be used to maximize bus throughput). Once the Stop condition for a Write command has been issued from the master, the device initiates the internally timed write cycle. ACK polling can be initiated immediately. This involves the master sending a Start condition followed by the control byte for a Write command ($R/\overline{W}$ = 0). If the device is still busy with the write cycle, then no ACK will be returned. If no ACK is returned, then the Start bit and control byte must be re-sent. If the cycle is complete, then the device will return the ACK and the master can then proceed with the next Read or Write command. See Figure 7-1 for flow diagram.

FIGURE 7-1: ACKNOWLEDGE POLLING FLOW



8.0 READ OPERATIONS

Read operations are initiated in the same way as write operations with the exception that the $R/\overline{W}$ bit of the slave address is set to one. There are three basic types of read operations: current address read, random read and sequential read.

8.1 Current Address Read

The 24C01C contains an address counter that maintains the address of the last word accessed, internally incremented by one. Therefore, if the previous read access was to address n, the next current address read operation would access data from address n + 1. Upon receipt of the slave address with the $R/\overline{W}$ bit set to one, the 24C01C issues an acknowledge and transmits the eight-bit data word. The master will not acknowledge the transfer, but does generate a Stop condition and the 24C01C discontinues transmission (Figure 8-1).

8.2 Random Read

Random read operations allow the master to access any memory location in a random manner. To perform this type of read operation, first the word address must be set. This is done by sending the word address to the 24C01C as part of a write operation.

After the word address is sent, the master generates a Start condition following the acknowledge. This terminates the write operation, but not before the internal Address Pointer is set. Then the master issues the control byte again but with the $R/\overline{W}$ bit set to a one. The 24C01C will then issue an acknowledge and transmits the eight bit data word. The master will not acknowledge the transfer, but does generate a Stop condition and the 24C01C discontinues transmission (Figure 8-2). After this command, the internal address counter will point to the address location following the one that was just read.

8.3 Sequential Read

Sequential reads are initiated in the same way as a random read except that after the 24C01C transmits the first data byte, the master issues an acknowledge as opposed to a Stop condition in a random read. This directs the 24C01C to transmit the next sequentially addressed 8-bit word (Figure 8-3).

To provide sequential reads the 24C01C contains an internal Address Pointer which is incremented by one at the completion of each operation. This Address Pointer allows the entire memory contents to be serially read during one operation. The internal Address Pointer will automatically roll over from address 7F to address 00.

FIGURE 8-1: CURRENT ADDRESS READ

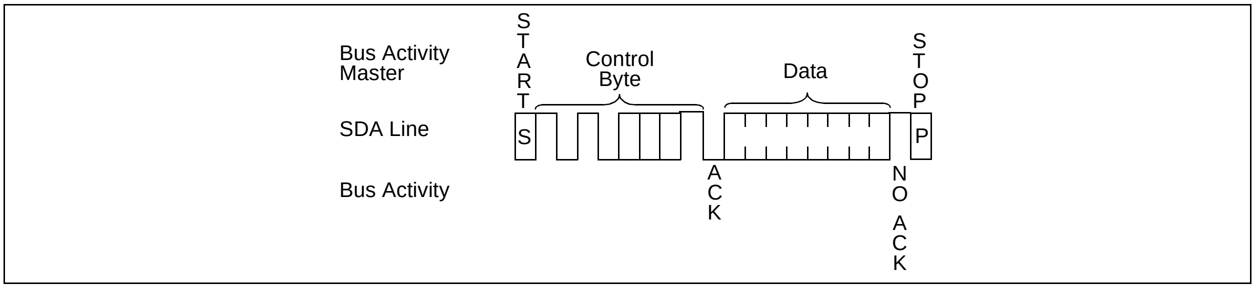


FIGURE 8-2: RANDOM READ

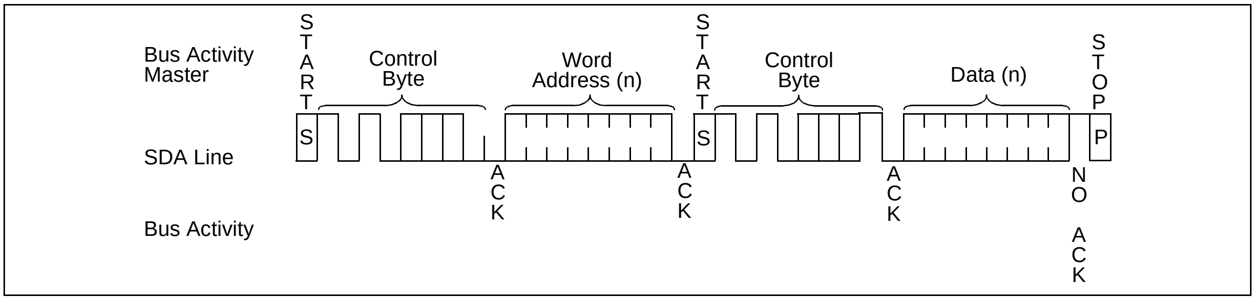
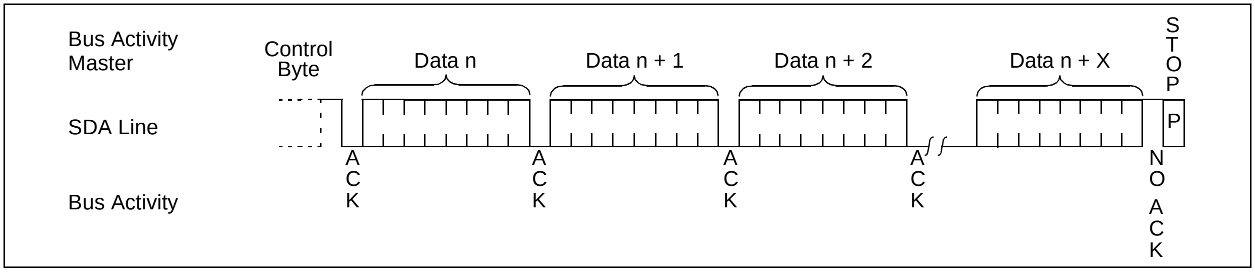


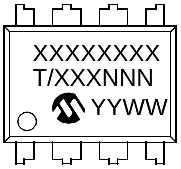
FIGURE 8-3: SEQUENTIAL READ



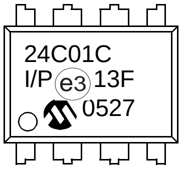
9.0 PACKAGING INFORMATION

9.1 Package Marking Information

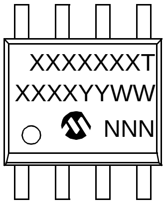
8-Lead PDIP (300 mil)



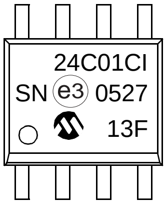
Example:



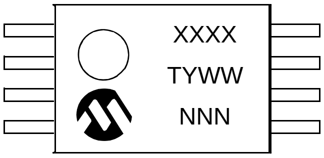
8-Lead SOIC (150 mil)



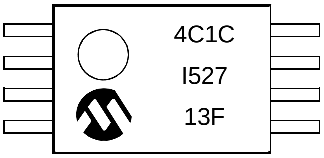
Example:



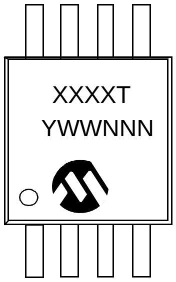
8-Lead TSSOP



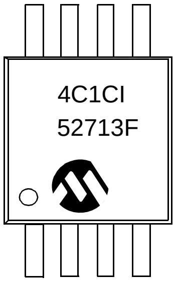
Example:



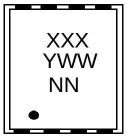
8-Lead MSOP



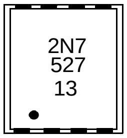
Example:



8-Lead 2x3 DFN



Example:



Part Number	1st Line Marking Codes			
	TSSOP	MSOP	DFN	
			I Temp.	E Temp.
24C01C	4C1C	4C1CT	2N7	2N8

Note: T = Temperature grade (I, E)

Legend:		
	XX...X	Part number or part number code
	T	Temperature (I, E)
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code (2 characters for small packages)
	e3	Pb-free JEDEC designator for Matte Tin (Sn)

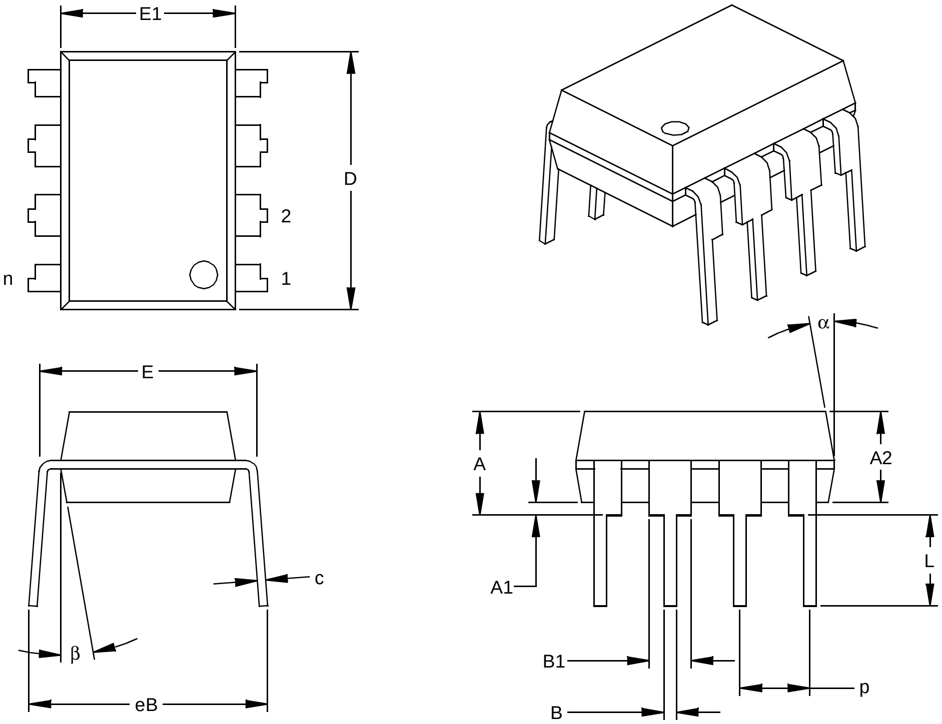
Note: For very small packages with no room for the Pb-free JEDEC designator e3, the marking will only appear on the outer carton or reel label.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

Note: Please visit www.microchip.com/Pbfree for the latest information on Pb-free conversion.

*****Standard OTP marking consists of Microchip part number, year code, week code, and traceability code.

8-Lead Plastic Dual In-line (P) – 300 mil (PDIP)

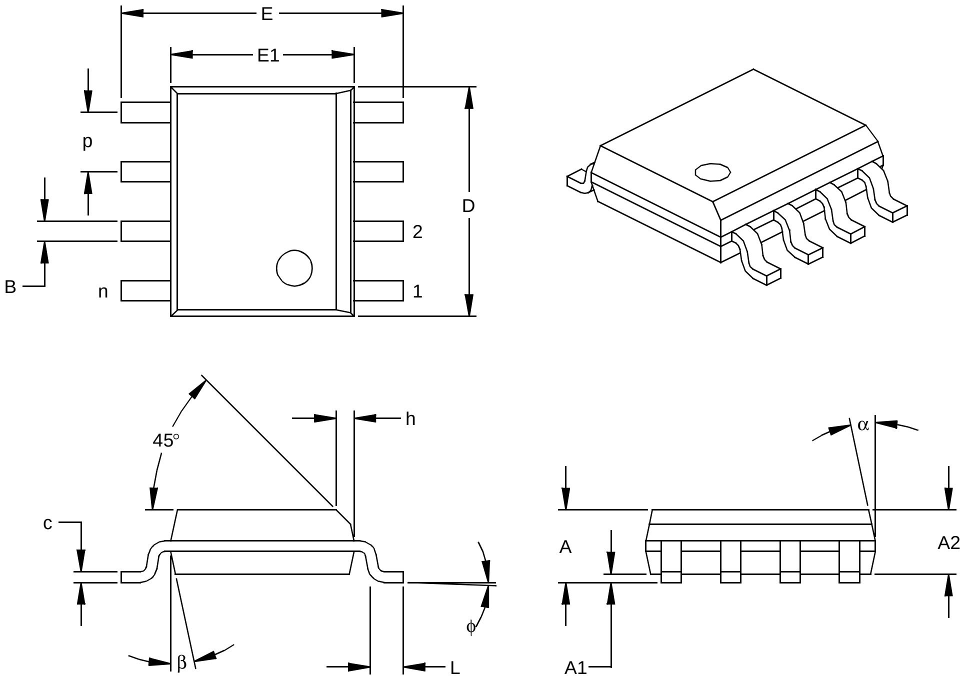


	Units	INCHES*			MILLIMETERS		
	Dimension Limits	MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		8			8	
Pitch	p		.100			2.54	
Top to Seating Plane	A	.140	.155	.170	3.56	3.94	4.32
Molded Package Thickness	A2	.115	.130	.145	2.92	3.30	3.68
Base to Seating Plane	A1	.015			0.38		
Shoulder to Shoulder Width	E	.300	.313	.325	7.62	7.94	8.26
Molded Package Width	E1	.240	.250	.260	6.10	6.35	6.60
Overall Length	D	.360	.373	.385	9.14	9.46	9.78
Tip to Seating Plane	L	.125	.130	.135	3.18	3.30	3.43
Lead Thickness	c	.008	.012	.015	0.20	0.29	0.38
Upper Lead Width	B1	.045	.058	.070	1.14	1.46	1.78
Lower Lead Width	B	.014	.018	.022	0.36	0.46	0.56
Overall Row Spacing §	eB	.310	.370	.430	7.87	9.40	10.92
Mold Draft Angle Top	α	5	10	15	5	10	15
Mold Draft Angle Bottom	β	5	10	15	5	10	15

* Controlling Parameter
§ Significant Characteristic

Notes:
Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010” (0.254mm) per side.
JEDEC Equivalent: MS-001
Drawing No. C04-018

8-Lead Plastic Small Outline (SN) – Narrow, 150 mil (SOIC)

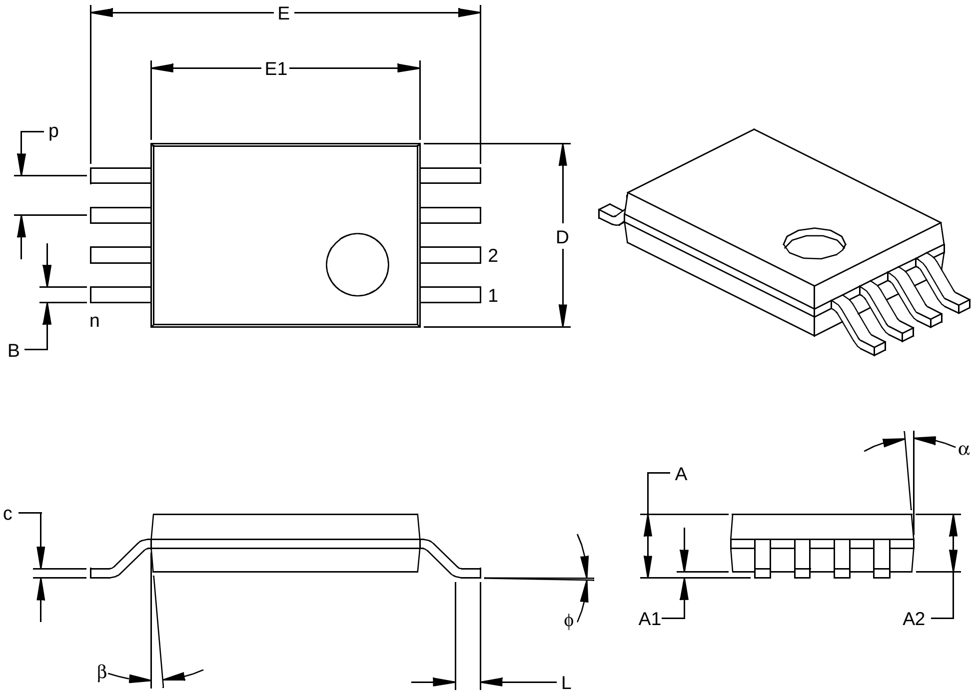


Units		INCHES*			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		8			8	
Pitch	p		.050			1.27	
Overall Height	A	.053	.061	.069	1.35	1.55	1.75
Molded Package Thickness	A2	.052	.056	.061	1.32	1.42	1.55
Standoff §	A1	.004	.007	.010	0.10	0.18	0.25
Overall Width	E	.228	.237	.244	5.79	6.02	6.20
Molded Package Width	E1	.146	.154	.157	3.71	3.91	3.99
Overall Length	D	.189	.193	.197	4.80	4.90	5.00
Chamfer Distance	h	.010	.015	.020	0.25	0.38	0.51
Foot Length	L	.019	.025	.030	0.48	0.62	0.76
Foot Angle	φ	0	4	8	0	4	8
Lead Thickness	c	.008	.009	.010	0.20	0.23	0.25
Lead Width	B	.013	.017	.020	0.33	0.42	0.51
Mold Draft Angle Top	α	0	12	15	0	12	15
Mold Draft Angle Bottom	β	0	12	15	0	12	15

* Controlling Parameter
§ Significant Characteristic

Notes:
Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010” (0.254mm) per side.
JEDEC Equivalent: MS-012
Drawing No. C04-057

8-Lead Plastic Thin Shrink Small Outline (ST) – 4.4 mm (TSSOP)

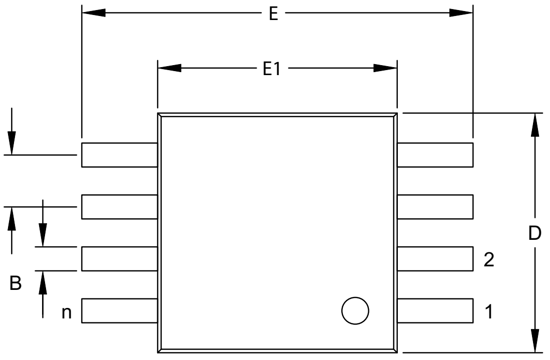


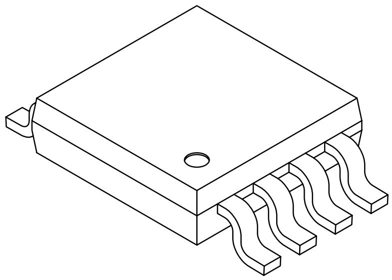
Units		INCHES			MILLIMETERS*		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		8			8	
Pitch	p		.026			0.65	
Overall Height	A			.043			1.10
Molded Package Thickness	A2	.033	.035	.037	0.85	0.90	0.95
Standoff §	A1	.002	.004	.006	0.05	0.10	0.15
Overall Width	E	.246	.251	.256	6.25	6.38	6.50
Molded Package Width	E1	.169	.173	.177	4.30	4.40	4.50
Molded Package Length	D	.114	.118	.122	2.90	3.00	3.10
Foot Length	L	.020	.024	.028	0.50	0.60	0.70
Foot Angle	φ	0	4	8	0	4	8
Lead Thickness	c	.004	.006	.008	0.09	0.15	0.20
Lead Width	B	.007	.010	.012	0.19	0.25	0.30
Mold Draft Angle Top	α	0	5	10	0	5	10
Mold Draft Angle Bottom	β	0	5	10	0	5	10

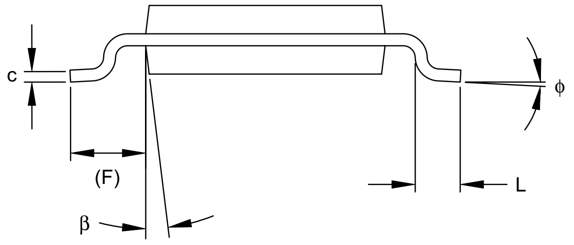
* Controlling Parameter
§ Significant Characteristic

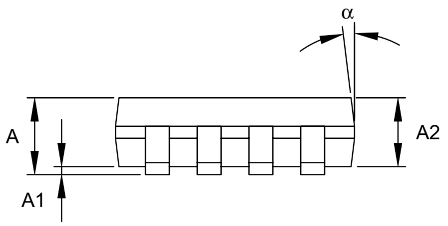
Notes:
Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .005" (0.127mm) per side.
JEDEC Equivalent: MO-153
Drawing No. C04-086

8-Lead Plastic Micro Small Outline Package (MS) (MSOP)









Units		INCHES			MILLIMETERS*		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n	8			8		
Pitch	p	.026 BSC			0.65 BSC		
Overall Height	A	-	-	.043	-	-	1.10
Molded Package Thickness	A2	.030	.033	.037	0.75	0.85	0.95
Standoff	A1	.000	-	.006	0.00	-	0.15
Overall Width	E	.193 TYP.			4.90 BSC		
Molded Package Width	E1	.118 BSC			3.00 BSC		
Overall Length	D	.118 BSC			3.00 BSC		
Foot Length	L	.016	.024	.031	0.40	0.60	0.80
Footprint (Reference)	F	.037 REF			0.95 REF		
Foot Angle	φ	0°	-	8°	0°	-	8°
Lead Thickness	c	.003	.006	.009	0.08	-	0.23
Lead Width	B	.009	.012	.016	0.22	-	0.40
Mold Draft Angle Top	α	5°	-	15°	5°	-	15°
Mold Draft Angle Bottom	β	5°	-	15°	5°	-	15°

*Controlling Parameter

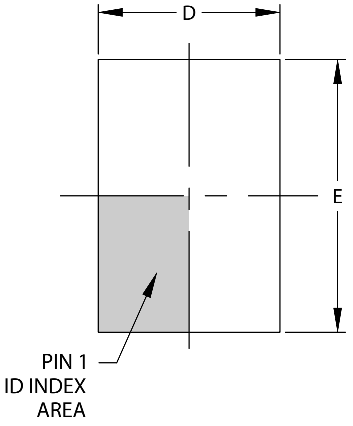
Notes:

Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" (0.254mm) per side.

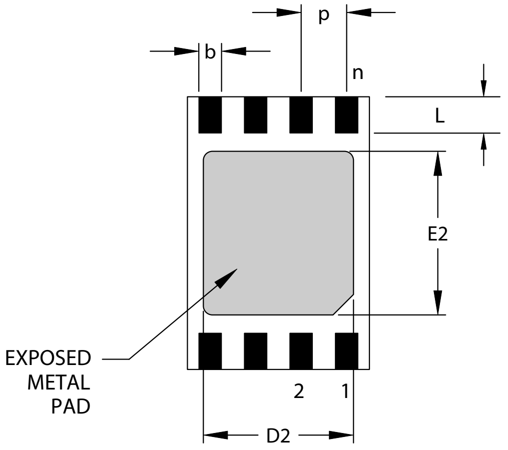
JEDEC Equivalent: MO-187

Drawing No. C04-111

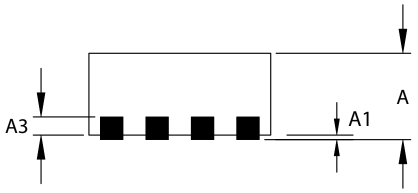
8-Lead Plastic Dual Flat No Lead Package (MC) 2x3x0.9 mm Body (DFN) – Saw Singulated

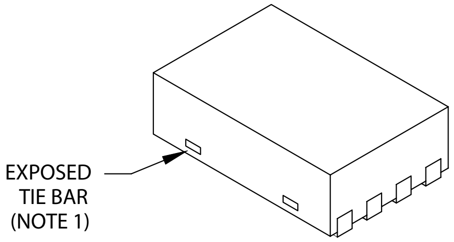


TOP VIEW



BOTTOM VIEW





Units		INCHES			MILLIMETERS*		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		8			8	
Pitch	p		.020 BSC			0.50 BSC	
Overall Height	A	.031	.035	.039	0.80	0.90	1.00
Standoff	A1	.000	.001	.002	0.00	0.02	0.05
Contact Thickness	A3		.008 REF.			0.20 REF.	
Overall Length	D		.079 BSC			2.00 BSC	
Exposed Pad Length (Note 3)	D2	.055	--	.064	1.39	--	1.62
Overall Width	E		.118 BSC			3.00 BSC	
Exposed Pad Width (Note 3)	E2	.047	--	.071	1.20	--	1.80
Contact Width	b	.008	.010	.012	0.20	0.25	0.30
Contact Length	L	.012	.016	.020	0.30	0.40	0.50

*Controlling Parameter

Notes:

1. Package may have one or more exposed tie bars at ends.
2. Pin 1 visual index feature may vary, but must be located within the hatched area.
3. Exposed pad dimensions vary with paddle size.
4. JEDEC equivalent: MO-229

Drawing No. C04-123

Revised 05/24/04

APPENDIX A: REVISION HISTORY

Revision D

Corrections to Section 1.0, Electrical Characteristics.

Revision E

Added DFN package.

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E = -40°C to +125°C

Package:
P = Plastic DIP (300 mil Body), 8-lead
SN = Plastic SOIC, (150 mil Body), 8-lead
ST = TSSOP (4.4 mm Body), 8-lead
MS = Plastic Micro Small Outline (MSOP), 8-lead
MC = 2x3 DFN, 8-lead

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