1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings (†)

V_{CC} 6.5V

All inputs and outputs w.r.t. V_{SS} .... -0.3V to V_{CC} +1.0V

Storage temperature .... -65°C to +150°C

Ambient temperature with power applied .... -65°C to +125°C

ESD protection on all pins .... ≥ 4 kV

† NOTICE: Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

TABLE 1-1: DC CHARACTERISTICS

DC CHARACTERISTICS			V_{CC} = +1.8V to +5.5V Industrial (I): T_A = -40°C to +85°C Automotive (E): T_A = -40°C to +125°C				
Param. No.	**Symbol**	**Characteristic**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
D1	V_{IH}	**WP, SCL and SDA pins**	—	—	—	—	—
D2	—	High-level input voltage	0.7 V_{CC}	—	—	V	—
D3	V_{IL}	Low-level input voltage	—	—	0.3 V_{CC}	V	—
D4	V_{HYS}	Hysteresis of Schmitt Trigger inputs	0.05 V_{CC}	—	—	V	**(Note 1)**
D5	V_{OL}	Low-level output voltage	—	—	0.40	V	I_{OL} = 3.0 mA, V_{CC} = 2.5V
D6	I_{LI}	**Input leakage current**	—	—	±1	µA	V_{IN} =.1V to V_{CC}
D7	I_{LO}	**Output leakage current**	—	—	±1	µA	V_{OUT} =.1V to V_{CC}
D8	C_{IN}, C_{OUT}	Pin capacitance (all inputs/outputs)	—	—	10	pF	V_{CC} = 5.0V **(Note 1)** T_A = 25°C, F_{CLK} = 1 MHz
D9	I_{CC} write	**Operating current**	—	0.1	3	mA	V_{CC} = 5.5V, SCL = 400 kHz
D10	I_{CC} read		—	0.05	1	mA	—
D11	I_{CCS}	**Standby current**	— —	0.01 —	1 5	µA µA	Industrial Automotive SDA = SCL = V_{CC} WP = V_{SS}

Note 1: This parameter is periodically sampled and not 100% tested.

2: Typical measurements taken at room temperature.

TABLE 1-2: AC CHARACTERISTICS

AC CHARACTERISTICS			V_{CC} = +1.8V to +5.5V Industrial (I): T_A = -40°C to +85°C Automotive (E): T_A = -40°C to +125°C			
Param. No.	**Symbol**	**Characteristic**	**Min**	**Max**	**Units**	**Conditions**
1	FCLK	Clock frequency	— —	400 100	kHz	2.5V ≤ VCC ≤ 5.5V 1.8V ≤ VCC < 2.5V **(24AA32A)**
2	THIGH	Clock high time	600 4000	— —	ns	2.5V ≤ VCC ≤ 5.5V 1.8V ≤ VCC < 2.5V **(24AA32A)**
3	TLOW	Clock low time	1300 4700	— —	ns	2.5V ≤ VCC ≤ 5.5V 1.8V ≤ VCC < 2.5V **(24AA32A)**
4	TR	SDA and SCL rise time **(Note 1)**	— —	300 1000	ns	2.5V ≤ VCC ≤ 5.5V 1.8V ≤ VCC < 2.5V **(24AA32A)**
5	TF	SDA and SCL fall time	—	300	ns	**(Note 1)**
6	THD:STA	Start condition hold time	600 4000	— —	ns	2.5V ≤ VCC ≤ 5.5V 1.8V ≤ VCC < 2.5V **(24AA32A)**
7	TSU:STA	Start condition setup time	600 4700	— —	ns	2.5V ≤ VCC ≤ 5.5V 1.8V ≤ VCC < 2.5V **(24AA32A)**
8	THD:DAT	Data input hold time	0	—	ns	**(Note 2)**
9	TSU:DAT	Data input setup time	100 250	— —	ns	2.5V ≤ VCC ≤ 5.5V 1.8V ≤ VCC < 2.5V **(24AA32A)**
10	TSU:STO	Stop condition setup time	600 4000	— —	ns	2.5V ≤ VCC ≤ 5.5V 1.8V ≤ VCC < 2.5V **(24AA32A)**
11	TAA	Output valid from clock **(Note 2)**	— —	900 3500	ns	2.5V ≤ VCC ≤ 5.5V 1.8V ≤ VCC < 2.5V **(24AA32A)**
12	TBUF	Bus free time: Time the bus must be free before a new transmission can start	1300 4700	— —	ns	2.5V ≤ VCC ≤ 5.5V 1.8V ≤ VCC < 2.5V **(24AA32A)**
13	TOF	Output fall time from VIH minimum to VIL maximum	20+0.1CB —	250 250	ns	2.5V ≤ VCC ≤ 5.5V 1.8V ≤ VCC < 2.5V **(24AA32A)**
14	TSP	Input filter spike suppression (SDA and SCL pins)	—	50	ns	**(Notes 1 and 3)**
15	TWC	Write cycle time (byte or page)	—	5	ms	—
16	—	Endurance	1M	—	cycles	25°C, **(Note 4)**

Note 1: Not 100% tested. CB = total capacitance of one bus line in pF.

2: As a transmitter, the device must provide an internal minimum delay time to bridge the undefined region (minimum 300 ns) of the falling edge of SCL to avoid unintended generation of Start or Stop conditions.

3: The combined TSP and VHYS specifications are due to new Schmitt Trigger inputs which provide improved noise spike suppression. This eliminates the need for a TI specification for standard operation.

4: This parameter is not tested but ensured by characterization. For endurance estimates in a specific application, please consult the Total Endurance™ Model which can be obtained on Microchip's web site: www.microchip.com.

FIGURE 1-1: BUS TIMING DATA

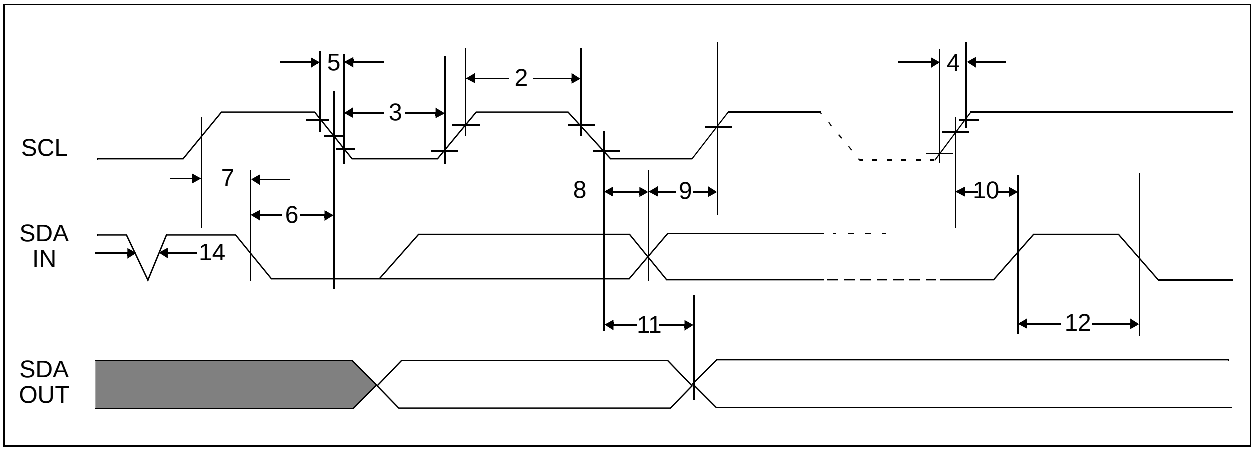
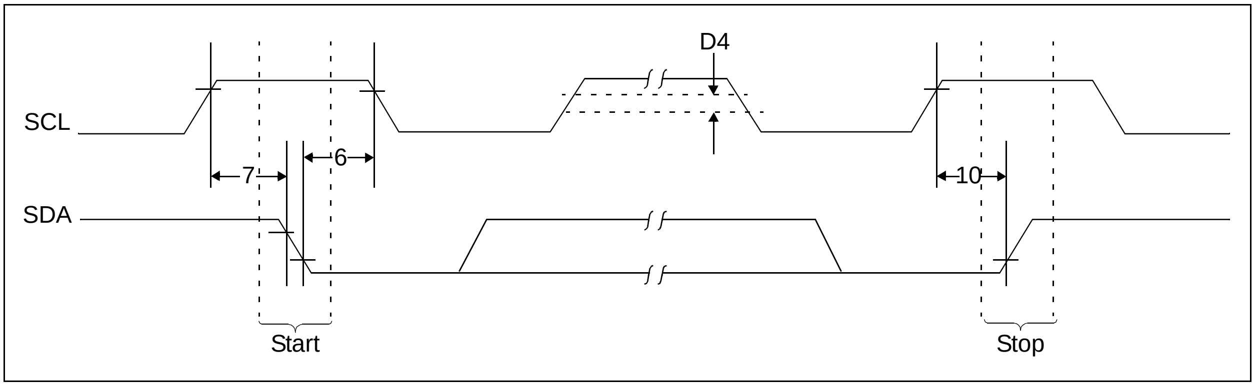


FIGURE 1-2: BUS TIMING START/STOP



2.0 FUNCTIONAL DESCRIPTION

The 24XX32A supports a bidirectional, 2-wire bus and data transmission protocol. A device that sends data onto the bus is defined as transmitter, while a device receiving data is defined as a receiver. The bus has to be controlled by a master device which generates the serial clock (SCL), controls the bus access and generates the Start and Stop conditions, while the 24XX32A works as slave. Both master and slave can operate as transmitter or receiver, but the master device determines which mode is activated.

3.0 BUS CHARACTERISTICS

The following **bus protocol** has been defined:

- Data transfer may be initiated only when the bus is not busy.
- During data transfer, the data line must remain stable whenever the clock line is high. Changes in the data line while the clock line is high will be interpreted as a Start or Stop condition.

Accordingly, the following bus conditions have been defined (Figure 3-1).

3.1 Bus not Busy (A)

Both data and clock lines remain high.

3.2 Start Data Transfer (B)

A high-to-low transition of the SDA line while the clock (SCL) is high determines a Start condition. All commands must be preceded by a Start condition.

3.3 Stop Data Transfer (C)

A low-to-high transition of the SDA line while the clock (SCL) is high determines a Stop condition. All operations must be ended with a Stop condition.

3.4 Data Valid (D)

The state of the data line represents valid data when, after a Start condition, the data line is stable for the duration of the high period of the clock signal.

The data on the line must be changed during the low period of the clock signal. There is one clock pulse per bit of data.

Each data transfer is initiated with a Start condition and terminated with a Stop condition. The number of data bytes transferred between Start and Stop conditions is determined by the master device and is, theoretically unlimited, (although only the last thirty two bytes will be stored when doing a write operation). When an overwrite does occur it will replace data in a first-in first-out (FIFO) fashion.

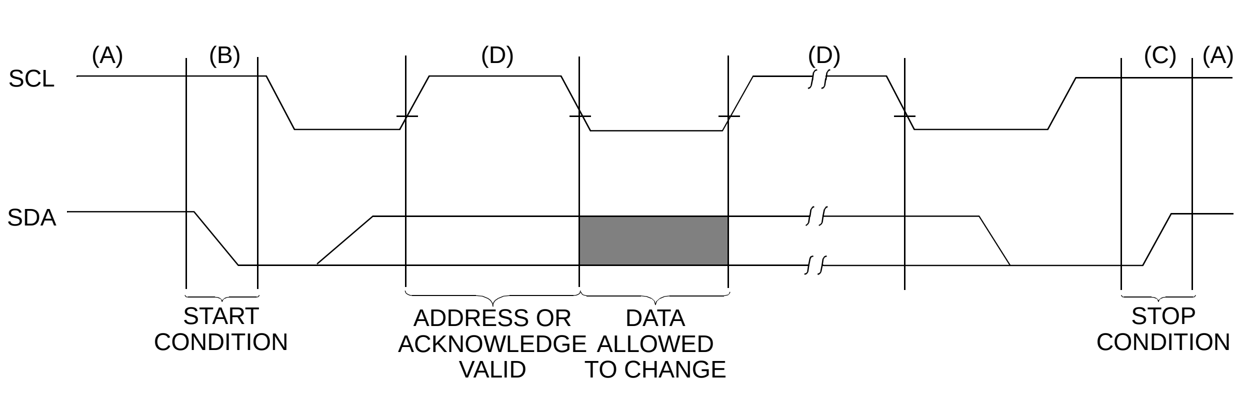
3.5 Acknowledge

Each receiving device, when addressed, is obliged to generate an acknowledge after the reception of each byte. The master device must generate an extra clock pulse which is associated with this Acknowledge bit.

Note:	The 24XX32A does not generate any Acknowledge bits if an internal programming cycle is in progress.

The device that acknowledges, has to pull down the SDA line during the Acknowledge clock pulse in such a way that the SDA line is stable low during the high period of the acknowledge related clock pulse. Of course, setup and hold times must be taken into account. During reads, a master must signal an end of data to the slave by not generating an Acknowledge bit on the last byte that has been clocked out of the slave. In this case, the slave (24XX32A) will leave the data line high to enable the master to generate the Stop condition.

FIGURE 3-1: DATA TRANSFER SEQUENCE ON THE SERIAL BUS



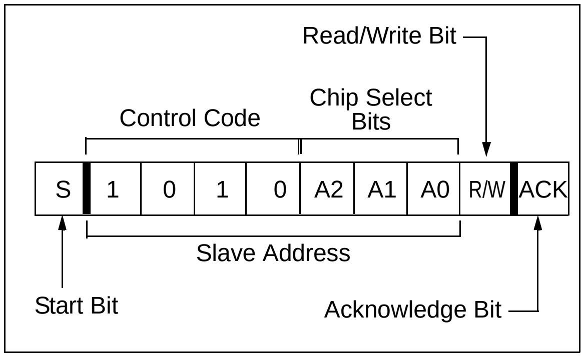
3.6 Device Addressing

A control byte is the first byte received following the Start condition from the master device (Figure 3-2). The control byte consists of a four-bit control code. For the 24XX32A, this is set as '1010' binary for read and write operations. The next three bits of the control byte are the Chip Select bits (A2, A1, A0). The Chip Select bits allow the use of up to eight 24XX32A devices on the same bus and are used to select which device is accessed. The Chip Select bits in the control byte must correspond to the logic levels on the corresponding A2, A1, and A0 pins for the device to respond. These bits are in effect the three Most Significant bits of the word address.

The last bit of the control byte defines the operation to be performed. When set to a '1', a read operation is selected. When set to a zero, a write operation is selected. The next two bytes received define the address of the first data byte (Figure 3-3). Because only A11 to A0 are used, the upper four address bits are don't care bits. The upper address bits are transferred first, followed by the less significant bits.

Following the Start condition, the 24XX32A monitors the SDA bus checking the device type identifier being transmitted and, upon receiving a '1010' code and appropriate device select bits, the slave device outputs an Acknowledge signal on the SDA line. Depending on the state of the R/$\overline{W}$ bit, the 24XX32A will select a read or write operation.

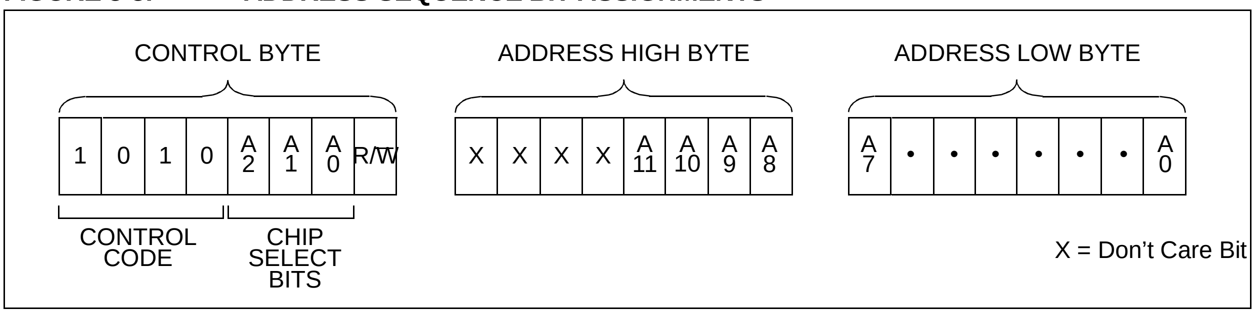
FIGURE 3-2: CONTROL BYTE FORMAT



3.7 Contiguous Addressing Across Multiple Devices

The Chip Select bits A2, A1, A0 can be used to expand the contiguous address space for up to 256K bits by adding up to eight 24XX32A's on the same bus. In this case, software can use A0 of the control byte as address bit A12, A1 as address bit A13, and A2 as address bit A14. It is not possible to sequentially read across device boundaries.

FIGURE 3-3: ADDRESS SEQUENCE BIT ASSIGNMENTS



4.0 WRITE OPERATIONS

4.1 Byte Write

Following the Start condition from the master, the control code (4 bits), the Chip Select (3 bits), and the R/$\overline{W}$ bit (which is a logic low) are clocked onto the bus by the master transmitter. This indicates to the addressed slave receiver that the address high byte will follow once it has generated an Acknowledge bit during the ninth clock cycle. Therefore, the next byte transmitted by the master is the high-order byte of the word address and will be written into the address pointer of the 24XX32A. The next byte is the Least Significant Address Byte. After receiving another Acknowledge signal from the 24XX32A, the master device will transmit the data word to be written into the addressed memory location. The 24XX32A acknowledges again and the master generates a Stop condition. This initiates the internal write cycle and, during this time, the 24XX32A will not generate Acknowledge signals (Figure 4-1). If an attempt is made to write to the array with the WP pin held high, the device will acknowledge the command but no write cycle will occur. No data will be written and the device will immediately accept a new command. After a byte Write command, the internal address counter will point to the address location following the one that was just written.

4.2 Page Write

The write control byte, word address and the first data byte are transmitted to the 24XX32A in the same way as in a byte write. However, instead of generating a Stop condition, the master transmits up to 31 additional bytes which are temporarily stored in the on-chip page buffer and will be written into memory once the master has transmitted a Stop condition. Upon receipt of each word, the five lower-address pointer bits are internally incremented by ‘1’. If the master should transmit more than 32 bytes prior to generating the Stop condition, the address counter will roll over and the previously received data will be overwritten. As with the byte write operation, once the Stop condition is received, an internal write cycle will begin (Figure 4-2). If an attempt is made to write to the array with the WP pin held high, the device will acknowledge the command but no write cycle will occur, no data will be written and the device will immediately accept a new command.

Note:	Page write operations are limited to writing bytes within a single physical page, **regardless** of the number of bytes actually being written. Physical page boundaries start at addresses that are integer multiples of the page buffer size (or ‘page size’) and, end at addresses that are integer multiples of [page size - 1]. If a Page Write command attempts to write across a physical page boundary, the result is that the data wraps around to the beginning of the current page (overwriting data previously stored there), instead of being written to the next page as might be expected. It is therefore necessary for the application software to prevent page write operations that would attempt to cross a page boundary.

4.3 Write-Protection

The WP pin allows the user to write-protect the entire array (0000-0FFFF) when the pin is tied to VCC. If tied to VSS or left floating, the write protection is disabled. The WP pin is sampled at the Stop bit for every write command (Figure 3-1) Toggling the WP pin after the Stop bit will have no effect on the execution of the write cycle.

FIGURE 4-1: BYTE WRITE

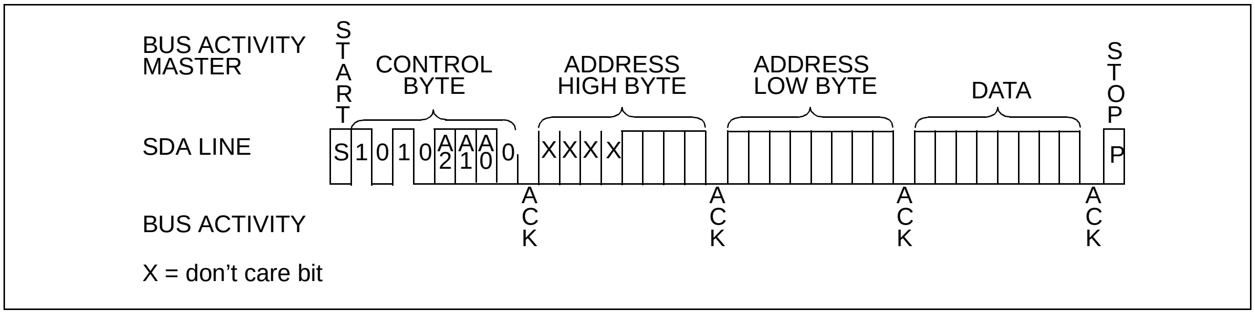
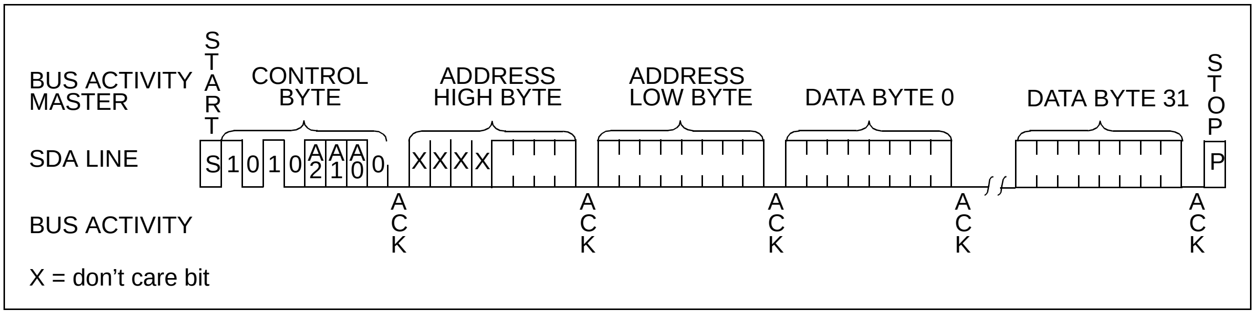


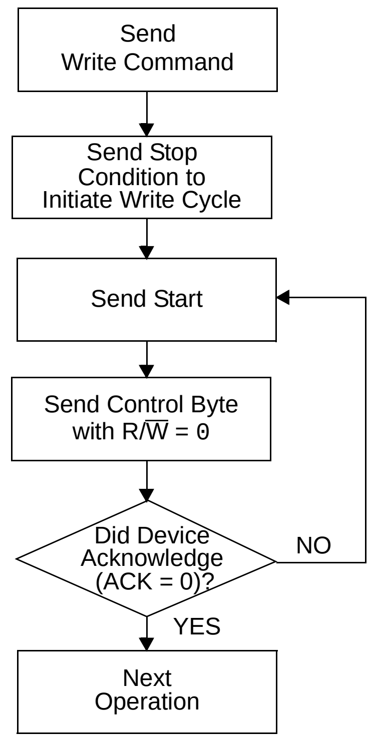
FIGURE 4-2: PAGE WRITE



5.0 ACKNOWLEDGE POLLING

Since the device will not acknowledge during a write cycle, this can be used to determine when the cycle is complete (this feature can be used to maximize bus throughput). Once the Stop condition for a write command has been issued from the master, the device initiates the internally-timed write cycle. ACK polling can then be initiated immediately. This involves the master sending a Start condition followed by the control byte for a Write command (R/$\overline{W}$ = 0). If the device is still busy with the write cycle, then no ACK will be returned. If no ACK is returned, the Start bit and control byte must be re-sent. If the cycle is complete, the device will return the ACK and the master can then proceed with the next Read or Write command. See Figure 5-1 for flow diagram of this operation.

FIGURE 5-1: ACKNOWLEDGE POLLING FLOW



6.0 READ OPERATION

Read operations are initiated in the same way as write operations, with the exception that the R/$\overline{W}$ bit of the control byte is set to '1'. There are three basic types of read operations: current address read, random read, and sequential read.

6.1 Current Address Read

The 24XX32A contains an address counter that maintains the address of the last word accessed, internally incremented by '1'. Therefore, if the previous read access was to address n (n is any legal address), the next current address read operation would access data from address n + 1.

Upon receipt of the control byte with R/$\overline{W}$ bit set to '1', the 24XX32A issues an acknowledge and transmits the 8- bit data word. The master will not acknowledge the transfer but does generate a Stop condition and the 24XX32A discontinues transmission (Figure 6-1).

6.2 Random Read

Random read operations allow the master to access any memory location in a random manner. To perform this type of read operation, the word address must first be first. This is accomplished by sending the word address to the 24XX32A as part of a write operation (R/$\overline{W}$ bit set to '0'). Once the word address is sent, the master generates a Start condition following the acknowledge. This terminates the write operation, but not before the internal address pointer is set. The master issues the control byte again, but with the R/$\overline{W}$ bit set to a '1'. The 24XX32A will then issue an acknowledge and transmit the 8-bit data word. The master will not acknowledge the transfer but does generate a Stop condition which causes the 24XX32A to discontinue transmission (Figure 6-2). After a random Read command, the internal address counter will point to the address location following the one that was just read.

6.3 Sequential Read

Sequential reads are initiated in the same way as a random read, except that once the 24XX32A transmits the first data byte, the master issues an acknowledge as opposed to the Stop condition used in a random read. This acknowledge directs the 24XX32A to transmit the next sequentially addressed 8-bit word (Figure 6-3). Following the final byte transmitted to the master, the master will NOT generate an acknowledge but will generate a Stop condition. To provide sequential reads, the 24XX32A contains an internal address pointer which is incremented by '1' upon completion of each operation. This address pointer allows the entire memory contents to be serially read during one operation. The internal address pointer will automatically roll over from address FFF to address 0000 if the master acknowledges the byte received from the array address 0FFF.

FIGURE 6-1: CURRENT ADDRESS READ

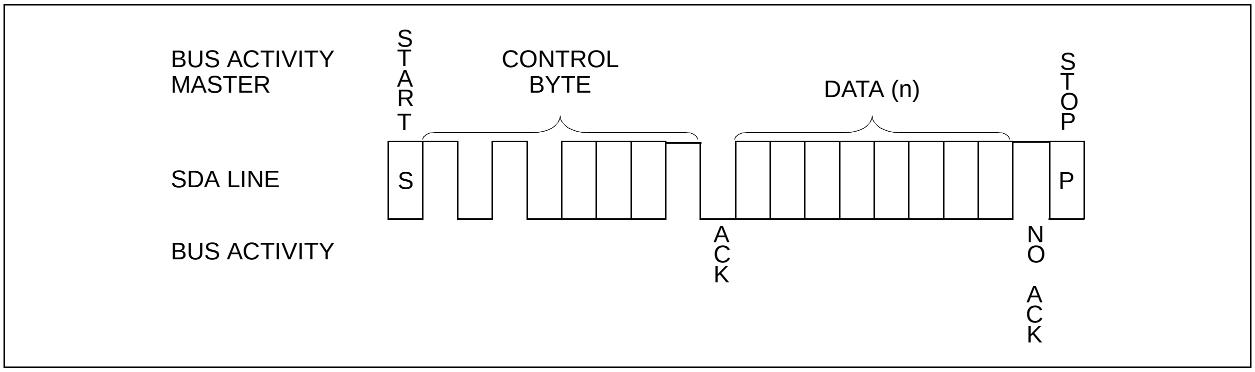


FIGURE 6-2: RANDOM READ

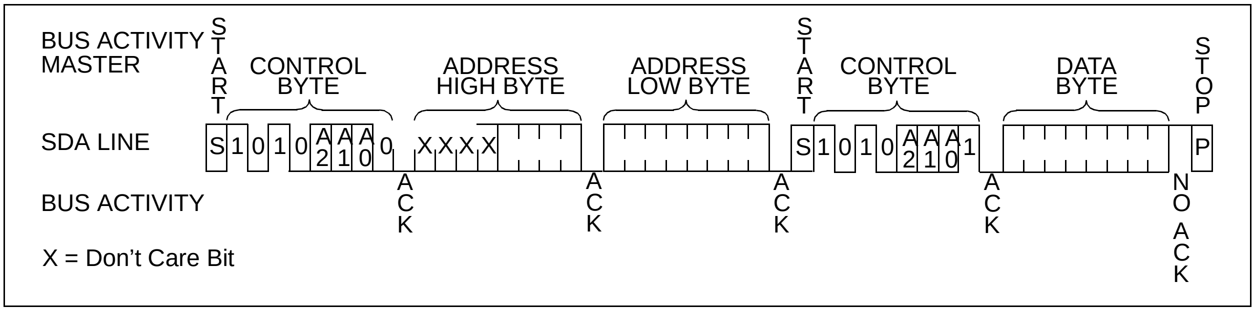
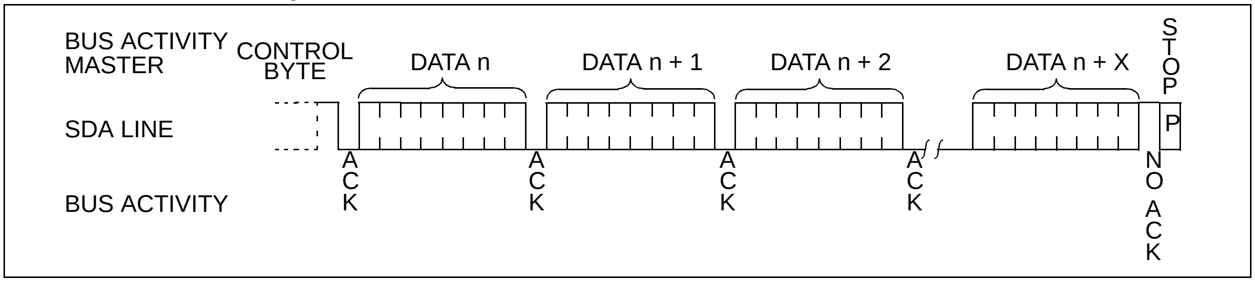


FIGURE 6-3: SEQUENTIAL READ



7.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 7-1.

TABLE 7-1: PIN FUNCTION TABLE

Name	PDIP	SOIC	TSSOP	MSOP	ROTATED TSSOP	Description
A0	1	1	1	1	3	Chip Address Input
A1	2	2	2	2	4	Chip Address Input
A2	3	3	3	3	5	Chip Address Input
VSS	4	4	4	4	6	Ground
SDA	5	5	5	5	7	Serial Address/Data I/O
SCL	6	6	6	6	8	Serial Clock
WP	7	7	7	7	1	Write-Protect Input
VCC	8	8	8	8	2	+1.8V to 5.5V Power Supply

7.1 A0, A1, A2 Chip Address Inputs

The A0, A1, A2 inputs are used by the 24XX32A for multiple device operation. The levels on these inputs are compared with the corresponding bits in the slave address. The chip is selected if the compare is true.

Up to eight devices may be connected to the same bus by using different Chip Select bit combinations. These inputs must be connected to either VCC or VSS.

7.2 Serial Data (SDA)

SDA is a bidirectional pin used to transfer addresses and data into and out of the device. It is an open-drain terminal, therefore, the SDA bus requires a pull-up resistor to VCC (typical 10 kΩ for 100 kHz, 2 kΩ for 400 kHz)

For normal data transfer, SDA is allowed to change only during SCL low. Changes during SCL high are reserved for indicating Start and Stop conditions.

7.3 Serial Clock (SCL)

The SCL input is used to synchronize the data transfer to and from the device.

7.4 Write-Protect (WP)

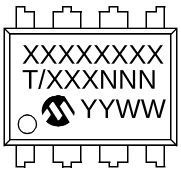
The WP pin can be connected to either VSS, VCC or left floating. An internal pull-down resistor on this pin will keep the device in the unprotected state if left floating. If tied to VSS, or left floating, normal memory operation is enabled (read/write the entire memory 000-FFF).

If tied to VCC, write operations are inhibited. Read operations are not affected.

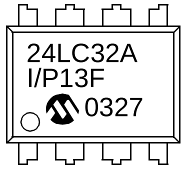
8.0 PACKAGING INFORMATION

8.1 Package Marking Information

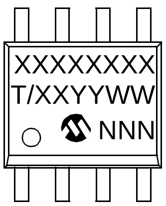
8-Lead PDIP (300 mil)



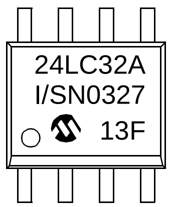
Example:



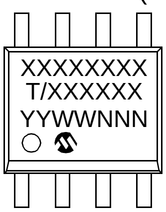
8-Lead SOIC (150 mil)



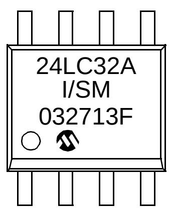
Example:



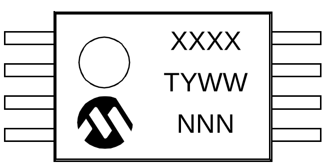
8-Lead SOIC (208 mil)



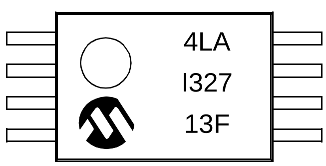
Example:



8-Lead TSSOP

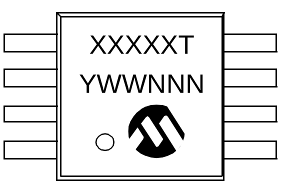


Example:

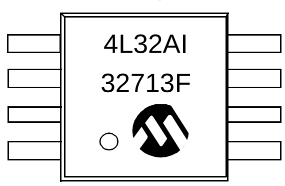


Device	TSSOP Marking Codes			
	STD	**Rot**	**Pb-free**	**Rot**
24AA32A	4AA	4AAX	G4AA	G4AAX
24LC32A	4LA	4LAX	G4LA	G4LAX

8-Lead MSOP



Example:



Device	MSOP Marking Codes	
	STD	**Pb-free**
24AA32A	4A32	G4AA
24LC32A	4L32A	G4LA

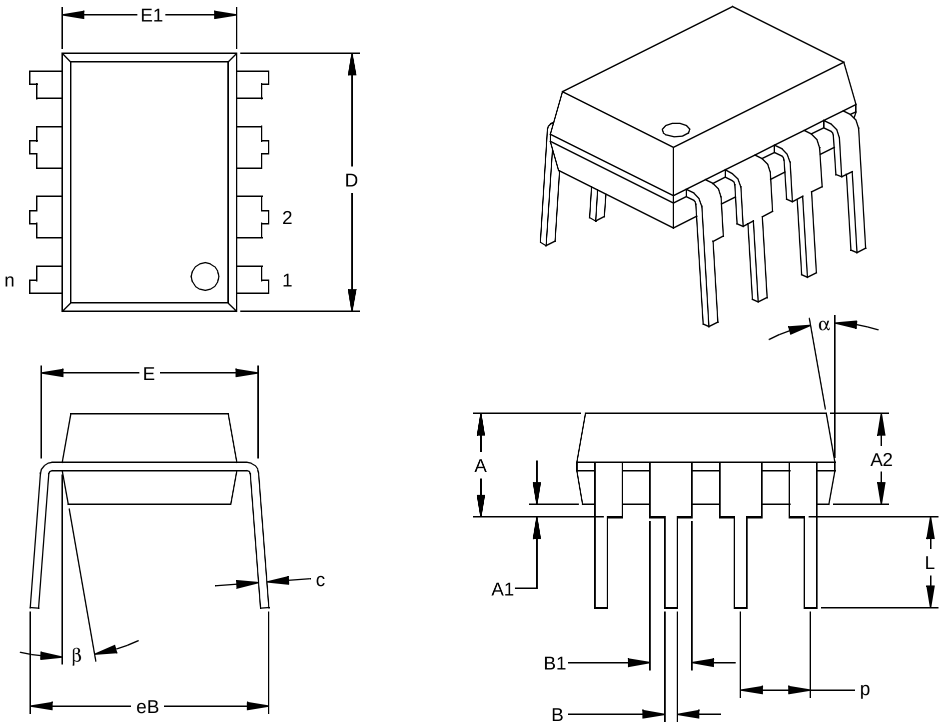
Note: Pb-free part number using “G” suffix is marked on carton

Legend:		
	XX...X	Customer specific information*
	T	Temperature grade (I, E)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line thus limiting the number of available characters for customer specific information.

***Standard QTP marking consists of Microchip part number, year code, week code, and traceability code.

8-Lead Plastic Dual In-line (P) – 300 mil (PDIP)

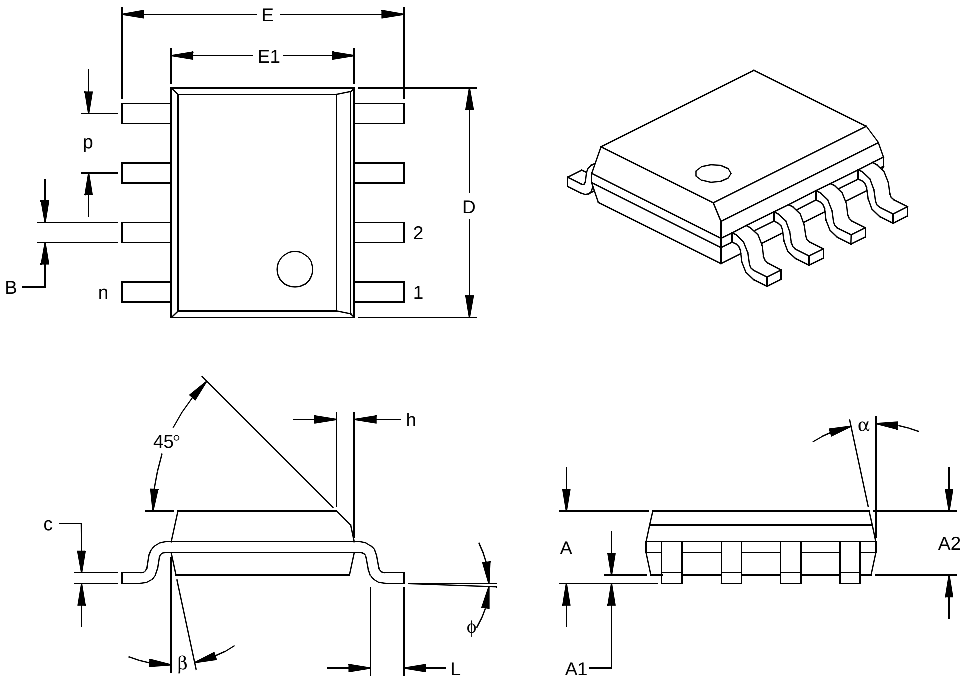


Units		INCHES*			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		8			8	
Pitch	p		.100			2.54	
Top to Seating Plane	A	.140	.155	.170	3.56	3.94	4.32
Molded Package Thickness	A2	.115	.130	.145	2.92	3.30	3.68
Base to Seating Plane	A1	.015			0.38		
Shoulder to Shoulder Width	E	.300	.313	.325	7.62	7.94	8.26
Molded Package Width	E1	.240	.250	.260	6.10	6.35	6.60
Overall Length	D	.360	.373	.385	9.14	9.46	9.78
Tip to Seating Plane	L	.125	.130	.135	3.18	3.30	3.43
Lead Thickness	c	.008	.012	.015	0.20	0.29	0.38
Upper Lead Width	B1	.045	.058	.070	1.14	1.46	1.78
Lower Lead Width	B	.014	.018	.022	0.36	0.46	0.56
Overall Row Spacing §	eB	.310	.370	.430	7.87	9.40	10.92
Mold Draft Angle Top	α	5	10	15	5	10	15
Mold Draft Angle Bottom	β	5	10	15	5	10	15

* Controlling Parameter
§ Significant Characteristic

Notes:
Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" (0.254mm) per side.
JEDEC Equivalent: MS-001
Drawing No. C04-018

8-Lead Plastic Small Outline (SN) – Narrow, 150 mil (SOIC)

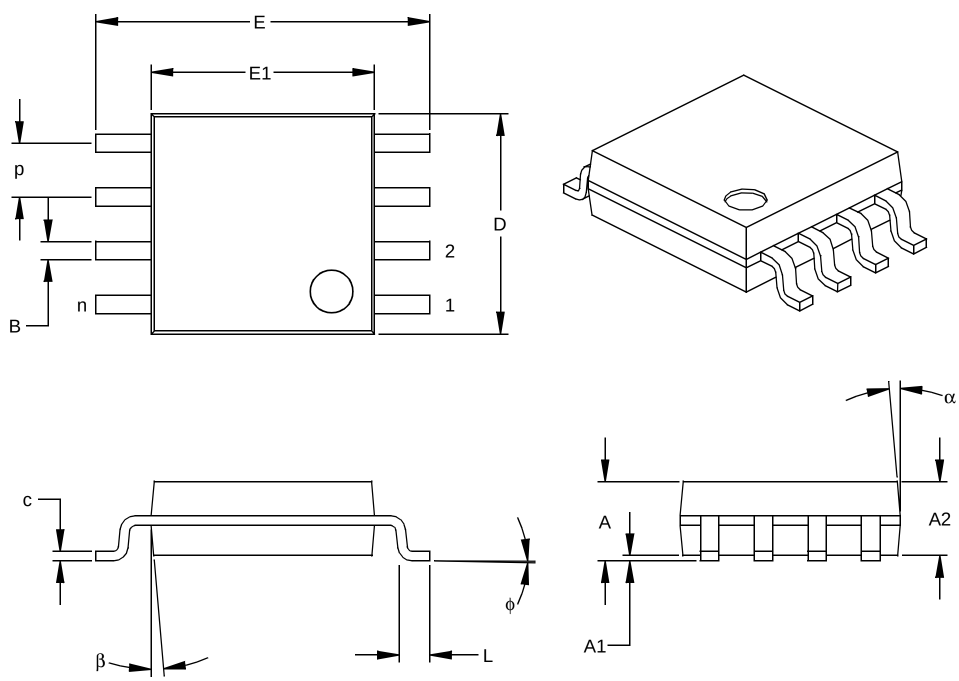


Units		INCHES*			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		8			8	
Pitch	p		.050			1.27	
Overall Height	A	.053	.061	.069	1.35	1.55	1.75
Molded Package Thickness	A2	.052	.056	.061	1.32	1.42	1.55
Standoff §	A1	.004	.007	.010	0.10	0.18	0.25
Overall Width	E	.228	.237	.244	5.79	6.02	6.20
Molded Package Width	E1	.146	.154	.157	3.71	3.91	3.99
Overall Length	D	.189	.193	.197	4.80	4.90	5.00
Chamfer Distance	h	.010	.015	.020	0.25	0.38	0.51
Foot Length	L	.019	.025	.030	0.48	0.62	0.76
Foot Angle	φ	0	4	8	0	4	8
Lead Thickness	c	.008	.009	.010	0.20	0.23	0.25
Lead Width	B	.013	.017	.020	0.33	0.42	0.51
Mold Draft Angle Top	α	0	12	15	0	12	15
Mold Draft Angle Bottom	β	0	12	15	0	12	15

* Controlling Parameter
§ Significant Characteristic

Notes:
Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010” (0.254mm) per side.
JEDEC Equivalent: MS-012
Drawing No. C04-057

8-Lead Plastic Small Outline (SM) – Medium, 208 mil (SOIC)

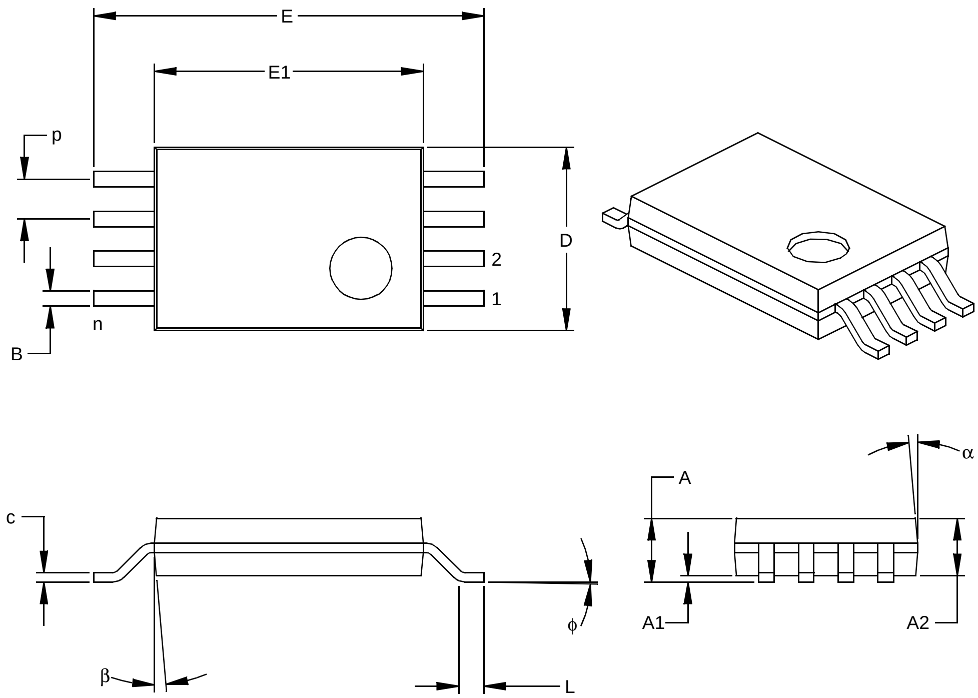


Units		INCHES*			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		8			8	
Pitch	p		.050			1.27	
Overall Height	A	.070	.075	.080	1.78	1.97	2.03
Molded Package Thickness	A2	.069	.074	.078	1.75	1.88	1.98
Standoff §	A1	.002	.005	.010	0.05	0.13	0.25
Overall Width	E	.300	.313	.325	7.62	7.95	8.26
Molded Package Width	E1	.201	.208	.212	5.11	5.28	5.38
Overall Length	D	.202	.205	.210	5.13	5.21	5.33
Foot Length	L	.020	.025	.030	0.51	0.64	0.76
Foot Angle	φ	0	4	8	0	4	8
Lead Thickness	c	.008	.009	.010	0.20	0.23	0.25
Lead Width	B	.014	.017	.020	0.36	0.43	0.51
Mold Draft Angle Top	α	0	12	15	0	12	15
Mold Draft Angle Bottom	β	0	12	15	0	12	15

* Controlling Parameter
§ Significant Characteristic

Notes:
Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010” (0.254mm) per side.
Drawing No. C04-056

8-Lead Plastic Thin Shrink Small Outline (ST) – 4.4 mm (TSSOP)

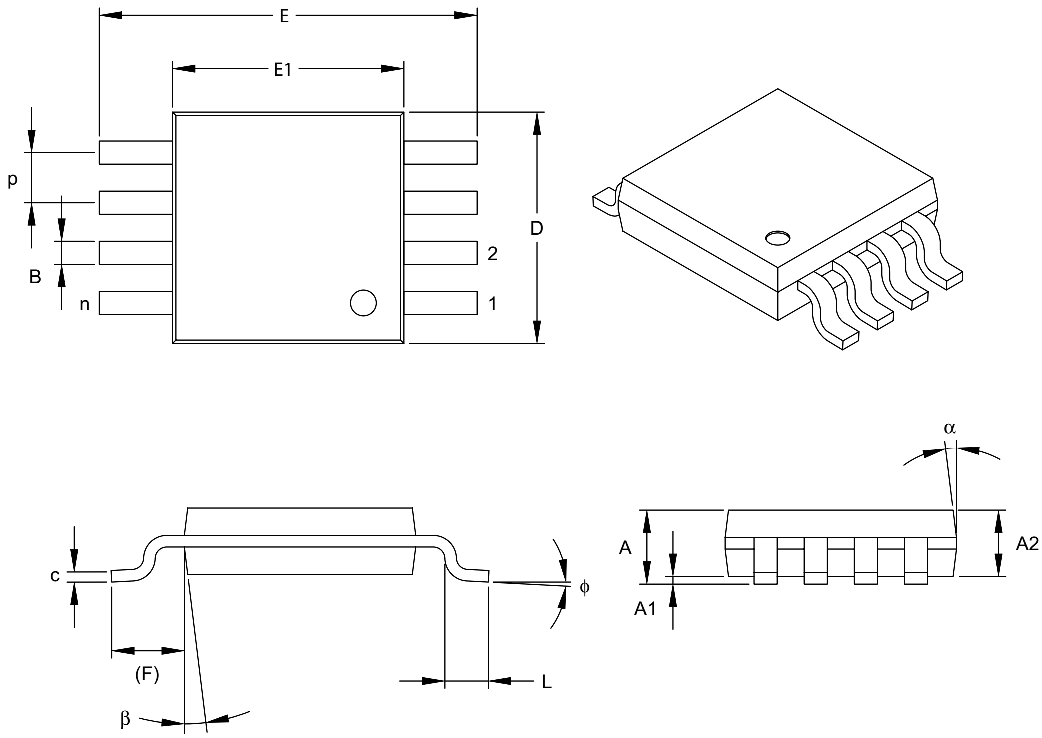


Units		INCHES			MILLIMETERS*		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		8			8	
Pitch	p		.026			0.65	
Overall Height	A			.043			1.10
Molded Package Thickness	A2	.033	.035	.037	0.85	0.90	0.95
Standoff §	A1	.002	.004	.006	0.05	0.10	0.15
Overall Width	E	.246	.251	.256	6.25	6.38	6.50
Molded Package Width	E1	.169	.173	.177	4.30	4.40	4.50
Molded Package Length	D	.114	.118	.122	2.90	3.00	3.10
Foot Length	L	.020	.024	.028	0.50	0.60	0.70
Foot Angle	ϕ	0	4	8	0	4	8
Lead Thickness	c	.004	.006	.008	0.09	0.15	0.20
Lead Width	B	.007	.010	.012	0.19	0.25	0.30
Mold Draft Angle Top	α	0	5	10	0	5	10
Mold Draft Angle Bottom	β	0	5	10	0	5	10

* Controlling Parameter
§ Significant Characteristic

Notes:
Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .005” (0.127mm) per side.
JEDEC Equivalent: MO-153
Drawing No. C04-086

8-Lead Plastic Micro Small Outline Package (MS) (MSOP)



Units		INCHES			MILLIMETERS*		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		8			8	
Pitch	p		.026 BSC			0.65 BSC	
Overall Height	A	-	-	.043	-	-	1.10
Molded Package Thickness	A2	.030	.033	.037	0.75	0.85	0.95
Standoff	A1	.000	-	.006	0.00	-	0.15
Overall Width	E		.193 TYP.			4.90 BSC	
Molded Package Width	E1		.118 BSC			3.00 BSC	
Overall Length	D		.118 BSC			3.00 BSC	
Foot Length	L	.016	.024	.031	0.40	0.60	0.80
Footprint (Reference)	F		.037 REF			0.95 REF	
Foot Angle	ϕ	0°	-	8°	0°	-	8°
Lead Thickness	c	.003	.006	.009	0.08	-	0.23
Lead Width	B	.009	.012	.016	0.22	-	0.40
Mold Draft Angle Top	α	5°	-	15°	5°	-	15°
Mold Draft Angle Bottom	β	5°	-	15°	5°	-	15°

*Controlling Parameter

Notes:

Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" (0.254mm) per side.

JEDEC Equivalent: MO-187

Drawing No. C04-111

APPENDIX A: REVISION HISTORY

Revision D

Corrections to Section 1.0, Electrical Characteristics.

NOTES:

ON-LINE SUPPORT

Microchip provides on-line support on the Microchip World Wide Web site.

The web site is used by Microchip as a means to make files and information easily available to customers. To view the site, the user must have access to the Internet and a web browser, such as Netscape® or Microsoft® Internet Explorer. Files are also available for FTP download from our FTP site.

Connecting to the Microchip Internet Web Site

The Microchip web site is available at the following URL:

www.microchip.com

The file transfer site is available by using an FTP service to connect to:

ftp://ftp.microchip.com

The web site and file transfer site provide a variety of services. Users may download files for the latest Development Tools, Data Sheets, Application Notes, User's Guides, Articles and Sample Programs. A variety of Microchip specific business information is also available, including listings of Microchip sales offices, distributors and factory representatives. Other data available for consideration is:

- Latest Microchip Press Releases
- Technical Support Section with Frequently Asked Questions
- Design Tips
- Device Errata
- Job Postings
- Microchip Consultant Program Member Listing
- Links to other useful web sites related to Microchip Products
- Conferences for products, Development Systems, technical information and more
- Listing of seminars and events

SYSTEMS INFORMATION AND UPGRADE HOT LINE

The Systems Information and Upgrade Line provides system users a listing of the latest versions of all of Microchip's development systems software products. Plus, this line provides information on how customers can receive the most current upgrade kits. The Hot Line Numbers are:

1-800-755-2345 for U.S. and most of Canada, and

1-480-792-7302 for the rest of the world.

042003

READER RESPONSE

It is our intention to provide you with the best documentation possible to ensure successful use of your Microchip product. If you wish to provide your comments on organization, clarity, subject matter, and ways in which our documentation can better serve you, please FAX your comments to the Technical Publications Manager at (480) 792-4150.

Please list the following information, and use this outline to provide us with your comments about this document.

To: Technical Publications Manager   Total Pages Sent ________

RE: Reader Response

From: Name ______________________________

Company ______________________________

Address ______________________________

City / State / ZIP / Country ______________________________

Telephone: (_______) _________ - _________   FAX: (______) _________ - _________

Application (optional):

Would you like a reply? ____Y ____N

Device: 24AA32A/24LC32A   Literature Number: DS21713D

Questions:

1. What are the best features of this document?

____

____

2. How does this document meet your hardware and software development needs?

____

____

3. Do you find the organization of this document easy to follow? If not, why?

____

____

4. What additions to the document do you think would enhance the structure and subject?

____

____

5. What deletions from the document could be made without affecting the overall usefulness?

____

____

6. Is there any incorrect or misleading information (what and where)?

____

____

7. How would you improve this document?

____

____

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	X	/XX	X
Device	Temperature Range	Package	Lead Finish

Device:	24AA32A:	1.8V, 32 Kbit I^2C Serial EEPROM
	24AA32AT:	1.8V, 32 Kbit I^2C Serial EEPROM (Tape and Reel)
	24AA32AX	1.8V, 32 Kbit I^2C Serial EEPROM in alternate pinout (ST only)
	24AA32AXT	1.8V, 32 Kbit I^2C Serial EEPROM in alternate pinout (ST only)
	24LC32A:	2.5V, 32 Kbit I^2C Serial EEPROM
	24LC32AT:	2.5V, 32 Kbit I^2C Serial EEPROM (Tape and Reel)
	24LC32AX	2.5V, 32 Kbit I^2C Serial EEPROM in alternate pinout (ST only)
	24LC32AXT	2.5V, 32 Kbit I^2C Serial EEPROM in alternate pinout (ST only)
Temperature Range:	I =	-40°C to +85°C
	E =	-40°C to +125°C
Package:	P =	Plastic DIP (300 mil body), 8-lead
	SN =	Plastic SOIC (150 mil body), 8-lead
	SM =	Plastic SOIC (208 mil body), 8-lead
	ST =	Plastic TSSOP (4.4 mm), 8-lead
	MS =	Plastic Micro Small Outline (MSOP), 8-lead
Lead Finish	Blank =	Standard 63% / 37% SnPb
	G =	Pb-free (Matte Tin - Pure Sn)

Examples:

a) 24AA32A-I/P: Industrial Temperature,1.8V, PDIP package
b) 24AA32A-I/SN: Industrial Temperature,1.8V, SOIC package
c) 24AA32A-I/SM: Industrial Temperature.,1.8V, SOIC (208 mil) package
d) 24AA32AX-I/ST: Industrial Temp.,1.8V, Rotated TSSOP package
e) 24AA32A-I/ST: Industrial Temperature.,1.8V, TSSOP package
f) 24AA32A-I/PG: Industrial Temperature.,1.8V, PDIP package. Pb-free

g) 24LC32A-I/P: Industrial Temperature, 2.5V, PDIP package
h) 24LC32A-E/SN: Automotive Temperature, 2.5V SOIC package
i) 24LC32A-E/SM: Automotive Temperature, 2.5V SOIC (208 mil) package
j) 24LC32AX-E/ST: Automotive Temperature, 2.5V, Rotated TSSOP package
k) 24LC32AT-I/ST: Industrial Temperature, 2.5V, TSSOP package, Tape and Reel
l) 24LC32AT-I/SNG: Industrial Temperature, 2.5V, SOIC package, Tape and Reel, Pb-free

Sales and Support

Data Sheets

Products supported by a preliminary Data Sheet may have an errata sheet describing minor operational differences and recommended workarounds. To determine if an errata sheet exists for a particular device, please contact one of the following:

1. Your local Microchip sales office
2. The Microchip Corporate Literature Center U.S. FAX: (480) 792-7277
3. The Microchip Worldwide Site (www.microchip.com)

Please specify which device, revision of silicon and Data Sheet (include Literature #) you are using.

New Customer Notification System

Register on our web site (www.microchip.com/cn) to receive the most current information on our products.

NOTES:

Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.
- Microchip is willing to work with the customer who is concerned about the integrity of their code.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as “unbreakable.”

Code protection is constantly evolving. We at Microchip are committed to continuously improving the code protection features of our products. Attempts to break microchip’s code protection feature may be a violation of the Digital Millennium Copyright Act. If such acts allow unauthorized access to your software or other copyrighted work, you may have a right to sue for relief under that Act.

Trademarks

Printed on recycled paper.

Microchip received QS-9000 quality system certification for its worldwide headquarters, design and wafer fabrication facilities in Chandler and Tempe, Arizona in July 1999 and Mountain View, California in March 2002. The Company’s quality system processes and procedures are QS-9000 compliant for its PICmicro® 8-bit MCUs, KEELOQ® code hopping devices, Serial EEPROMs, microperipherals, non-volatile memory and analog products. In addition, Microchip’s quality system for the design and manufacture of development systems is ISO 9001 certified.

WORLDWIDE SALES AND SERVICE

AMERICAS

Corporate Office
2355 West Chandler Blvd.
Chandler, AZ 85224-6199
Tel: 480-792-7200
Fax: 480-792-7277
Technical Support: 480-792-7627
Web Address: http://www.microchip.com

Atlanta
3780 Mansell Road, Suite 130
Alpharetta, GA 30022
Tel: 770-640-0034
Fax: 770-640-0307

Boston
2 Lan Drive, Suite 120
Westford, MA 01886
Tel: 978-692-3848
Fax: 978-692-3821

Chicago
333 Pierce Road, Suite 180
Itasca, IL 60143
Tel: 630-285-0071
Fax: 630-285-0075

Dallas
4570 Westgrove Drive, Suite 160
Addison, TX 75001
Tel: 972-818-7423
Fax: 972-818-2924

Detroit
Tri-Atria Office Building
32255 Northwestern Highway, Suite 190
Farmington Hills, MI 48334
Tel: 248-538-2250
Fax: 248-538-2260

Kokomo
2767 S. Albright Road
Kokomo, IN 46902
Tel: 765-864-8360
Fax: 765-864-8387

Los Angeles
18201 Von Karman, Suite 1090
Irvine, CA 92612
Tel: 949-263-1888
Fax: 949-263-1338

Phoenix
2355 West Chandler Blvd.
Chandler, AZ 85224-6199
Tel: 480-792-7966
Fax: 480-792-4338

San Jose
2107 North First Street, Suite 590
San Jose, CA 95131
Tel: 408-436-7950
Fax: 408-436-7955

Toronto
6285 Northam Drive, Suite 108
Mississauga, Ontario L4V 1X5, Canada
Tel: 905-673-0699
Fax: 905-673-6509

ASIA/PACIFIC

Australia
Suite 22, 41 Rawson Street
Epping 2121, NSW
Australia
Tel: 61-2-9868-6733
Fax: 61-2-9868-6755

China - Beijing
Unit 915
Bei Hai Wan Tai Bldg.
No. 6 Chaoyangmen Beidajie
Beijing, 100027, No. China
Tel: 86-10-85282100
Fax: 86-10-85282104

China - Chengdu
Rm. 2401-2402, 24th Floor,
Ming Xing Financial Tower
No. 88 TIDU Street
Chengdu 610016, China
Tel: 86-28-86766200
Fax: 86-28-86766599

China - Fuzhou
Unit 28F, World Trade Plaza
No. 71 Wusi Road
Fuzhou 350001, China
Tel: 86-591-7503506
Fax: 86-591-7503521

China - Hong Kong SAR
Unit 901-6, Tower 2, Metroplaza
223 Hing Fong Road
Kwai Fong, N.T., Hong Kong
Tel: 852-2401-1200
Fax: 852-2401-3431

China - Shanghai
Room 701, Bldg. B
Far East International Plaza
No. 317 Xian Xia Road
Shanghai, 200051
Tel: 86-21-6275-5700
Fax: 86-21-6275-5060

China - Shenzhen
Rm. 1812, 18/F, Building A, United Plaza
No. 5022 Binhe Road, Futian District
Shenzhen 518033, China
Tel: 86-755-82901380
Fax: 86-755-8295-1393

China - Shunde
Room 401, Hongjian Building
No. 2 Fengxiangnan Road, Ronggui Town
Shunde City, Guangdong 528303, China
Tel: 86-765-8395507 Fax: 86-765-8395571

China - Qingdao
Rm. B505A, Fullhope Plaza,
No. 12 Hong Kong Central Rd.
Qingdao 266071, China
Tel: 86-532-5027355 Fax: 86-532-5027205

India
Divyasree Chambers
1 Floor, Wing A (A3/A4)
No. 11, O'Shaugnessey Road
Bangalore, 560 025, India
Tel: 91-80-2290061 Fax: 91-80-2290062

Japan
Benex S-1 6F
3-18-20, Shinyokohama
Kohoku-Ku, Yokohama-shi
Kanagawa, 222-0033, Japan
Tel: 81-45-471- 6166 Fax: 81-45-471-6122

Korea
168-1, Youngbo Bldg. 3 Floor
Samsung-Dong, Kangnam-Ku
Seoul, Korea 135-882
Tel: 82-2-554-7200 Fax: 82-2-558-5932 or
82-2-558-5934

Singapore
200 Middle Road
#07-02 Prime Centre
Singapore, 188980
Tel: 65-6334-8870 Fax: 65-6334-8850

Taiwan
Kaohsiung Branch
30F - 1 No. 8
Min Chuan 2nd Road
Kaohsiung 806, Taiwan
Tel: 886-7-536-4818
Fax: 886-7-536-4803

Taiwan
Taiwan Branch
11F-3, No. 207
Tung Hua North Road
Taipei, 105, Taiwan
Tel: 886-2-2717-7175 Fax: 886-2-2545-0139

EUROPE

Austria
Durisolstrasse 2
A-4600 Wels
Austria
Tel: 43-7242-2244-399
Fax: 43-7242-2244-393

Denmark
Regus Business Centre
Lautrup hoj 1-3
Ballerup DK-2750 Denmark
Tel: 45-4420-9895 Fax: 45-4420-9910

France
Parc d'Activite du Moulin de Massy
43 Rue du Saule Trapu
Batiment A - ler Etage
91300 Massy, France
Tel: 33-1-69-53-63-20
Fax: 33-1-69-30-90-79

Germany
Steinheilstrasse 10
D-85737 Ismaning, Germany
Tel: 49-89-627-144-0
Fax: 49-89-627-144-44

Italy
Via Quasimodo, 12
20025 Legnano (MI)
Milan, Italy
Tel: 39-0331-742611
Fax: 39-0331-466781

Netherlands
P. A. De Biesbosch 14
NL-5152 SC Drunen, Netherlands
Tel: 31-416-690399
Fax: 31-416-690340

United Kingdom
505 Eskdale Road
Winnersh Triangle
Wokingham
Berkshire, England RG41 5TU
Tel: 44-118-921-5869
Fax: 44-118-921-5820

07/28/03