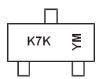


Marking Information



 $\begin{array}{l} \text{K7K} = \text{Product Type Marking Code} \\ \text{YM} = \text{Date Code Marking} \\ \text{Y or } \overline{\text{Y}} = \text{Year (ex: I = 2021)} \\ \text{M or } \overline{\text{M}} = \text{Month (ex: 9 = September)} \end{array}$

Date Code Key

Year	2006		2021	2022	2023	2024	2025	2026	2027	2028	2029	2030
Code	Т		_	J	K	L	М	N	0	Р	R	S
								1				1
Month	Jan	Feb	Mar	Apr	May	Jun	Jul	Aug	Sep	Oct	Nov	Dec

Maximum Ratings (@T_A = +25°C, unless otherwise specified.)

Characteristic	Symbol	Value	Unit			
Drain-Source Voltage	VDSS	60	V			
Gate-Source Voltage			Vgss	±20	V	
Operitoring Preio Operant (Note 6) V	Steady State	T _A = +25°C T _A = +70°C	lo	380 300	mA	
Continuous Drain Current (Note 6) V _{GS} = 10V	t<5s	T _A = +25°C T _A = +70°C	I _D	430 340	mA	
Continuous Dunin Coursett (Note C) V	Steady State	T _A = +25°C T _A = +70°C	I _D	310 240	mA	
Continuous Drain Current (Note 6) V _{GS} = 5V	t<5s	T _A = +25°C T _A = +70°C	lo	350 270	mA	
Maximum Continuous Body Diode Forward Curre	ls	0.5	Α			
Pulsed Drain Current (10µs Pulse, Duty Cycle = 1	IDM	1.2	А			

Thermal Characteristics (@TA = +25°C, unless otherwise specified.)

Characteristic		Symbol	Value	Unit
Total Power Dissipation (Note 5)		PD	370	mW
Thermal Resistance, Junction to Ambient (Note 5)	Steady State	Reja	357	°C/W
Thermal Resistance, Junction to Ambient (Note 5)	t<5s	Көја	292	C/VV
Total Power Dissipation (Note 6)		PD	540	mW
Thermal Decistores, Junction to Ambient (Note 6)	Steady State	D	240	
Thermal Resistance, Junction to Ambient (Note 6)	t<5s	Reja	197	°C/W
Thermal Resistance, Junction to Case (Note 6)		Rejc	91	
Operating and Storage Temperature Range		TJ, TSTG	-55 to +150	°C

5. Device mounted on FR-4 PCB, with minimum recommended pad layout.
6. Device mounted on 1" x 1" FR-4 PCB with high coverage 2oz. copper, single sided.

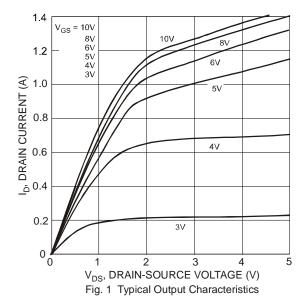


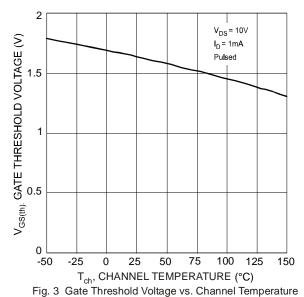
Electrical Characteristics (@T_A = +25°C, unless otherwise specified.)

Characteristic	Symbol	Min	Тур	Max	Unit	Test Condition	
OFF CHARACTERISTICS (Note 7)							
Drain-Source Breakdown Voltage	BVDSS	60	_	_	V	$V_{GS} = 0V, I_{D} = 10\mu A$	
Zero Gate Voltage Drain Current	IDSS	_	_	1.0	μΑ	$V_{DS} = 60V$, $V_{GS} = 0V$	
Gate-Source Leakage	I _{GSS}	_	_	±10	μΑ	$V_{GS} = \pm 20V, V_{DS} = 0V$	
ON CHARACTERISTICS (Note 7)	_						
Gate Threshold Voltage	Vgs(th)	1.0	1.6	2.5	V	$V_{DS} = 10V$, $I_D = 1mA$	
Static Drain-Source On-Resistance	Process		1.2	2.0	0	$V_{GS} = 10V, I_{D} = 0.5A$	
Static Dialit-Source Off-Resistance	RDS(ON)		1.4	3.0	22	$V_{GS} = 5V, I_{D} = 0.05A$	
Forward Transfer Admittance	Y _{fs}	80	_	_	ms	$V_{DS} = 10V, I_D = 0.2A$	
Diode Forward Voltage	VsD		0.75	1.1	>	$V_{GS} = 0V, I_{S} = 115mA$	
DYNAMIC CHARACTERISTICS (Note 8)							
Input Capacitance	Ciss	_	30	50	pF	V 05V V 0V	
Output Capacitance	Coss	_	4.2	25	рF	$V_{DS} = 25V, V_{GS} = 0V$ f = 1.0MHz	
Reverse Transfer Capacitance	Crss		2.9	5.0	рF	1 – 1.000112	
Gate Resistance	Rg		133	_	Ω	$f = 1MHz$, $V_{GS} = 0V$, $V_{DS} = 0V$	
Total Gate Charge	Q_g	_	0.3	_	nC	1/ 451/1/ 401/	
Gate-Source Charge	Qgs	_	0.2	_	nC	$V_{GS} = 4.5V, V_{DS} = 10V,$ $I_{D} = 250 \text{mA}$	
Gate-Drain Charge	Q_{gd}	_	0.08	_	nC	ID = 230IIIA	
Turn-On Delay Time	t _{D(ON)}	_	3.9	_	ns		
Turn-On Rise Time	t _R	_	3.4	_	ns	V _{DD} = 30V, V _{GS} = 10V,	
Turn-Off Delay Time	tD(OFF)	_	15.7	_	ns	$R_G = 25\Omega$, $I_D = 200mA$	
Turn-Off Fall Time	tF	_	9.9	_	ns		

7. Short duration pulse test used to minimize self-heating effect. 8. Guaranteed by design. Not subject to product testing. Notes:







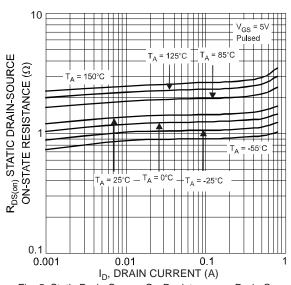
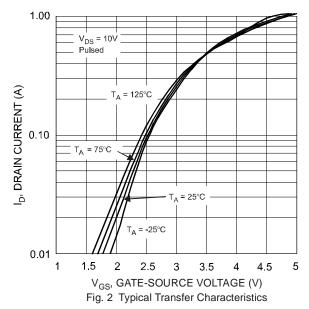


Fig. 5 Static Drain-Source On-Resistance vs. Drain Current



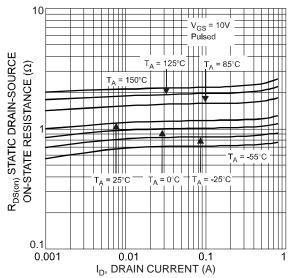


Fig. 4 Static Drain-Source On-Resistance vs. Drain Current

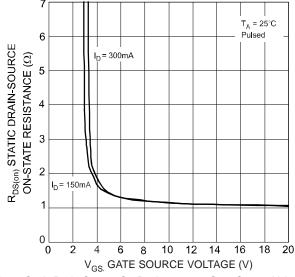


Fig. 6 Static Drain-Source On-Resistance vs. Gate-Source Voltage



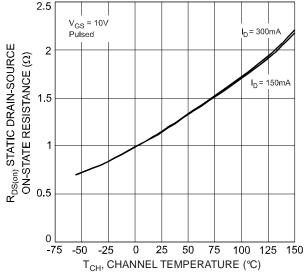


Fig. 7 Static Drain-Source On-State Resistance vs. Channel Temperature

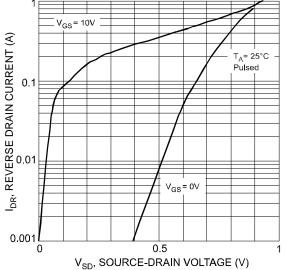
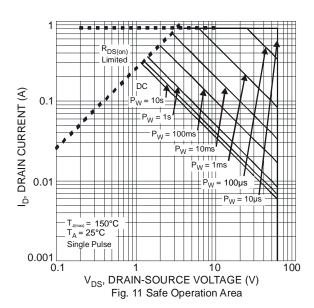
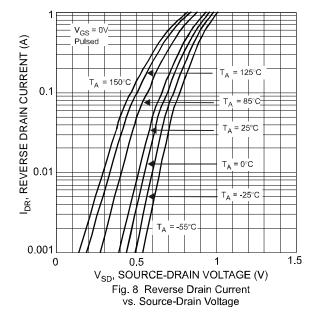


Fig. 9 Reverse Drain Current vs. Source-Drain Voltage





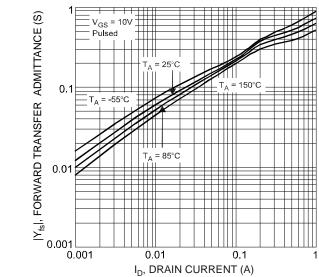


Fig.10 Forward Transfer Admittance vs. Drain Current

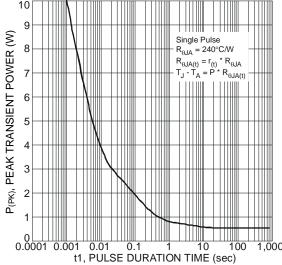
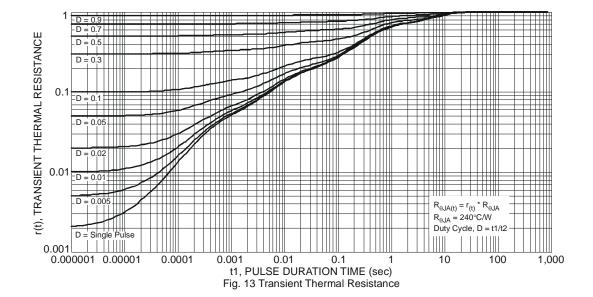


Fig. 12 Single Pulse Maximum Power Dissipation



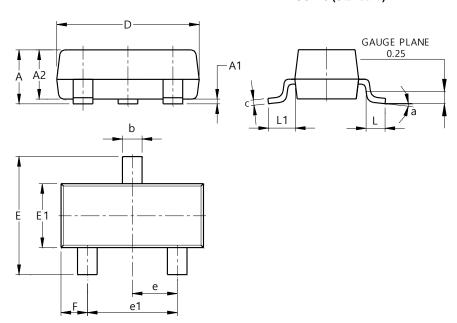




Package Outline Dimensions

Please see http://www.diodes.com/package-outlines.html for the latest version.

SOT23 (Standard)

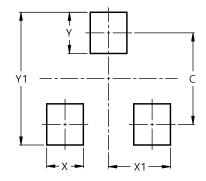


SOT23 (Standard)							
Dim	Min	Max	Тур				
Α	0.90	1.15	1.025				
A1	0.00	0.10	0.05				
A2	0.85	1.10	0.975				
b	0.30	0.51	0.40				
С	0.080	0.202	0.11				
D	2.80	3.00	2.90				
Е	2.25	2.55	2.40				
E1	1.20	1.40	1.30				
е	0.89	1.03	0.915				
e1	1.78	2.05	1.83				
F	0.40	0.60	0.535				
L1	0.45	0.61	0.55				
L	0.25	0.55	0.40				
а	0°	8°					
All Dimensions in mm							

Suggested Pad Layout

Please see http://www.diodes.com/package-outlines.html for the latest version.

SOT23 (Standard)



Dimensions	Value (in mm)
С	2.0
Х	0.8
X1	1.35
Y	0.9
Y1	2.9



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