ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise stated)

Symbols	Parameters	Test Conditions		Min.	Typ.	Max.	Units
$V_{(BR)DSS}$	Drain - Source Breakdown Voltage	V_{GS} = 0	I_D = 0.25mA	100			V
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}	I_D = 0.25mA	2.0		4.0	V
I_{GSS}	Gate - Source Leakage	V_{DS} = 0	V_{GS} = ±20V			±100	nA
I_{DSS}	Zero Gate Voltage Drain Current	V_{GS} = 0	V_{DS} = 0.8BV_{DSS}			250	µA
			T_A = 125°C			1000	
$R_{DS(on)}$ (2)	Static Drain - Source On - State Resistance	V_{GS} = 10V	I_D = 4.6A			0.18	Ω
			T_A = 125°C			0.35	
		V_{GS} = 10V	I_D = 7.2A			0.207	
$V_{DS(on)}$	Drain-Source On-Voltage	V_{GS} = 10V	I_D = 7.2A			1.5	V
g_{fs} (2)	Forward Transconductance	V_{GS} = 15V	I_D = 4.6A	3			S(ʊ)

DYNAMIC CHARACTERISTICS (T_C = 25°C unless otherwise stated)

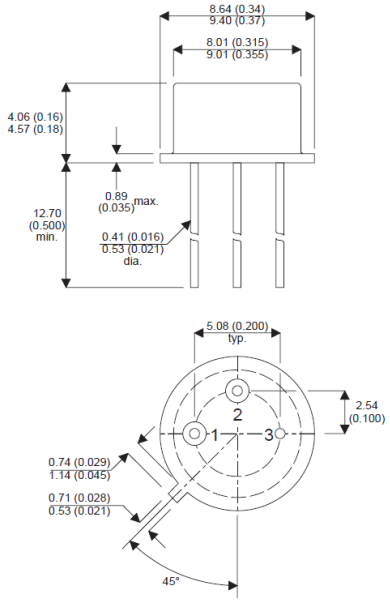
C_{iss}	Input Capacitance	V_{DS} = 25V V_{GS} = 0V f = 1.0MHz		683		pF
C_{oss}	Output Capacitance			165		
C_{rss}	Reverse Transfer Capacitance			84		
$t_{d(on)}$	Turn-On Delay Time	V_{DD} = 50V I_D = 7.2A R_G = 7.5Ω			30	ns
t_r	Rise Time				75	
$t_{d(off)}$	Turn-Off Delay Time				40	
t_f	Fall Time				45	

SOURCE-DRAIN DIODE CHARACTERISTICS

t_{rr} (3)	Reverse Recovery Time	I_S = 7.2A di/dt ≤ 100A/µs	V_{GS} = 0 VDD ≤ 50V			300	ns

MECHANICAL DATA

Dimensions in mm (inches)



TO-39 (TO-205AF)

PACKAGE PIN CONNECTIONS

Pin	Connection
1	Source
2	Gate
3	Drain

PART NUMBER VARIANTS(4)(5)

Part Number Reference	Termination Finish	SML ROHS
2N6796	Pre-tinned 63% Tin, 37% Lead	LD(6)

Notes

(4) Specify lead finish option by part number at point of order.

(5) All design variants contain Lead (Pb) within the construction of the device. The Lead content is fully RoHS compliant but using an exemption as currently understood from the EU directive 2011/65/EU (Annex III, exemption 7a).

(6) LD = e0, as defined in J-STD-609 2nd Level Interconnect Category.