1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings(†)

VCC 7.0V
All inputs and outputs w.r.t. VSS .... -0.6V to VCC + 1.0V
Storage temperature .... -65°C to +150°C
Ambient temperature with power applied .... -40°C to +125°C
Soldering temperature of leads (10 seconds) .... +300°C
ESD protection on all pins .... ≥ 4 kV

† NOTICE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

TABLE 1-1: DC CHARACTERISTICS

DC CHARACTERISTICS	**VCC = +2.5V to 5.5V** **Commercial (C): TA = 0°C to +70°C** **Industrial (I): TA = -40°C to +85°C**				
Parameter	**Symbol**	**Min**	**Max**	**Units**	**Conditions**
SCL and SDA pins: High-level input voltage Low-level input voltage	VIH VIL	.7 VCC —	— .3 VCC	V V	— —
Input levels on VCLK pin: High-level input voltage Low-level input voltage	VIH VIL	2.0 —	.8 .2 VCC	V V	VCC ≥ 2.7V **(Note 1)** VCC < 2.7V **(Note 1)**
Hysteresis of Schmitt Trigger inputs	VHYS	.05 VCC	—	V	**(Note 1)**
Low-level output voltage	VOL1	—	.4	V	IOL = 3 mA, VCC = 2.5V **(Note 1)**
Low-level output voltage	VOL2	—	.6	V	IOL = 6 mA, VCC = 2.5V
Input leakage current	ILI	-10	10	µA	VIN = .1V to VCC
Output leakage current	ILO	-10	10	µA	VOUT = .1V to VCC
Pin capacitance (all inputs/outputs)	CIN, COUT	—	10	pF	VCC = 5.0V **(Note1)**, TA = 25°C, FCLK = 1 MHz
Operating current	ICC Write ICC Read	— —	3 1	mA mA	VCC = 5.5V, SCL = 400 kHz
Standby current	ICCS	— —	30 100	µA µA	VCC = 3.0V, SDA = SCL = VCC VCC = 5.5V, SDA = SCL = VCC **(Note 2)**

Note 1: This parameter is periodically sampled and not 100% tested.
2: VLCK must be grounded.

TABLE 1-2: AC CHARACTERISTICS

Parameter	Symbol	Standard Mode		Vcc= 4.5 - 5.5V Fast Mode		Units	Remarks
		Min	Max	Min	Max		
Clock frequency	FCLK	—	100	—	400	kHz	—
Clock high time	THIGH	4000	—	600	—	ns	—
Clock low time	TLOW	4700	—	1300	—	ns	—
SDA and SCL rise time	TR	—	1000	—	300	ns	**(Note 1)**
SDA and SCL fall time	TF	—	300	—	300	ns	**(Note 1)**
Start condition hold time	THD:STA	4000	—	600	—	ns	After this period the first clock pulse is generated
Start condition setup time	TSU:STA	4700	—	600	—	ns	Only relevant for repeated Start condition
Data input hold time	THD:DAT	0	—	0	—	ns	**(Note 2)**
Data input setup time	TSU:DAT	250	—	100	—	ns	—
Stop condition setup time	TSU:STO	4000	—	600	—	ns	—
Output valid from clock	TAA	—	3500	—	900	ns	**(Note 2)**
Bus free time	TBUF	4700	—	1300	—	ns	Time the bus must be free before a new transmission can start
Output fall time from VIH min. to VIL max.	TOF	—	250	20 + .1 CB	250	ns	**(Note 1)**, CB ≤ 100 pF
Input filter spike suppression (SDA and SCL pins)	TSP	—	50	—	50	ns	**(Note 3)**
Write cycle time	TWR	—	10	—	10	ms	Byte or Page mode
Transmit-only Mode Parameters							
Output valid from VCLK	TVAA	—	2000	—	1000	ns	—
VCLK high time	TVHIGH	4000	—	600	—	ns	—
VCLK low time	TVLOW	4700	—	1300	—	ns	—
Mode transition time	TVHZ	—	500	—	500	ns	—
Transmit-only power-up time	TVPU	0	—	0	—	ns	—
Endurance	—	1M	—	1M	—	cycles	25°C, VCC = 5.0V, Block mode **(Note 4)**

Note 1: Not 100% tested. CB = total capacitance of one bus line in pF.

2: As a transmitter, the device must provide an internal minimum delay time to bridge the undefined region (minimum 300 ns) of the falling edge of SCL to avoid unintended generation of Start or Stop conditions.

3: The combined TSP and VHYS specifications are due to new Schmitt Trigger inputs which provide improved noise and spike suppression. This eliminates the need for a TI specification for standard operation.

4: This parameter is not tested but ensured by characterization. For endurance estimates in a specific application, please consult the Total Endurance™ Model which can be obtained from Microchip's web site at: www.microchip.com

2.0 FUNCTIONAL DESCRIPTION

The 24LC21 operates in two modes, the Transmit-only mode and the Bidirectional mode. There is a separate two wire protocol to support each mode, each having a separate clock input and sharing a common data line (SDA). The device enters the Transmit-only mode upon power-up. In this mode, the device transmits data bits on the SDA pin in response to a clock signal on the VCLK pin. The device will remain in this mode until a valid high-to-low transition is placed on the SCL input. When a valid transition on SCL is recognized, the device will switch into the Bidirectional mode. The only way to switch the device back to the Transmit-only mode is to remove power from the device.

2.1 Transmit-only Mode

The device will power-up in the Transmit-only mode. This mode supports a unidirectional two wire protocol for transmission of the contents of the memory array. This device requires that it be initialized prior to valid data being sent in the Transmit-only mode (see Initialization Procedure, below). In this mode, data is transmitted on the SDA pin in 8-bit bytes, each followed by a ninth, null bit (see Figure 2-1). The clock source for the Transmit-only mode is provided on the VCLK pin, and a data bit is output on the rising edge on this pin. The eight bits in each byte are transmitted Most Significant bit first. Each byte within the memory array will be output in sequence. When the last byte in the memory array is transmitted, the output will wrap around to the first location and continue. The Bidirectional mode Clock (SCL) pin must be held high for the device to remain in the Transmit-only mode.

2.2 Initialization Procedure

After VCC has stabilized, the device will be in the Transmit-only mode. Nine clock cycles on the VCLK pin must be given to the device for it to perform internal synchronization. During this period, the SDA pin will be in a high-impedance state. On the rising edge of the tenth clock cycle, the device will output the first valid data bit which will be the Most Significant bit of a byte. The device will power-up at an indeterminate byte address. (Figure 2-2).

FIGURE 2-1: TRANSMIT-ONLY MODE

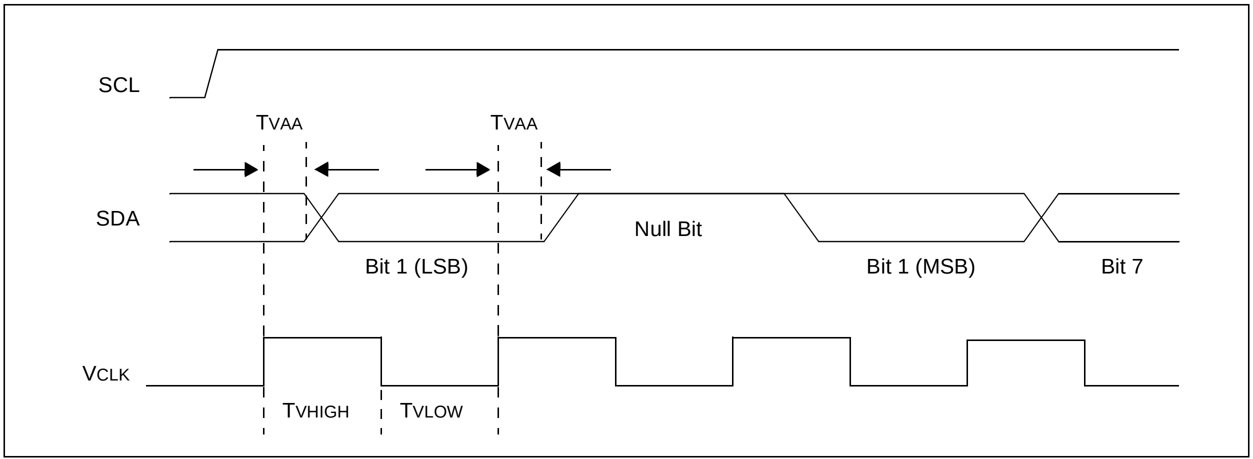
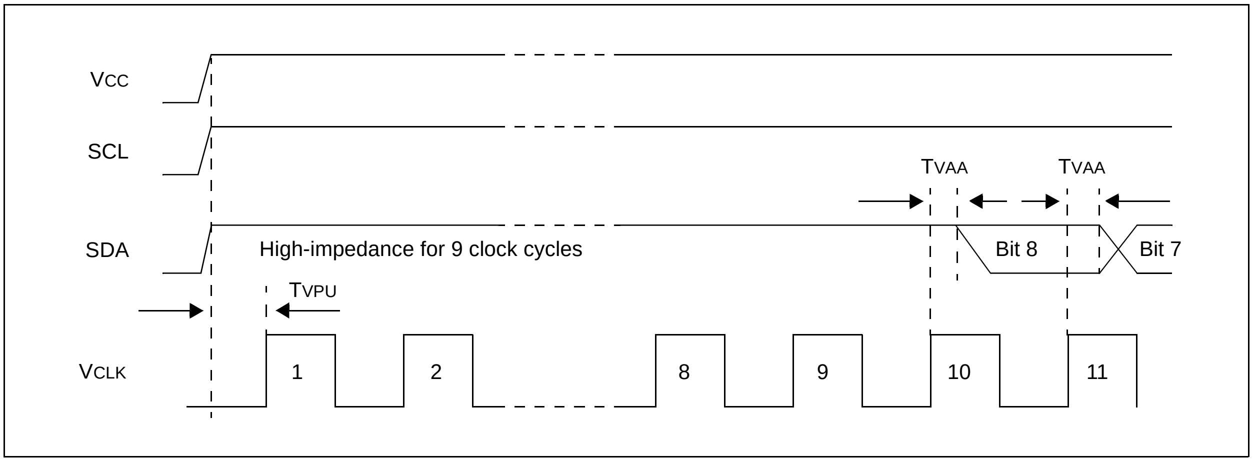


FIGURE 2-2: DEVICE INITIALIZATION



3.0 BIDIRECTIONAL MODE

The 24LC21 can be switched into the Bidirectional mode (see Figure 3-1) by applying a valid high-to-low transition on the Bidirectional mode clock (SCL). When the device has been switched into the Bidirectional mode, the VCLK input is disregarded, with the exception that a logic high level is required to enable write capability. This mode supports a two wire bidirectional data transmission protocol. In this protocol, a device that sends data on the bus is defined to be the transmitter, and a device that receives data from the bus is defined to be the receiver. The bus must be controlled by a master device that generates the Bidirectional mode clock (SCL), controls access to the bus and generates the Start and Stop conditions, while the 24LC21 acts as the slave. Both master and slave can operate as transmitter or receiver, but the master device determines which mode is activated.

3.1 Bidirectional Mode Bus Characteristics

The following **bus protocol** has been defined:

- Data transfer may be initiated only when the bus is not busy.
- During data transfer, the data line must remain stable whenever the clock line is high. Changes in the data line while the clock line is high will be interpreted as a Start or Stop condition.

Accordingly, the following bus conditions have been defined (see Figure 3-2).

3.1.1 BUS NOT BUSY (A)

Both data and clock lines remain high.

3.1.2 START DATA TRANSFER (B)

A high-to-low transition of the SDA line while the clock (SCL) is high determines a Start condition. All commands must be preceded by a Start condition.

3.1.3 STOP DATA TRANSFER (C)

A low-to-high transition of the SDA line while the clock (SCL) is high determines a Stop condition. All operations must be ended with a Stop condition.

FIGURE 3-1: MODE TRANSITION

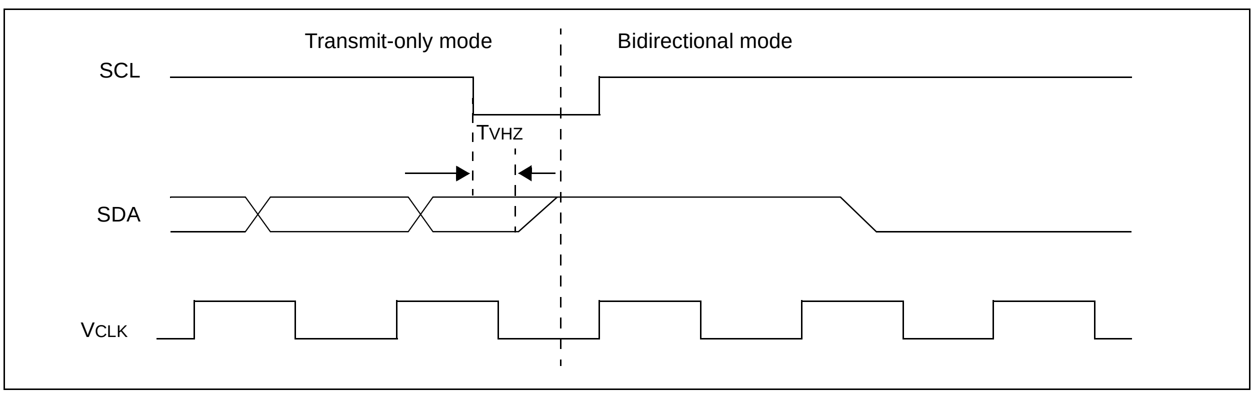
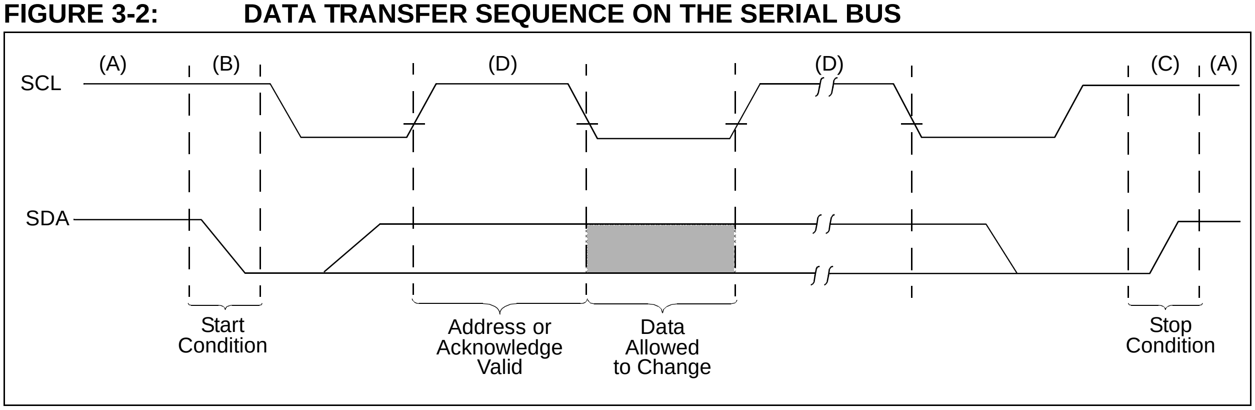


FIGURE 3-2: DATA TRANSFER SEQUENCE ON THE SERIAL BUS



3.1.4 DATA VALID (D)

The state of the data line represents valid data when, after a Start condition, the data line is stable for the duration of the high period of the clock signal.

The data on the line must be changed during the low period of the clock signal. There is one clock pulse per bit of data.

Each data transfer is initiated with a Start condition and terminated with a Stop condition. The number of the data bytes transferred between the Start and Stop conditions is determined by the master device and is theoretically unlimited, although only the last eight will be stored when doing a write operation. When an overwrite does occur, it will replace data in a first in first out fashion.

3.1.5 ACKNOWLEDGE

Each receiving device, when addressed, is obliged to generate an acknowledge after the reception of each byte. The master device must generate an extra clock pulse which is associated with this Acknowledge bit.

Note:	The 24LC21 does not generate any Acknowledge bits if an internal programming cycle is in progress.

The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable low during the high period of the acknowledge related clock pulse. Of course, setup and hold times must be taken into account. A master must signal an end of data to the slave by not generating an Acknowledge bit on the last byte that has been clocked out of the slave. In this case, the slave must leave the data line high to enable the master to generate the Stop condition.

FIGURE 3-3: BUS TIMING START/STOP

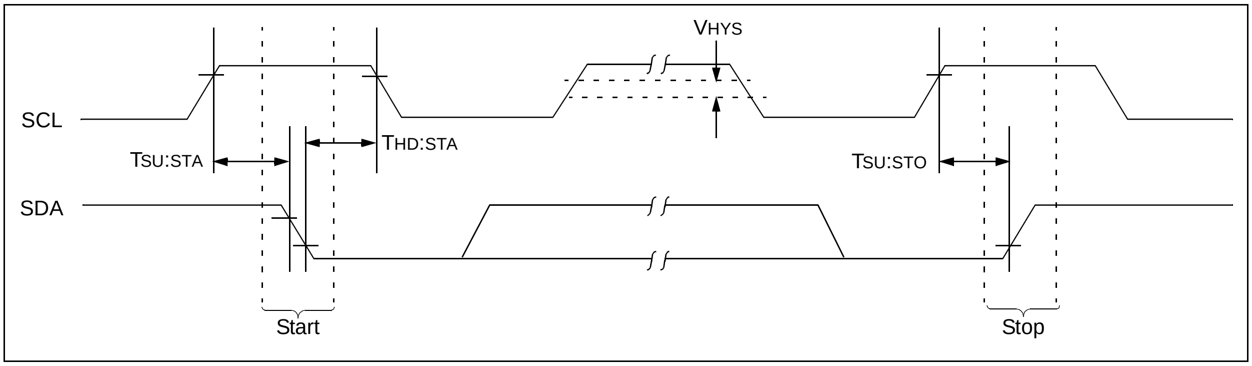
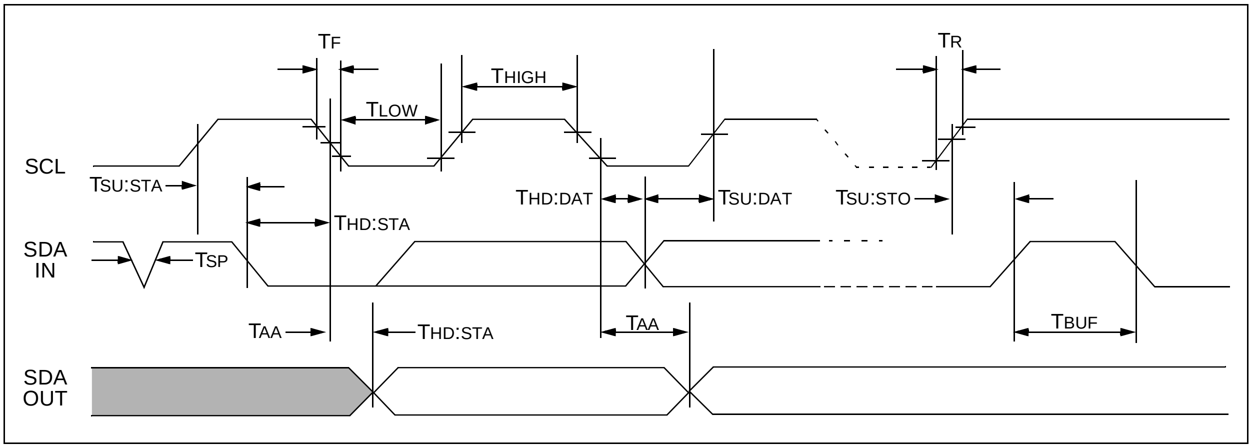


FIGURE 3-4: BUS TIMING DATA



3.1.6 SLAVE ADDRESS

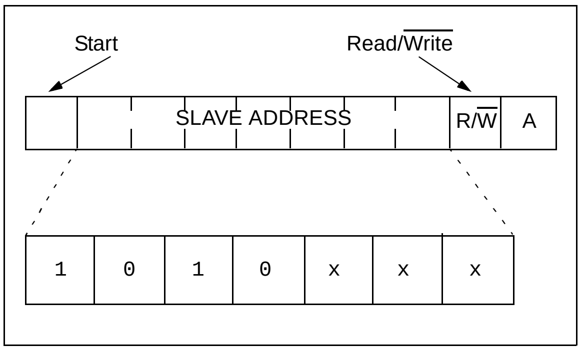
After generating a Start condition, the bus master transmits the slave address consisting of a 7-bit device code '1010' for the 24LC21, followed by three "don't care" bits.

The eighth bit of slave address determines if the master device wants to read or write to the 24LC21 (Figure 3-5).

The 24LC21 monitors the bus for its corresponding slave address all the time. It generates an Acknowledge bit if the slave address was true and it is not in a programming mode.

Operation	Control Code	Chip Select	$R/\overline{W}$
Read	1010	xxx	1
Write	1010	xxx	0

FIGURE 3-5: CONTROL BYTE ALLOCATION



4.0 WRITE OPERATION

4.1 Byte Write

Following the Start signal from the master, the slave address (4 bits), the "don't care" bits (3 bits) and the $R/\overline{W}$ bit which is a logic low, is placed onto the bus by the master transmitter. This indicates to the addressed slave receiver that a byte with a word address will follow after it has generated an Acknowledge bit during the ninth clock cycle. Therefore, the next byte transmitted by the master is the word address and will be written into the address pointer of the 24LC21. After receiving another Acknowledge signal from the 24LC21 the master device will transmit the data word to be written into the addressed memory location. The 24LC21 acknowledges again and the master generates a Stop condition. This initiates the internal write cycle, and during this time the 24LC21 will not generate Acknowledge signals (Figure 4-1).

It is required that V_{CLK} be held at a logic high level in order to program the device. This applies to byte write and page write operation. Note that V_{CLK} can go low while the device is in its self-timed program operation and not affect programming.

4.2 Page Write

The write control byte, word address and the first data byte are transmitted to the 24LC21 in the same way as in a byte write. But instead of generating a Stop condition the master transmits up to eight data bytes to the 24LC21, which are temporarily stored in the on-chip page buffer and will be written into the memory after the master has transmitted a Stop condition. After the receipt of each word, the three lower order address pointer bits are internally incremented by one. The higher order five bits of the word address remains constant. If the master should transmit more than eight words prior to generating the Stop condition, the address counter will roll over and the previously received data will be overwritten. As with the byte write operation, once the Stop condition is received an internal write cycle will begin (Figure 4-3).

It is required that VCLK be held at a logic high level in order to program the device. This applies to byte write and page write operation. Note that VCLK can go low while the device is in its self-timed program operation and not affect programming.

Note:	Page write operations are limited to writing bytes within a single physical page, **regardless** of the number of bytes actually being written. Physical page boundaries start at addresses that are integer multiples of the page buffer size (or 'page size') and end at addresses that are integer multiples of [page size - 1]. If a page Write command attempts to write across a physical page boundary, the result is that the data wraps around to the beginning of the current page (overwriting data previously stored there), instead of being written to the next page as might be expected. It is therefore necessary for the application software to prevent page write operations that would attempt to cross a page boundary.

FIGURE 4-1: BYTE WRITE

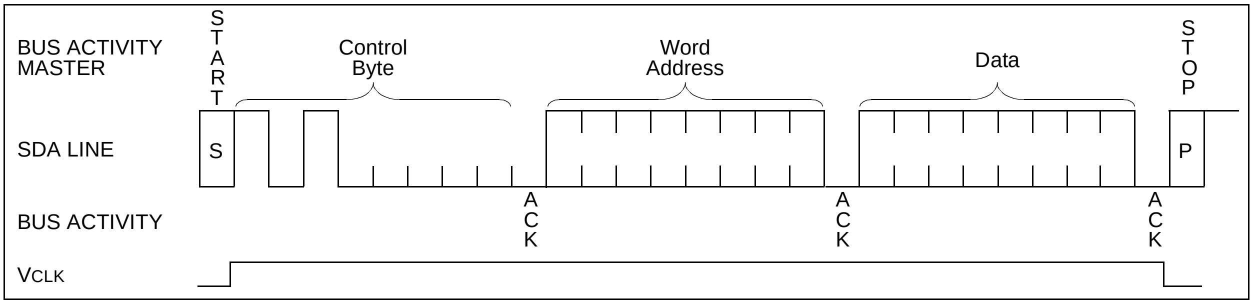


FIGURE 4-2: BYTE WRITE

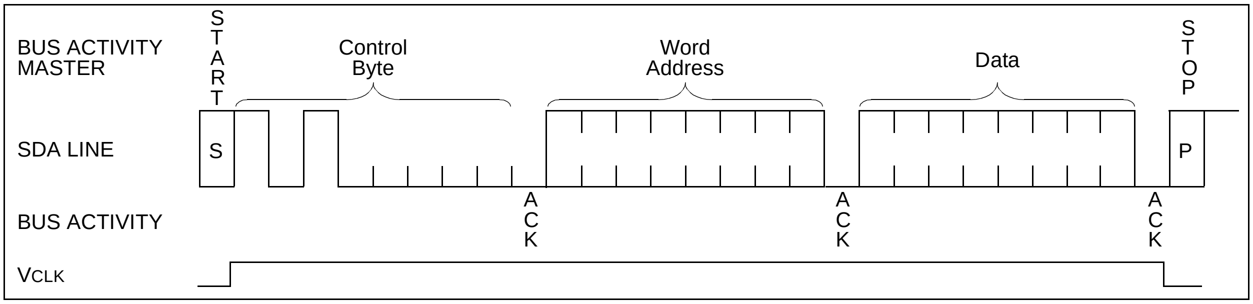
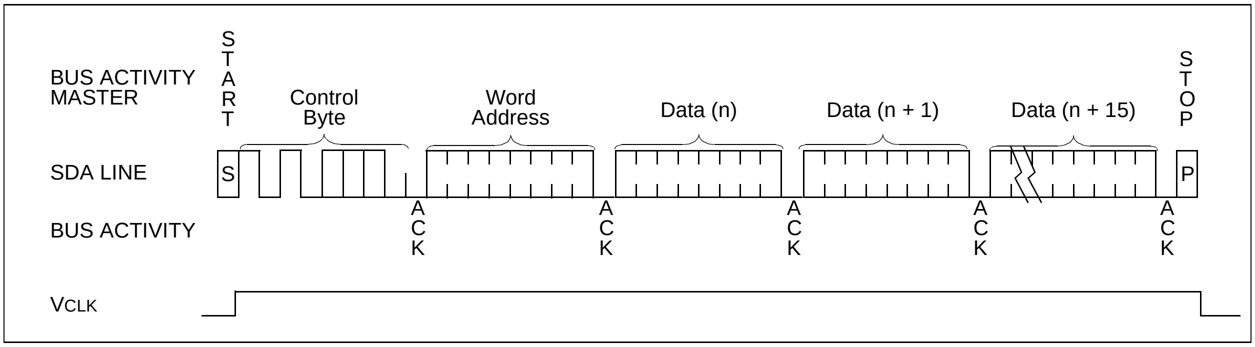


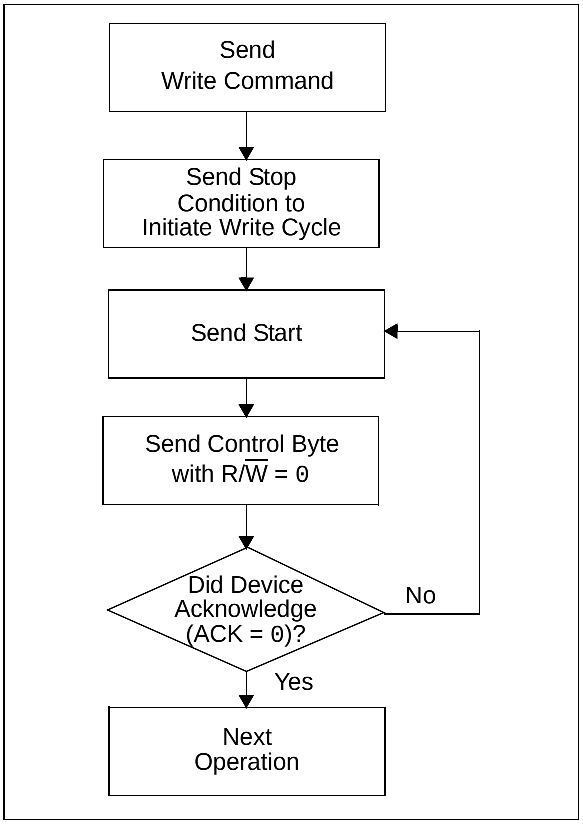
FIGURE 4-3: PAGE WRITE



5.0 ACKNOWLEDGE POLLING

Since the device will not acknowledge during a write cycle, this can be used to determine when the cycle is complete (this feature can be used to maximize bus throughput). Once the Stop condition for a Write command has been issued from the master, the device initiates the internally timed write cycle. ACK polling can be initiated immediately. This involves the master sending a Start condition followed by the control byte for a Write command (R/$\overline{W}$ = 0). If the device is still busy with the write cycle, then no ACK will be returned. If the cycle is complete, then the device will return the ACK and the master can then proceed with the next Read or Write command. See Figure 5-1 for the flow diagram.

FIGURE 5-1: ACKNOWLEDGE POLLING FLOW



6.0 WRITE PROTECTION

When using the 24LC21 in the Bidirectional mode, the VCLK pin operates as the write-protect control pin. Setting VCLK high allows normal write operations, while setting VCLK low prevents writing to any location in the array. Connecting the VCLK pin to VSS would allow the 24LC21 to operate as a serial ROM, although this configuration would prevent using the device in the Transmit-only mode.

7.0 READ OPERATION

Read operations are initiated in the same way as write operations with the exception that the R/$\overline{W}$ bit of the slave address is set to '1'. There are three basic types of read operations: current address read, random read and sequential read.

7.1 Current Address Read

The 24LC21 contains an address counter that maintains the address of the last word accessed, internally incremented by one. Therefore, if the previous access (either a read or write operation) was to address n, the next current address read operation would access data from address n + 1. Upon receipt of the slave address with R/$\overline{W}$ bit set to '1', the 24LC21 issues an acknowledge and transmits the eight bit data word. The master will not acknowledge the transfer but does generate a Stop condition and the 24LC21 discontinues transmission (Figure 7-1).

7.2 Random Read

Random read operations allow the master to access any memory location in a random manner. To perform this type of read operation, first the word address must be set. This is done by sending the word address to the 24LC21 as part of a write operation. After the word address is sent, the master generates a Start condition following the acknowledge. This terminates the write operation, but not before the internal address pointer is set. Then the master issues the control byte again but with the R/$\overline{W}$ bit set to a '1'. The 24LC21 will then issue an acknowledge and transmits the eight bit data word. The master will not acknowledge the transfer but does generate a Stop condition and the 24LC21 discontinues transmission (Figure 7-2).

7.3 Sequential Read

Sequential reads are initiated in the same way as a random read except that after the 24LC21 transmits the first data byte, the master issues an acknowledge as opposed to a Stop condition in a random read. This directs the 24LC21 to transmit the next sequentially addressed 8-bit word (see Figure 7-3).

To provide sequential reads the 24LC21 contains an internal address pointer which is incremented by one at the completion of each operation. This address pointer allows the entire memory contents to be serially read during one operation.

7.4 Noise Protection

The 24LC21 employs a VCC threshold detector circuit which disables the internal erase/write logic if the VCC is below 1.5 volts at nominal conditions.

The SCL and SDA inputs have Schmitt Trigger and filter circuits which suppress noise spikes to assure proper device operation even on a noisy bus.

FIGURE 7-1: CURRENT ADDRESS READ

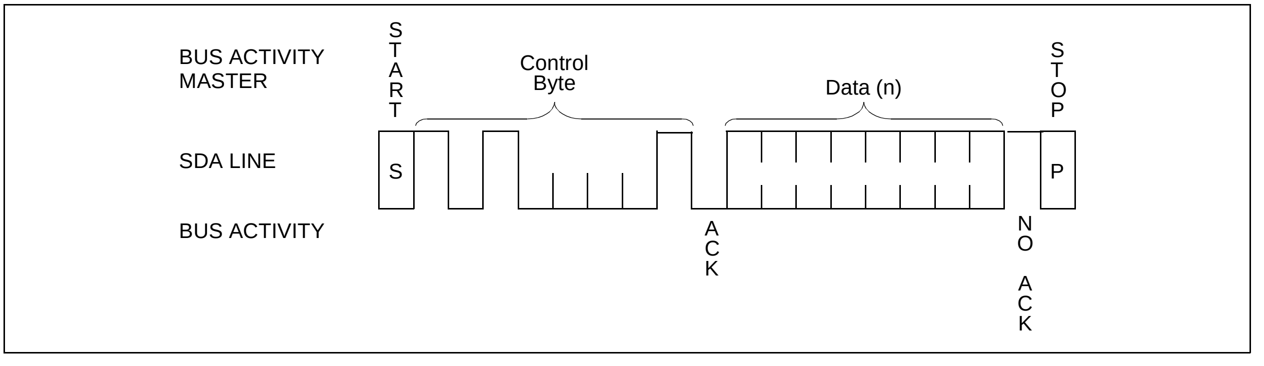


FIGURE 7-2: RANDOM READ

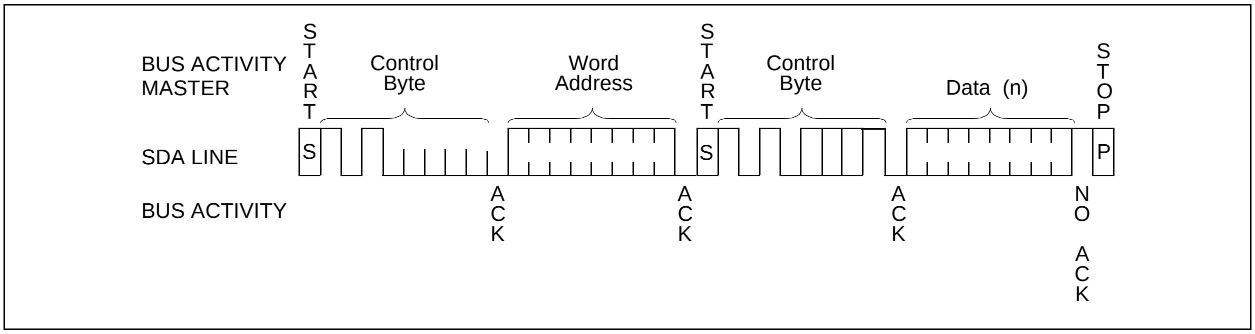
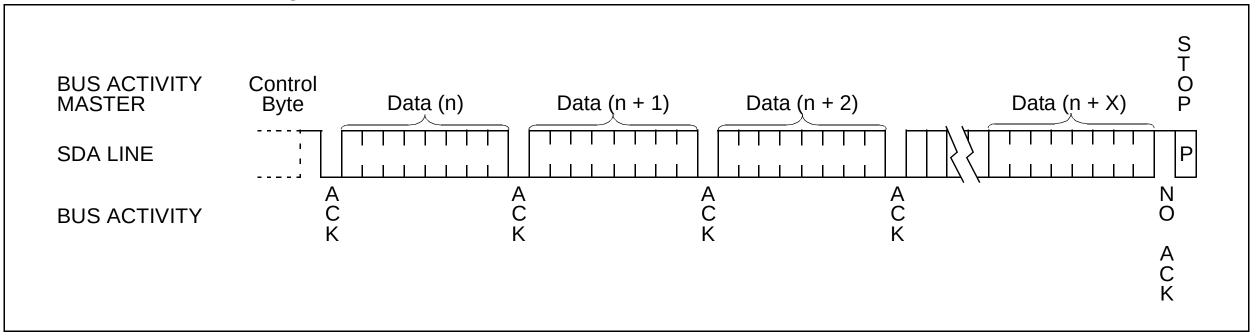


FIGURE 7-3: SEQUENTIAL READ



8.0 PIN DESCRIPTIONS

TABLE 8-1: PIN FUNCTION TABLE

Name	Function
VSS	Ground
SDA	Serial Address/Data I/O
SCL	Serial Clock (Bidirectional mode)
VCLK	Serial Clock (Transmit-only mode)
VCC	+2.5V to 5.5V Power Supply
NC	No Connection

8.1 SDA

This pin is used to transfer addresses and data into and out of the device, when the device is in the Bidirectional mode. In the Transmit-only mode, which only allows data to be read from the device, data is also transferred on the SDA pin. This pin is an open drain terminal, therefore the SDA bus requires a pull-up resistor to VCC (typical 10KΩ for 100 kHz, 2KΩ for 400 kHz).

For normal data transfer in the Bidirectional mode, SDA is allowed to change only during SCL low. Changes during SCL high are reserved for indicating the Start and Stop conditions.

8.2 SCL

This pin is the clock input for the Bidirectional mode, and is used to synchronize data transfer to and from the device. It is also used as the signaling input to switch the device from the Transmit-only mode to the Bidirectional mode. It must remain high for the chip to continue operation in the Transmit-only mode.

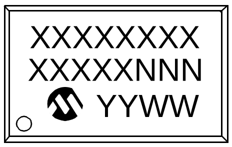
8.3 VCLK

This pin is the clock input for the Transmit-only mode. In the Transmit-only mode, each bit is clocked out on the rising edge of this signal. In the Bidirectional mode, a high logic level is required on this pin to enable write capability.

9.0 PACKAGING INFORMATION

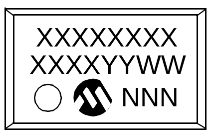
9.1 Package Marking Information

8-Lead PDIP

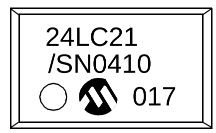


Example

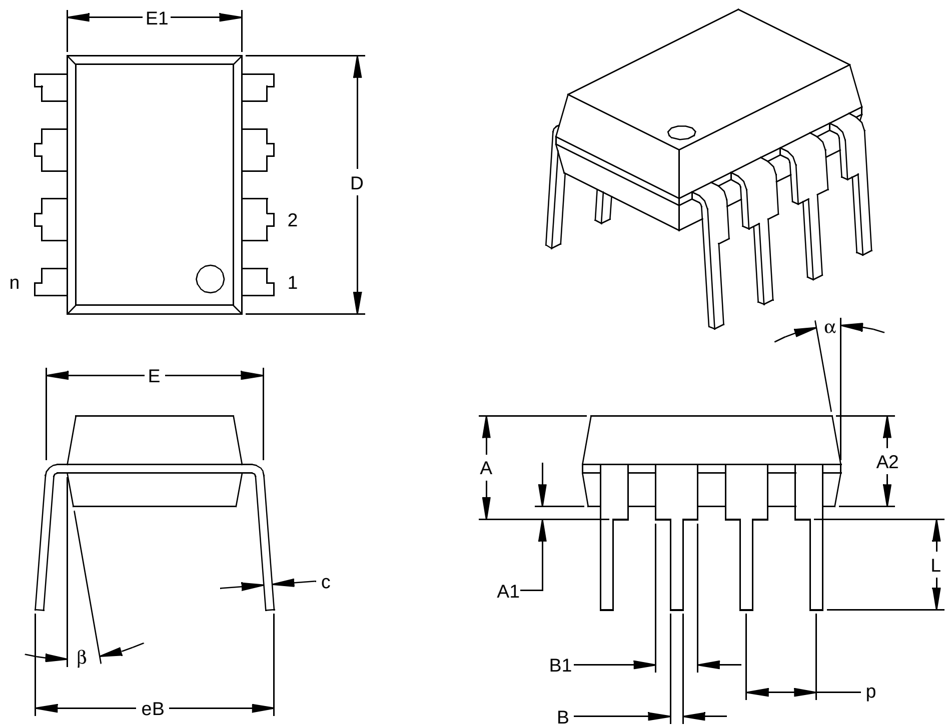
8-Lead SOIC (.150”)



Example



8-Lead Plastic Dual In-line (P) – 300 mil Body (PDIP)

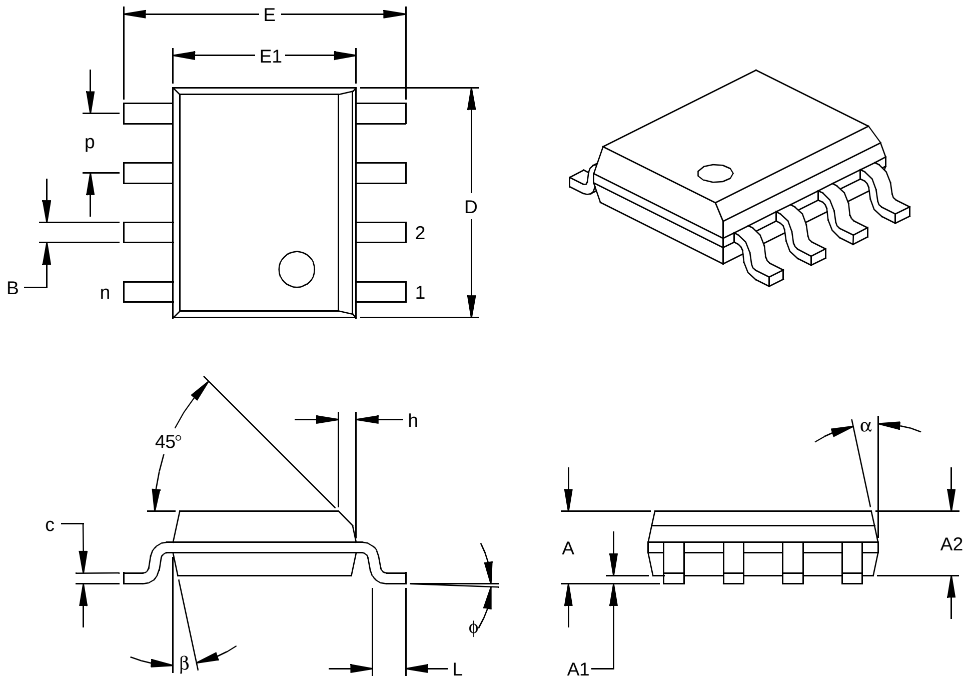


Units		INCHES*			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		8			8	
Pitch	p		.100			2.54	
Top to Seating Plane	A	.140	.155	.170	3.56	3.94	4.32
Molded Package Thickness	A2	.115	.130	.145	2.92	3.30	3.68
Base to Seating Plane	A1	.015			0.38		
Shoulder to Shoulder Width	E	.300	.313	.325	7.62	7.94	8.26
Molded Package Width	E1	.240	.250	.260	6.10	6.35	6.60
Overall Length	D	.360	.373	.385	9.14	9.46	9.78
Tip to Seating Plane	L	.125	.130	.135	3.18	3.30	3.43
Lead Thickness	c	.008	.012	.015	0.20	0.29	0.38
Upper Lead Width	B1	.045	.058	.070	1.14	1.46	1.78
Lower Lead Width	B	.014	.018	.022	0.36	0.46	0.56
Overall Row Spacing §	eB	.310	.370	.430	7.87	9.40	10.92
Mold Draft Angle Top	α	5	10	15	5	10	15
Mold Draft Angle Bottom	β	5	10	15	5	10	15

* Controlling Parameter
§ Significant Characteristic

Notes:
Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010” (0.254mm) per side.
JEDEC Equivalent: MS-001
Drawing No. C04-018

8-Lead Plastic Small Outline (SN) – Narrow, 150 mil Body (SOIC)



Units		INCHES*			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		8			8	
Pitch	p		.050			1.27	
Overall Height	A	.053	.061	.069	1.35	1.55	1.75
Molded Package Thickness	A2	.052	.056	.061	1.32	1.42	1.55
Standoff §	A1	.004	.007	.010	0.10	0.18	0.25
Overall Width	E	.228	.237	.244	5.79	6.02	6.20
Molded Package Width	E1	.146	.154	.157	3.71	3.91	3.99
Overall Length	D	.189	.193	.197	4.80	4.90	5.00
Chamfer Distance	h	.010	.015	.020	0.25	0.38	0.51
Foot Length	L	.019	.025	.030	0.48	0.62	0.76
Foot Angle	φ	0	4	8	0	4	8
Lead Thickness	c	.008	.009	.010	0.20	0.23	0.25
Lead Width	B	.013	.017	.020	0.33	0.42	0.51
Mold Draft Angle Top	α	0	12	15	0	12	15
Mold Draft Angle Bottom	β	0	12	15	0	12	15

* Controlling Parameter
§ Significant Characteristic

Notes:
Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" (0.254mm) per side.
JEDEC Equivalent: MS-012
Drawing No. C04-057

APPENDIX A: REVISION HISTORY

Revision J

Added note to page 1 header (Not recommended for new designs).

Added Section 9.0: Package Marking Information.

Added On-line Support page.

Updated document format.

NOTES:

ON-LINE SUPPORT

Microchip provides on-line support on the Microchip World Wide Web site.

The web site is used by Microchip as a means to make files and information easily available to customers. To view the site, the user must have access to the Internet and a web browser, such as Netscape® or Microsoft® Internet Explorer. Files are also available for FTP download from our FTP site.

Connecting to the Microchip Internet Web Site

The Microchip web site is available at the following URL:

www.microchip.com

The file transfer site is available by using an FTP service to connect to:

ftp://ftp.microchip.com

The web site and file transfer site provide a variety of services. Users may download files for the latest Development Tools, Data Sheets, Application Notes, User's Guides, Articles and Sample Programs. A variety of Microchip specific business information is also available, including listings of Microchip sales offices, distributors and factory representatives. Other data available for consideration is:

- Latest Microchip Press Releases
- Technical Support Section with Frequently Asked Questions
- Design Tips
- Device Errata
- Job Postings
- Microchip Consultant Program Member Listing
- Links to other useful web sites related to Microchip Products
- Conferences for products, Development Systems, technical information and more
- Listing of seminars and events

SYSTEMS INFORMATION AND UPGRADE HOT LINE

The Systems Information and Upgrade Line provides system users a listing of the latest versions of all of Microchip's development systems software products. Plus, this line provides information on how customers can receive the most current upgrade kits. The Hot Line Numbers are:

1-800-755-2345 for U.S. and most of Canada, and

1-480-792-7302 for the rest of the world.

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READER RESPONSE

It is our intention to provide you with the best documentation possible to ensure successful use of your Microchip product. If you wish to provide your comments on organization, clarity, subject matter, and ways in which our documentation can better serve you, please FAX your comments to the Technical Publications Manager at (480) 792-4150.

Please list the following information, and use this outline to provide us with your comments about this document.

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Device: 24LC21 Literature Number: DS21095J

Questions:

1. What are the best features of this document?

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2. How does this document meet your hardware and software development needs?

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3. Do you find the organization of this document easy to follow? If not, why?

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5. What deletions from the document could be made without affecting the overall usefulness?

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6. Is there any incorrect or misleading information (what and where)?

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PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	X	/XX	XXX
Device	Temperature Range	Package	Pattern

Device	24LC21: Dual Mode I^{2}C™ Serial EEPROM 24LC21T: Dual Mode I^{2}C™ Serial EEPROM (Tape and Reel)		
Temperature Range	Blank I	= =	0°C to +70°C -40°C to +85°C
Package	P SN	= =	Plastic DIP (300 mil Body), 8-lead Plastic SOIC (150 mil Body), 8-lead

Sales and Support

Data Sheets
Products supported by a preliminary Data Sheet may have an errata sheet describing minor operational differences and recommended workarounds. To determine if an errata sheet exists for a particular device, please contact one of the following:

1. Your local Microchip sales office
2. The Microchip Corporate Literature Center U.S. FAX: (480) 792-7277
3. The Microchip Worldwide Site (www.microchip.com)

Please specify which device, revision of silicon and Data Sheet (include Literature #) you are using.

New Customer Notification System
Register on our web site (www.microchip.com/cn) to receive the most current information on our products.

NOTES:

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Technical Support: 480-792-7627
Web Address: www.microchip.com

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Alpharetta, GA 30022
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Fax: 770-640-0307

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2 Lan Drive, Suite 120
Westford, MA 01886
Tel: 978-692-3848
Fax: 978-692-3821

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333 Pierce Road, Suite 180
Itasca, IL 60143
Tel: 630-285-0071
Fax: 630-285-0075

Dallas
4570 Westgrove Drive, Suite 160
Addison, TX 75001
Tel: 972-818-7423
Fax: 972-818-2924

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Tri-Atria Office Building
32255 Northwestern Highway, Suite 190
Farmington Hills, MI 48334
Tel: 248-538-2250
Fax: 248-538-2260

Kokomo
2767 S. Albright Road
Kokomo, IN 46902
Tel: 765-864-8360
Fax: 765-864-8387

Los Angeles
18201 Von Karman, Suite 1090
Irvine, CA 92612
Tel: 949-263-1888
Fax: 949-263-1338

San Jose
1300 Terra Bella Avenue
Mountain View, CA 94043
Tel: 650-215-1444
Fax: 650-961-0286

Toronto
6285 Northam Drive, Suite 108
Mississauga, Ontario L4V 1X5, Canada
Tel: 905-673-0699
Fax: 905-673-6509

ASIA/PACIFIC

Australia
Suite 22, 41 Rawson Street
Epping 2121, NSW
Australia
Tel: 61-2-9868-6733
Fax: 61-2-9868-6755

China - Beijing
Unit 706B
Wan Tai Bei Hai Bldg.
No. 6 Chaoyangmen Bei Str.
Beijing, 100027, China
Tel: 86-10-85282100
Fax: 86-10-85282104

China - Chengdu
Rm. 2401-2402, 24th Floor,
Ming Xing Financial Tower
No. 88 TIDU Street
Chengdu 610016, China
Tel: 86-28-86766200
Fax: 86-28-86766599

China - Fuzhou
Unit 28F, World Trade Plaza
No. 71 Wusi Road
Fuzhou 350001, China
Tel: 86-591-7503506
Fax: 86-591-7503521

China - Hong Kong SAR
Unit 901-6, Tower 2, Metroplaza
223 Hing Fong Road
Kwai Fong, N.T., Hong Kong
Tel: 852-2401-1200
Fax: 852-2401-3431

China - Shanghai
Room 701, Bldg. B
Far East International Plaza
No. 317 Xian Xia Road
Shanghai, 200051
Tel: 86-21-6275-5700
Fax: 86-21-6275-5060

China - Shenzhen
Rm. 1812, 18/F, Building A, United Plaza
No. 5022 Binhe Road, Futian District
Shenzhen 518033, China
Tel: 86-755-82901380
Fax: 86-755-8295-1393

China - Shunde
Room 401, Hongjian Building, No. 2
Fengxiangnan Road, Ronggui Town, Shunde District, Foshan City, Guangdong 528303, China
Tel: 86-757-28395507 Fax: 86-757-28395571

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Rm. B505A, Fullhope Plaza,
No. 12 Hong Kong Central Rd.
Qingdao 266071, China
Tel: 86-532-5027355 Fax: 86-532-5027205

India
Divyasree Chambers
1 Floor, Wing A (A3/A4)
No. 11, O'Shaugnessey Road
Bangalore, 560 025, India
Tel: 91-80-22290061 Fax: 91-80-22290062

Japan
Benex S-1 6F
3-18-20, Shinyokohama
Kohoku-Ku, Yokohama-shi
Kanagawa, 222-0033, Japan
Tel: 81-45-471- 6166 Fax: 81-45-471-6122

Korea
168-1, Youngbo Bldg. 3 Floor
Samsung-Dong, Kangnam-Ku
Seoul, Korea 135-882
Tel: 82-2-554-7200 Fax: 82-2-558-5932 or 82-2-558-5934

Singapore
200 Middle Road
#07-02 Prime Centre
Singapore, 188980
Tel: 65-6334-8870 Fax: 65-6334-8850

Taiwan
Kaohsiung Branch
30F - 1 No. 8
Min Chuan 2nd Road
Kaohsiung 806, Taiwan
Tel: 886-7-536-4818
Fax: 886-7-536-4803

Taiwan
Taiwan Branch
11F-3, No. 207
Tung Hua North Road
Taipei, 105, Taiwan
Tel: 886-2-2717-7175 Fax: 886-2-2545-0139

EUROPE

Austria
Durisolstrasse 2
A-4600 Wels
Austria
Tel: 43-7242-2244-399
Fax: 43-7242-2244-393

Denmark
Regus Business Centre
Lautrup hoj 1-3
Ballerup DK-2750 Denmark
Tel: 45-4420-9895 Fax: 45-4420-9910

France
Parc d'Activite du Moulin de Massy
43 Rue du Saule Trapu
Batiment A - ler Etage
91300 Massy, France
Tel: 33-1-69-53-63-20
Fax: 33-1-69-30-90-79

Germany
Steinheilstrasse 10
D-85737 Ismaning, Germany
Tel: 49-89-627-144-0
Fax: 49-89-627-144-44

Italy
Via Quasimodo, 12
20025 Legnano (MI)
Milan, Italy
Tel: 39-0331-742611
Fax: 39-0331-466781

Netherlands
Waegenburghtplein 4
NL-5152 JR, Drunen, Netherlands
Tel: 31-416-690399
Fax: 31-416-690340

United Kingdom
505 Eskdale Road
Winnersh Triangle
Wokingham
Berkshire, England RG41 5TU
Tel: 44-118-921-5869
Fax: 44-118-921-5820

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