FAIRCHILD
SEMICONDUCTOR®

December 2013

FDP7N60NZ / FDPF7N60NZ

N-Channel UniFET^{TM} II MOSFET

600 V, 6.5 A, 1.25 Ω

Features

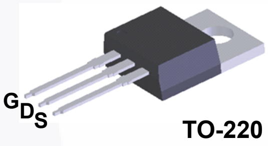
- $R_{DS(on)}$ = 1.05 Ω (Typ.) @ V_{GS} = 10 V, I_D = 3.25 A
- Low Gate Charge (Typ. 13 nC)
- Low C_{rss} (Typ. 7 pF)
- 100% Avalanche Tested
- Improved dv/dt Capability
- ESD Improved Capability
- RoHS Compliant

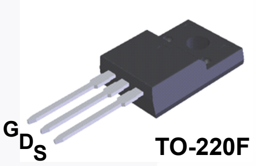
Applications

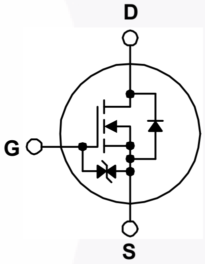
- LCD/ LED/ PDP TV
- Lighting
- Uninterruptible Power Supply
- AC-DC Power Supply

Description

UniFET^{TM} II MOSFET is Fairchild Semiconductor's high voltage MOSFET family based on advanced planar stripe and DMOS technology. This advanced MOSFET family has the smallest on-state resistance among the planar MOSFET, and also provides superior switching performance and higher avalanche energy strength. In addition, internal gate-source ESD diode allows UniFET II MOSFET to withstand over 2kV HBM surge stress. This device family is suitable for switching power converter applications such as power factor correction (PFC), flat panel display (FPD) TV power, ATX and electronic lamp ballasts.







MOSFET Maximum Ratings T_C = 25°C unless otherwise noted.

Symbol	Parameter		FDP7N60NZ	FDPF7N60NZ / FDPF7N60NZT	Unit
V_{DSS}	Drain to Source Voltage		600		V
V_{GSS}	Gate to Source Voltage		±30		V
I_D	Drain Current	- Continuous (T_C = 25°C)	6.5	6.5*	A
		- Continuous (T_C = 100°C)	3.9	3.9*	
I_{DM}	Drain Current	- Pulsed (Note 1)	26	26*	A
E_{AS}	Single Pulsed Avalanche Energy	(Note 2)	275		mJ
I_{AR}	Avalanche Current	(Note 1)	6.5		A
E_{AR}	Repetitive Avalanche Energy	(Note 1)	14.7		mJ
dv/dt	Peak Diode Recovery dv/dt	(Note 3)	10		V/ns
P_D	Power Dissipation	(T_C = 25°C)	147	33	W
		- Derate Above 25°C	1.2	0.26	W/°C
T_J, T_{STG}	Operating and Storage Temperature Range		-55 to +150		°C
T_L	Maximum Lead Temperature for Soldering, 1/8" from Case for 5 Seconds		300		°C

*Drain current limited by maximum junction temperature.

Thermal Characteristics

Symbol	Parameter	FDP7N60NZ	FDPF7N60NZ / FDPF7N60NZT	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case, Max.	0.85	3.8	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient, Max.	62.5	62.5	

Package Marking and Ordering Information

Part Number	Top Mark	Package	Packing Method	Reel Size	Tape Width	Quantity
FDP7N60NZ	FDP7N60NZ	TO-220	Tube	N/A	N/A	50 units
FDPF7N60NZ	FDPF7N60NZ	TO-220F	Tube	N/A	N/A	50 units
FDPF7N60NZT	FDPF7N60NZ	TO-220F	Tube	N/A	N/A	50 units

Electrical Characteristics $T_C = 25^oC$ unless otherwise noted.

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Off Characteristics						
BV_{DSS}	Drain to Source Breakdown Voltage	$I_D = 250\ \mu A$, $V_{GS} = 0\ V$, $T_J = 25^oC$	600	-	-	V
$\Delta BV_{DSS} / \Delta T_J$	Breakdown Voltage Temperature Coefficient	$I_D = 250\ \mu A$, Referenced to 25^oC	-	0.6	-	V/°C
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 600\ V$, $V_{GS} = 0\ V$	-	-	1	µA
		$V_{DS} = 480\ V$, $T_C = 125^oC$	-	-	10	
I_{GSS}	Gate to Body Leakage Current	$V_{GS} = \pm 25\ V$, $V_{DS} = 0\ V$	-	-	±10	µA
On Characteristics						
$V_{GS(th)}$	Gate Threshold Voltage	$V_{GS} = V_{DS}$, $I_D = 250\ \mu A$	3	-	5	V
$R_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = 10\ V$, $I_D = 3.25\ A$	-	1.05	1.25	Ω
g_{FS}	Forward Transconductance	$V_{DS} = 20\ V$, $I_D = 3.25\ A$	-	7.3	-	S
Dynamic Characteristics						
C_{iss}	Input Capacitance	$V_{DS} = 25\ V$, $V_{GS} = 0\ V$, $f = 1\ MHz$	-	550	730	pF
C_{oss}	Output Capacitance		-	70	90	pF
C_{rss}	Reverse Transfer Capacitance		-	7	10	pF
$Q_{g(tot)}$	Total Gate Charge at 10V	$V_{DS} = 480\ V$, $I_D = 6.5\ A$, $V_{GS} = 10\ V$ (Note 4)	-	13	17	nC
Q_{gs}	Gate to Source Gate Charge		-	3	-	nC
Q_{gd}	Gate to Drain “Miller” Charge		-	5.6	-	nC
Switching Characteristics						
$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 300\ V$, $I_D = 6.5\ A$, $V_{GS} = 10\ V$, $R_G = 25\ \Omega$ (Note 4)	-	17.5	45	ns
t_r	Turn-On Rise Time		-	30	70	ns
$t_{d(off)}$	Turn-Off Delay Time		-	40	90	ns
t_f	Turn-Off Fall Time		-	25	60	ns
Drain-Source Diode Characteristics						
I_S	Maximum Continuous Drain to Source Diode Forward Current		-	-	6.5	A
I_{SM}	Maximum Pulsed Drain to Source Diode Forward Current		-	-	26	A
V_{SD}	Drain to Source Diode Forward Voltage	$V_{GS} = 0\ V$, $I_{SD} = 6.5\ A$	-	-	1.4	V
t_{rr}	Reverse Recovery Time	$V_{GS} = 0\ V$, $I_{SD} = 6.5\ A$, $dI_F/dt = 100\ A/\mu s$	-	250	-	ns
Q_{rr}	Reverse Recovery Charge		-	1.4	-	µC

Notes:

1: Repetitive rating: pulse-width limited by maximum junction temperature.

2: $L = 13\ mH$, $I_{AS} = 6.5\ A$, $V_{DD} = 50\ V$, $R_G = 25\ \Omega$, starting $T_J = 25°C$.

3: $I_{SD} \leq 6.5\ A$, $di/dt \leq 200\ A/\mu s$, $V_{DD} \leq BV_{DSS}$, starting $T_J = 25°C$.

4: Essentially independent of operating temperature typical characteristics.

Typical Performance Characteristics

Figure 1. On-Region Characteristics

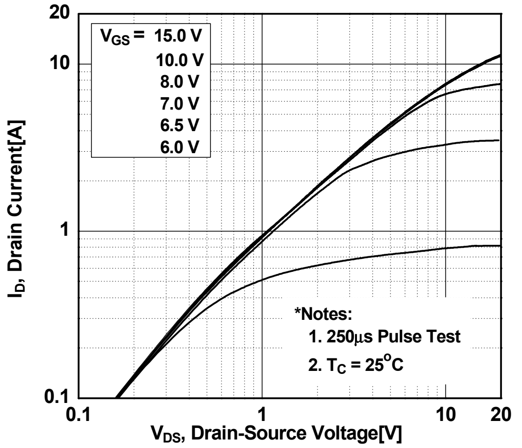


Figure 2. Transfer Characteristics

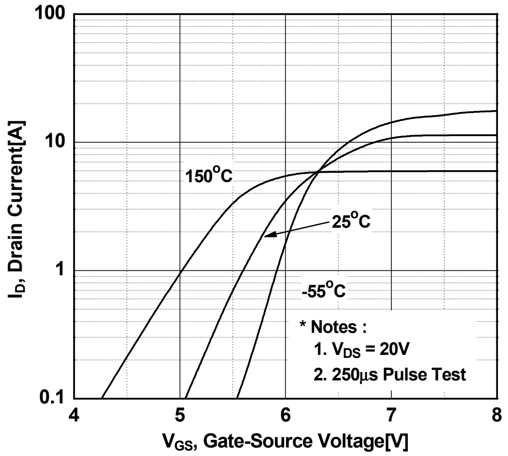


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

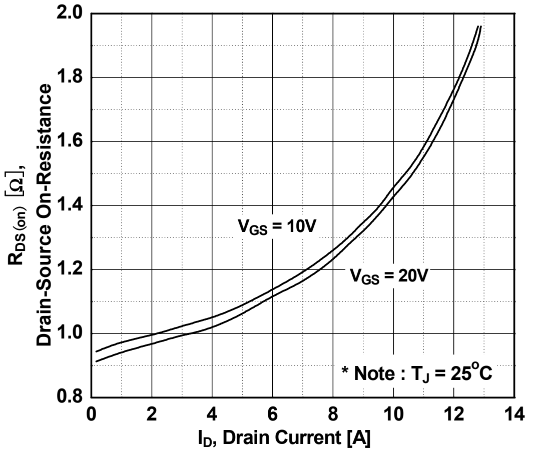


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

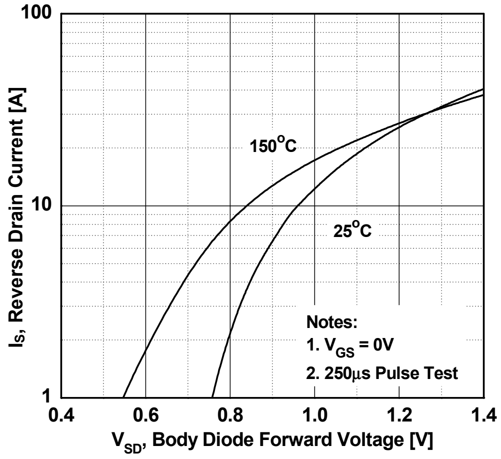


Figure 5. Capacitance Characteristics

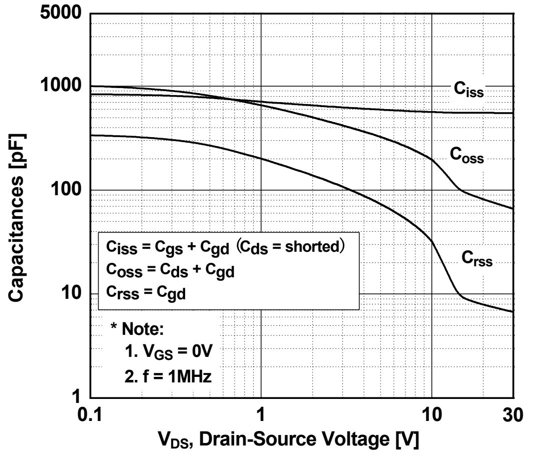
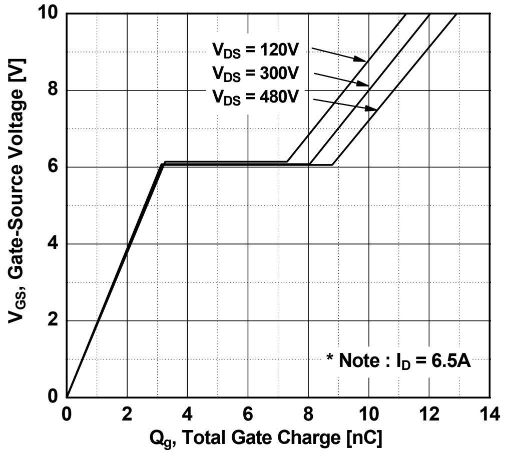


Figure 6. Gate Charge Characteristics



Typical Performance Characteristics (Continued)

Figure 7. Breakdown Voltage Variation vs. Temperature

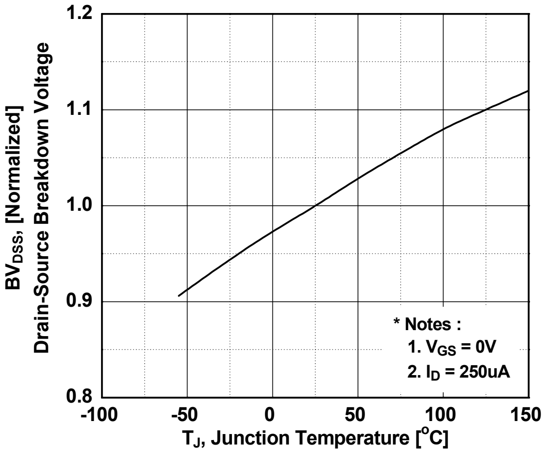


Figure 8. On-Resistance Variation vs Temperature

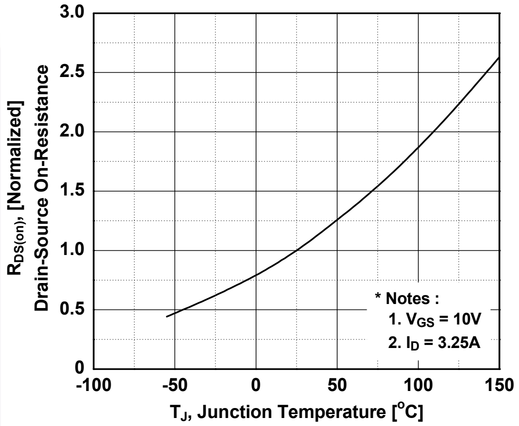


Figure 9. Maximum Safe Operating Area - FDPF7N60NZ / FDPF7N60NZT

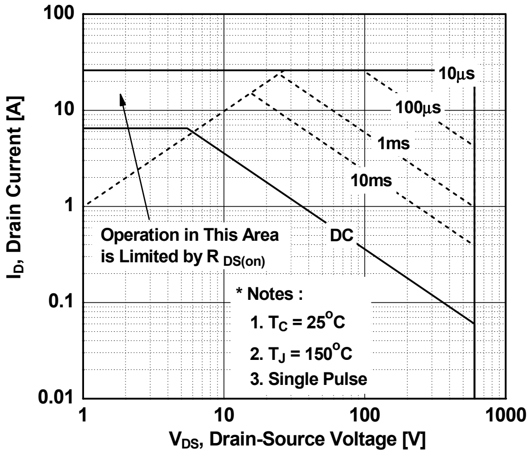


Figure 10. Maximum Safe Operating Area - FDP7N60NZ

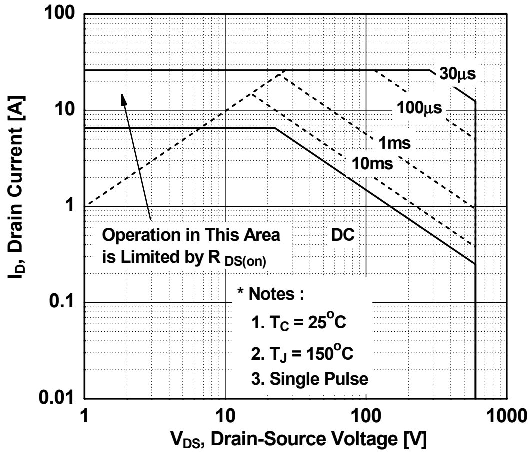
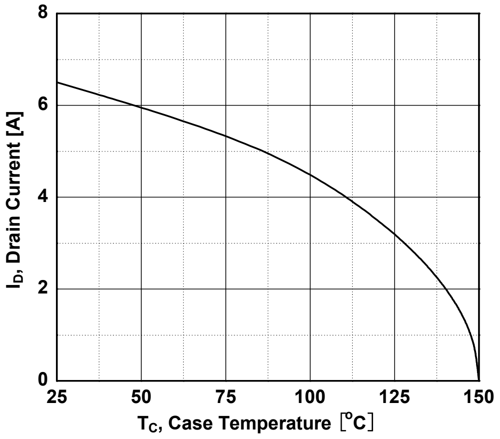


Figure 11. Maximum Drain Current vs. Case Temperature



Typical Performance Characteristics (Continued)

Figure 12. Transient Thermal Response Curve - FDPF7N60NZ / FDPF7N60NZT

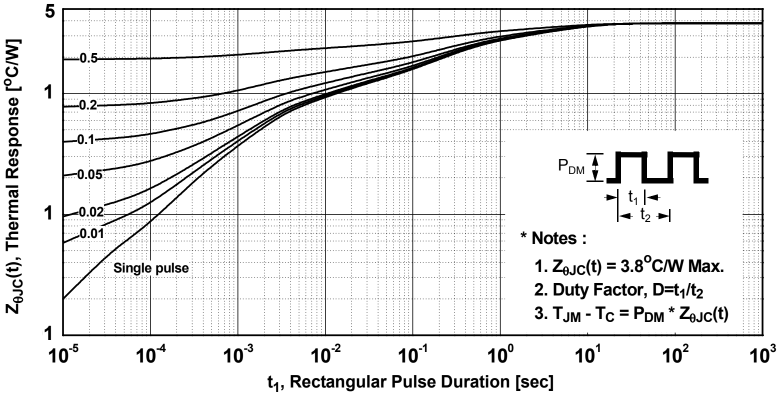
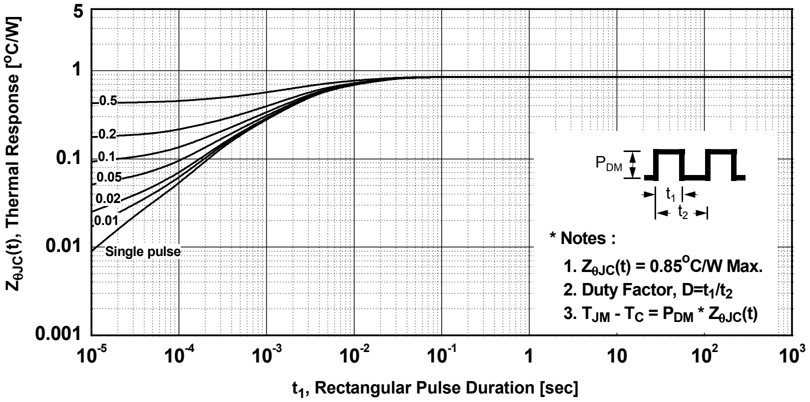


Figure 13. Transient Thermal Response Curve - FDP7N60NZ



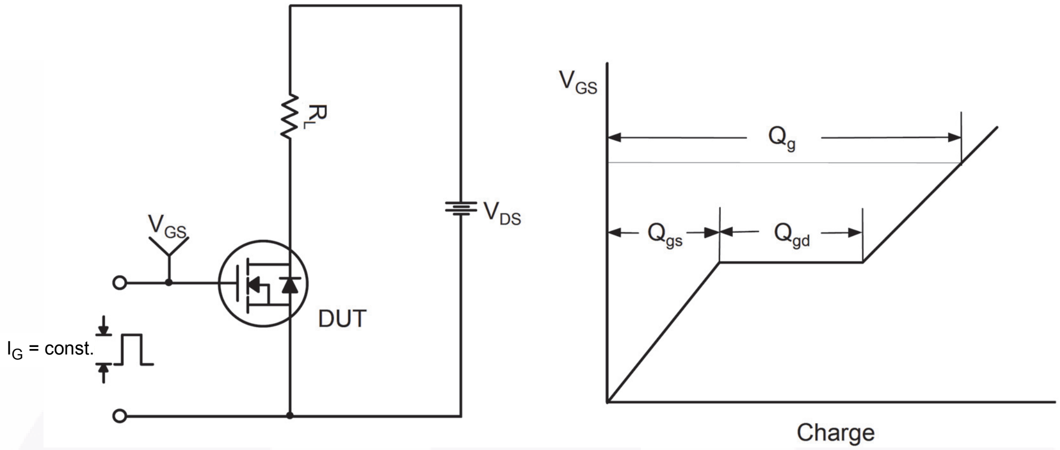


Figure 14. Gate Charge Test Circuit & Waveform

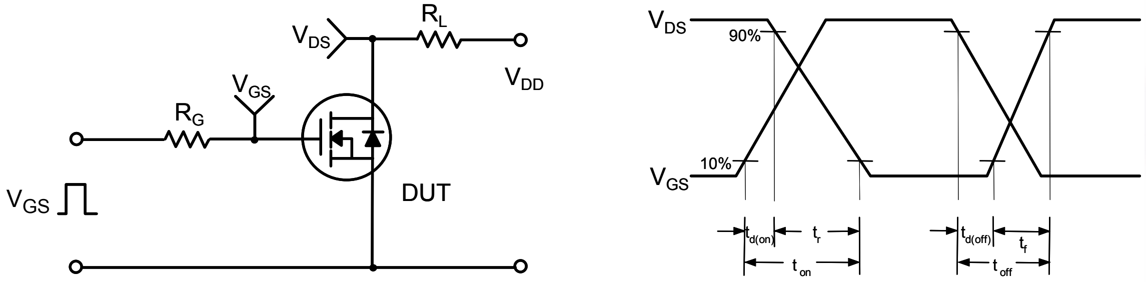


Figure 15. Resistive Switching Test Circuit & Waveforms

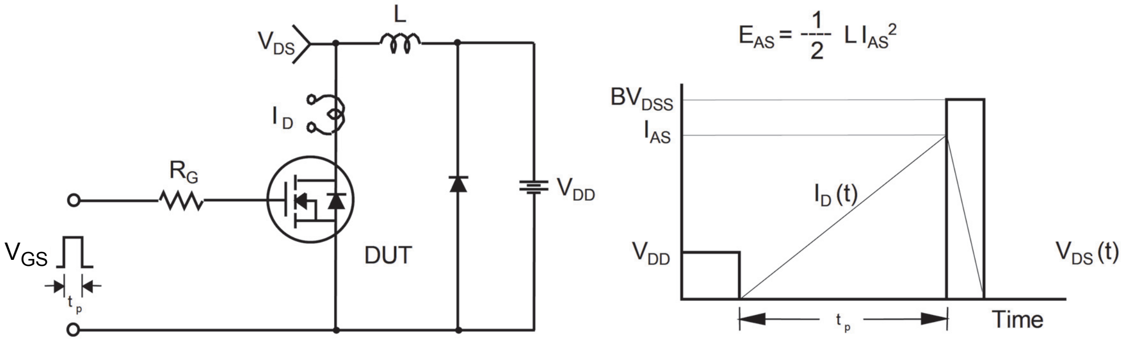


Figure 16. Unclamped Inductive Switching Test Circuit & Waveforms

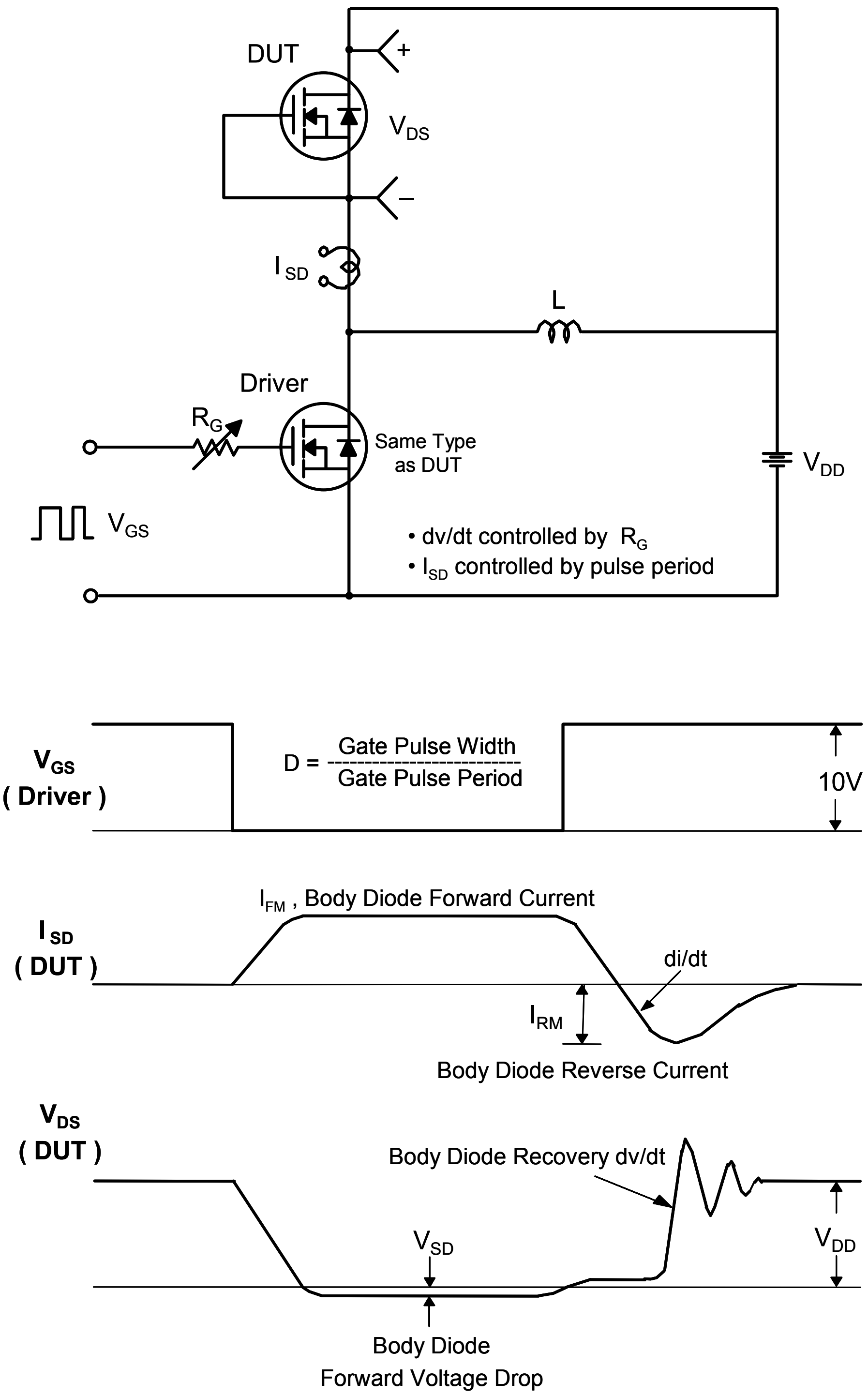
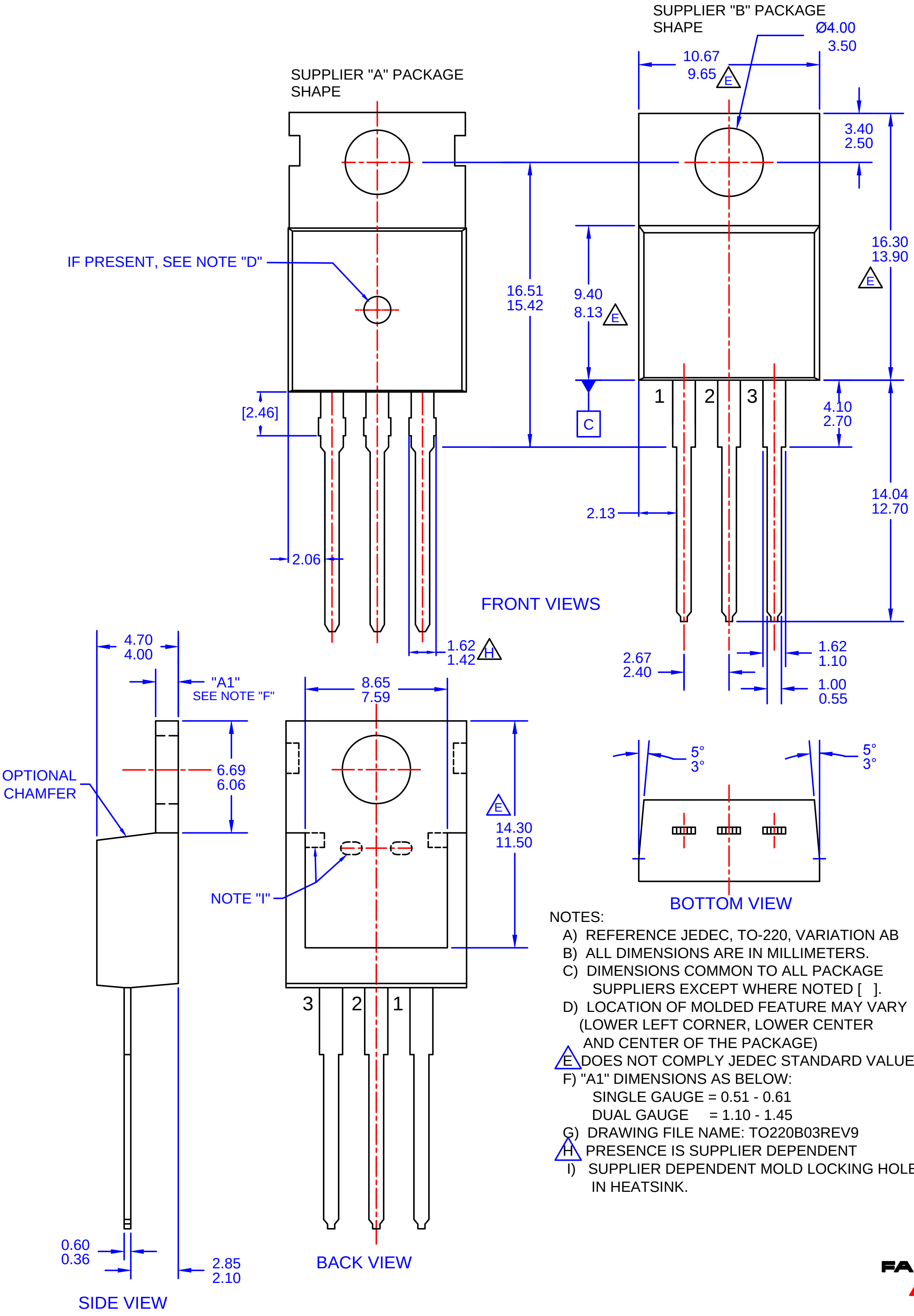
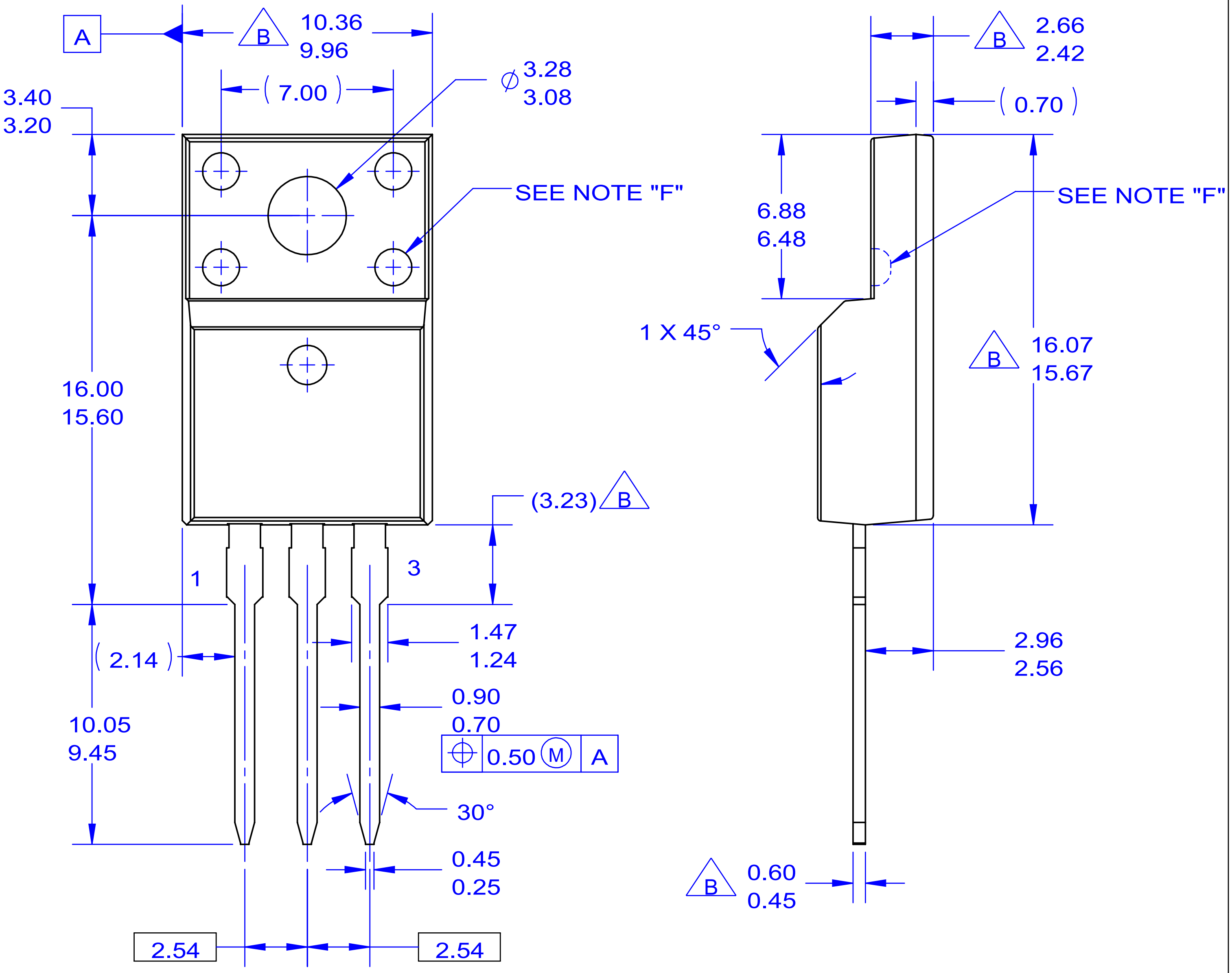
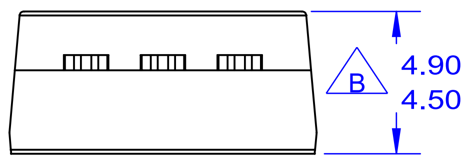


Figure 17. Peak Diode Recovery dv/dt Test Circuit & Waveforms



NOTES:
- A) REFERENCE JEDEC, TO-220, VARIATION AB
- B) ALL DIMENSIONS ARE IN MILLIMETERS.
- C) DIMENSIONS COMMON TO ALL PACKAGE SUPPLIERS EXCEPT WHERE NOTED [ ].
- D) LOCATION OF MOLDED FEATURE MAY VARY (LOWER LEFT CORNER, LOWER CENTER AND CENTER OF THE PACKAGE)
- E DOES NOT COMPLY JEDEC STANDARD VALUE.
- F) "A1" DIMENSIONS AS BELOW:
  - SINGLE GAUGE = 0.51 - 0.61
  - DUAL GAUGE = 1.10 - 1.45
- G) DRAWING FILE NAME: TO220B03REV9
- H PRESENCE IS SUPPLIER DEPENDENT
- I) SUPPLIER DEPENDENT MOLD LOCKING HOLES IN HEATSINK.





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NOTES:

A. EXCEPT WHERE NOTED CONFORMS TO EIAJ SC91A.

△B DOES NOT COMPLY EIAJ STD. VALUE.

C. ALL DIMENSIONS ARE IN MILLIMETERS.

D. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH AND TIE BAR PROTRUSIONS.

E. DIMENSION AND TOLERANCE AS PER ASME Y14.5-1994.

F. OPTION 1 - WITH SUPPORT PIN HOLE.
OPTION 2 - NO SUPPORT PIN HOLE.

G. DRAWING FILE NAME: TO220M03REV5

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