

## 1. Feature List

The EFM8SB1 highlighted features are listed below.

- Core:
  - Pipelined CIP-51 Core
  - Fully compatible with standard 8051 instruction set
  - 70% of instructions execute in 1-2 clock cycles
  - 25 MHz maximum operating frequency
- Memory:
  - Up to 8 kB flash memory, in-system re-programmable from firmware.
  - Up to 512 bytes RAM (including 256 bytes standard 8051 RAM and 256 bytes on-chip XRAM)
- Power:
  - Internal LDO regulator for CPU core voltage
  - Power-on reset circuit and brownout detectors
- I/O: Up to 17 total multifunction I/O pins:
  - Flexible peripheral crossbar for peripheral routing
  - 5 mA source, 12.5 mA sink allows direct drive of LEDs
- Clock Sources:
  - Internal 20 MHz low power oscillator with  $\pm 10\%$  accuracy
  - Internal 24.5 MHz precision oscillator with  $\pm 2\%$  accuracy
  - Internal 16.4 kHz low-frequency oscillator or RTC 32 kHz crystal (RTC crystal not available on CSP16 packages)
  - External crystal, RC, C, and CMOS clock options
- Timers/Counters and PWM:
  - 32-bit Real Time Clock (RTC)
  - 3-channel Programmable Counter Array (PCA) supporting PWM, capture/compare, and frequency output modes with watchdog timer function
  - 4 x 16-bit general-purpose timers
- Communications and Digital Peripherals:
  - UART
  - SPI™ Master / Slave
  - SMBus™ / I2C™ Master / Slave
  - 16-bit CRC unit, supporting automatic CRC of flash at 256-byte boundaries
- Analog:
  - Capacitive Sense (CS0)
  - Programmable current reference (IREF0)
  - 12-Bit Analog-to-Digital Converter (ADC0)
  - 1 x Low-current analog comparator
- On-Chip, Non-Intrusive Debugging
  - Full memory and register inspection
  - Four hardware breakpoints, single-stepping
- Pre-loaded UART bootloader
- Temperature range -40 to 85 °C
- Single power supply 1.8 to 3.6 V
- QSOP24, QFN24, QFN20, and CSP16 packages

With on-chip power-on reset, voltage supply monitor, watchdog timer, and clock oscillator, the EFM8SB1 devices are truly standalone system-on-a-chip solutions. The flash memory is reprogrammable in-circuit, providing non-volatile data storage and allowing field upgrades of the firmware. The on-chip debugging interface (C2) allows non-intrusive (uses no on-chip resources), full speed, in-circuit debugging using the production MCU installed in the final application. This debug logic supports inspection and modification of memory and registers, setting breakpoints, single stepping, and run and halt commands. All analog and digital peripherals are fully functional while debugging. Each device is specified for 1.8 to 3.6 V operation. Devices are AEC-Q100 qualified (Grade 3) and are available in 16-pin CSP, 20-pin QFN, 24-pin QFN, or 24-pin QSOP packages. All package options are lead-free and RoHS compliant.

**Note:** CSP devices can be handled and soldered using industry standard surface mount assembly techniques. However, because CSP devices are essentially a piece of silicon and are not encapsulated in plastic, they are susceptible to mechanical damage and may be sensitive to light. When CSP packages must be used in an environment exposed to light, it may be necessary to cover the top and sides with an opaque material.

## 2. Ordering Information

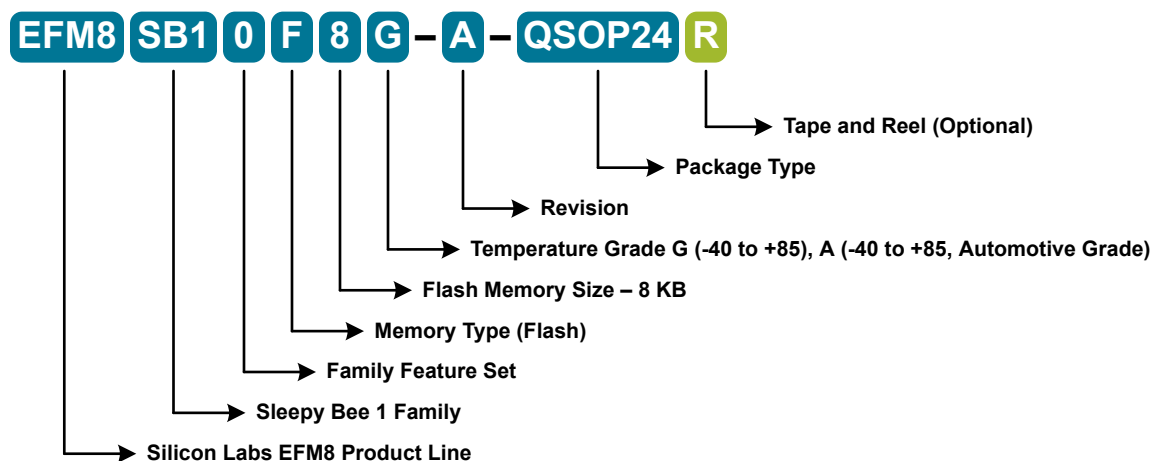


Figure 2.1. EFM8SB1 Part Numbering

All EFM8SB1 family members have the following features:

- CIP-51 Core running up to 25 MHz
- Three Internal Oscillators (24.5 MHz, 20 MHz, and 16 kHz)
- SMBus / I2C
- SPI
- UART
- 3-Channel Programmable Counter Array (PWM, Clock Generation, Capture/Compare)
- 4 16-bit Timers
- Analog Comparator
- 6-bit current source reference
- 12-bit Analog-to-Digital Converter with integrated multiplexer, voltage reference, and temperature sensor
- 16-bit CRC Unit
- AEC-Q100 qualified (Grade 3)
- Pre-loaded UART bootloader

In addition to these features, each part number in the EFM8SB1 family has a set of features that vary across the product line. The product selection guide shows the features available on each family member.

Table 2.1. Product Selection Guide

| Ordering Part Number | Flash Memory (kB) | RAM (Bytes) | Digital Port I/Os (Total) | ADC0 Channels | Capacitive Touch Inputs | Pb-free (RoHS Compliant) | Temperature Range | Package |
|----------------------|-------------------|-------------|---------------------------|---------------|-------------------------|--------------------------|-------------------|---------|
| EFM8SB10F8G-A-QSOP24 | 8                 | 512         | 17                        | 10            | 14                      | Yes                      | -40 to +85 C      | QSOP24  |
| EFM8SB10F8G-A-QFN24  | 8                 | 512         | 17                        | 10            | 14                      | Yes                      | -40 to +85 C      | QFN24   |
| EFM8SB10F8G-A-QFN20  | 8                 | 512         | 16                        | 9             | 13                      | Yes                      | -40 to +85 C      | QFN20G  |
| EFM8SB10F8G-A-CSP16  | 8                 | 512         | 13                        | 9             | 12                      | Yes                      | -40 to +85 C      | CSP16   |
| EFM8SB10F4G-A-QFN20  | 4                 | 512         | 16                        | 9             | 13                      | Yes                      | -40 to +85 C      | QFN20G  |

| Ordering Part Number | Flash Memory (kB) | RAM (Bytes) | Digital Port I/Os (Total) | ADC0 Channels | Capacitive Touch Inputs | Pb-free (RoHS Compliant) | Temperature Range | Package |
|----------------------|-------------------|-------------|---------------------------|---------------|-------------------------|--------------------------|-------------------|---------|
| EFM8SB10F2G-A-QFN20  | 2                 | 256         | 16                        | 9             | 13                      | Yes                      | -40 to +85 C      | QFN20G  |
| EFM8SB10F8A-A-QFN24  | 8                 | 512         | 17                        | 10            | 14                      | Yes                      | -40 to +85 C      | QFN24   |
| EFM8SB10F8A-A-QFN20  | 8                 | 512         | 16                        | 9             | 13                      | Yes                      | -40 to +85 C      | QFN20A  |

The A-grade (i.e. EFM8SB10F8A-A-QFN20) devices receive full automotive quality production status, including AEC-Q100 qualification, registration with International Material Data System (IMDS), and Part Production Approval Process (PPAP) documentation. PPAP documentation is available at [www.silabs.com](http://www.silabs.com) with a registered and NDA approved user account.

### 3. System Overview

#### 3.1 Introduction

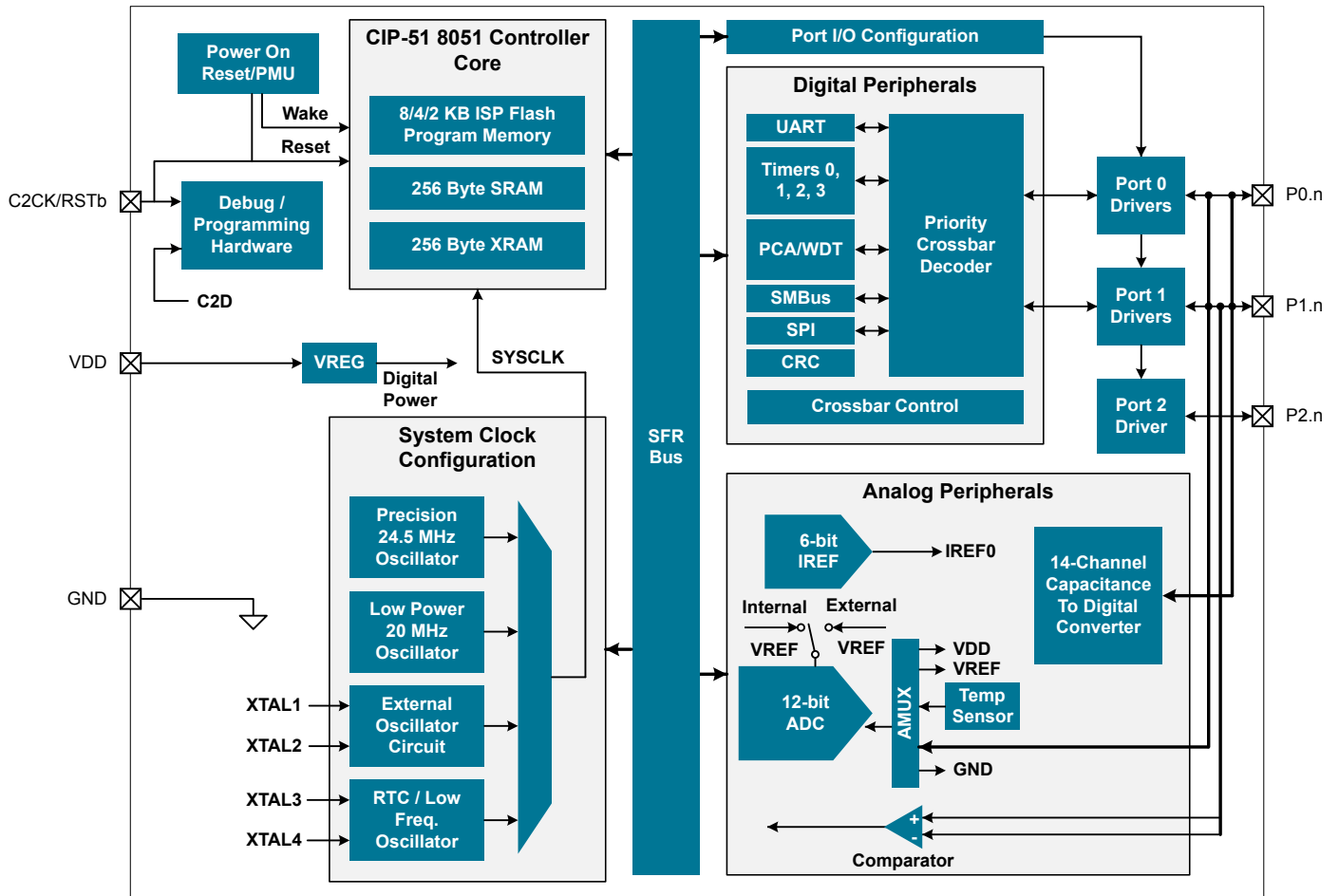


Figure 3.1. Detailed EFM8SB1 Block Diagram

This section describes the EFM8SB1 family at a high level. For more information on each module including register definitions, see the EFM8SB1 Reference Manual.

### 3.2 Power

All internal circuitry draws power from the VDD supply pin. External I/O pins are powered from the VIO supply voltage (or VDD on devices without a separate VIO connection), while most of the internal circuitry is supplied by an on-chip LDO regulator. Control over the device power can be achieved by enabling/disabling individual peripherals as needed. Each analog peripheral can be disabled when not in use and placed in low power mode. Digital peripherals, such as timers and serial buses, have their clocks gated off and draw little power when they are not in use.

**Table 3.1. Power Modes**

| Power Mode         | Details  | Mode Entry   | Wake-Up Sources  |
|--------------------|--|--|--|
| Normal             | Core and all peripherals clocked and fully operational   | —  | —  |
| Idle               | <ul style="list-style-type: none"> <li>Core halted</li> <li>All peripherals clocked and fully operational</li> <li>Code resumes execution on wake event</li> </ul>   | Set IDLE bit in PCON0  | Any interrupt  |
| Suspend            | <ul style="list-style-type: none"> <li>Core and digital peripherals halted</li> <li>Internal oscillators disabled</li> <li>Code resumes execution on wake event</li> </ul>   | <ol style="list-style-type: none"> <li>Switch SYSCLK to HFOSC0 or LPOSC0</li> <li>Set SUSPEND bit in PMU0CF</li> </ol> | <ul style="list-style-type: none"> <li>RTC0 Alarm Event</li> <li>RTC0 Fail Event</li> <li>CS0 Interrupt</li> <li>Port Match Event</li> <li>Comparator 0 Rising Edge</li> </ul> |
| Stop               | <ul style="list-style-type: none"> <li>All internal power nets shut down</li> <li>Pins retain state</li> <li>Exit on any reset source</li> </ul>   | Set STOP bit in PCON0  | Any reset source   |
| Sleep <sup>1</sup> | <ul style="list-style-type: none"> <li>Most internal power nets shut down</li> <li>Select circuits remain powered</li> <li>Pins retain state</li> <li>All RAM and SFRs retain state</li> <li>Code resumes execution on wake event</li> </ul> | <ol style="list-style-type: none"> <li>Disable unused analog peripherals</li> <li>Set SLEEP bit in PMU0CF</li> </ol>   | <ul style="list-style-type: none"> <li>RTC0 Alarm Event</li> <li>RTC0 Fail Event</li> <li>Port Match Event</li> <li>Comparator 0 Rising Edge</li> </ul>                        |

**Note:**

- Entering Sleep may disconnect the active debug session.

### 3.3 I/O

Digital and analog resources are externally available on the device's multi-purpose I/O pins. Port pins P0.0-P1.7 can be defined as general-purpose I/O (GPIO), assigned to one of the internal digital resources through the crossbar or dedicated channels, or assigned to an analog function. Port pin P2.7 can be used as GPIO. Additionally, the C2 Interface Data signal (C2D) is shared with P2.7.

- Up to 17 multi-functions I/O pins, supporting digital and analog functions.
- Flexible priority crossbar decoder for digital peripheral assignment.
- Two drive strength settings for each pin.
- Two direct-pin interrupt sources with dedicated interrupt vectors (INT0 and INT1).
- Up to 16 direct-pin interrupt sources with shared interrupt vector (Port Match).

### 3.4 Clocking

The CPU core and peripheral subsystem may be clocked by both internal and external oscillator resources. By default, the system clock comes up running from the 20 MHz low power oscillator divided by 8.

- Provides clock to core and peripherals.
- 20 MHz low power oscillator (LPOSC0), accurate to  $\pm 10\%$  over supply and temperature corners.
- 24.5 MHz internal oscillator (HFOSC0), accurate to  $\pm 2\%$  over supply and temperature corners.
- 16.4 kHz low-frequency oscillator (LFOSC0) or external RTC 32 kHz crystal.
- External RC, C, CMOS, and high-frequency crystal clock options (EXTCLK).
- Clock divider with eight settings for flexible clock scaling: Divide the selected clock source by 1, 2, 4, 8, 16, 32, 64, or 128.

### 3.5 Counters/Timers and PWM

#### Real Time Clock (RTC0)

The RTC is an ultra low power, 36 hour 32-bit independent time-keeping Real Time Clock with alarm. The RTC has a dedicated 32 kHz oscillator. No external resistor or loading capacitors are required, and a missing clock detector features alerts the system if the external crystal fails. The on-chip loading capacitors are programmable to 16 discrete levels allowing compatibility with a wide range of crystals.

The RTC module includes the following features:

- Up to 36 hours (32-bit) of independent time keeping.
- Support for internal 16.4 kHz low frequency oscillator (LFOSC0) or external 32 kHz crystal (crystal not available on CSP16 packages).
- Internal crystal loading capacitors with 16 levels.
- Operation in the lowest power mode and across the full supported voltage range.
- Alarm and oscillator failure events to wake from the lowest power mode or reset the device.
- Buffered clock output available for other system devices even in the lowest power mode.

#### Programmable Counter Array (PCA0)

The programmable counter array (PCA) provides multiple channels of enhanced timer and PWM functionality while requiring less CPU intervention than standard counter/timers. The PCA consists of a dedicated 16-bit counter/timer and one 16-bit capture/compare module for each channel. The counter/timer is driven by a programmable timebase that has flexible external and internal clocking options. Each capture/compare module may be configured to operate independently in one of five modes: Edge-Triggered Capture, Software Timer, High-Speed Output, Frequency Output, or Pulse-Width Modulated (PWM) Output. Each capture/compare module has its own associated I/O line (CEXn) which is routed through the crossbar to port I/O when enabled.

- 16-bit time base.
- Programmable clock divisor and clock source selection.
- Up to three independently-configurable channels
- 8, 9, 10, 11 and 16-bit PWM modes (edge-aligned operation).
- Frequency output mode.
- Capture on rising, falling or any edge.
- Compare function for arbitrary waveform generation.
- Software timer (internal compare) mode.
- Integrated watchdog timer.

### Timers (Timer 0, Timer 1, Timer 2, and Timer 3)

Several counter/timers are included in the device: two are 16-bit counter/timers compatible with those found in the standard 8051, and the rest are 16-bit auto-reload timers for timing peripherals or for general purpose use. These timers can be used to measure time intervals, count external events and generate periodic interrupt requests. Timer 0 and Timer 1 are nearly identical and have four primary modes of operation. The other timers offer both 16-bit and split 8-bit timer functionality with auto-reload and capture capabilities.

Timer 0 and Timer 1 include the following features:

- Standard 8051 timers, supporting backwards-compatibility with firmware and hardware.
- Clock sources include SYSCLK, SYSCLK divided by 12, 4, or 48, the External Clock divided by 8, or an external pin.
- 8-bit auto-reload counter/timer mode
- 13-bit counter/timer mode
- 16-bit counter/timer mode
- Dual 8-bit counter/timer mode (Timer 0)

Timer 2 and Timer 3 are 16-bit timers including the following features:

- Clock sources include SYSCLK, SYSCLK divided by 12, or the External Clock divided by 8.
- 16-bit auto-reload timer mode
- Dual 8-bit auto-reload timer mode
- Comparator 0 or RTC0 capture (Timer 2)
- RTC0 or EXTCLK/8 capture (Timer 3)

### Watchdog Timer (WDT0)

The device includes a programmable watchdog timer (WDT) integrated within the PCA0 peripheral. A WDT overflow forces the MCU into the reset state. To prevent the reset, the WDT must be restarted by application software before overflow. If the system experiences a software or hardware malfunction preventing the software from restarting the WDT, the WDT overflows and causes a reset. Following a reset, the WDT is automatically enabled and running with the default maximum time interval. If needed, the WDT can be disabled by system software. The state of the RSTb pin is unaffected by this reset.

The Watchdog Timer integrated in the PCA0 peripheral has the following features:

- Programmable timeout interval
- Runs from the selected PCA clock source
- Automatically enabled after any system reset

## 3.6 Communications and Other Digital Peripherals

### Universal Asynchronous Receiver/Transmitter (UART0)

UART0 is an asynchronous, full duplex serial port offering modes 1 and 3 of the standard 8051 UART. Enhanced baud rate support allows a wide range of clock sources to generate standard baud rates. Received data buffering allows UART0 to start reception of a second incoming data byte before software has finished reading the previous data byte.

The UART module provides the following features:

- Asynchronous transmissions and receptions.
- Baud rates up to  $\text{SYSCLK}/2$  (transmit) or  $\text{SYSCLK}/8$  (receive).
- 8- or 9-bit data.
- Automatic start and stop generation.
- Single-byte FIFO on transmit and receive.

## Serial Peripheral Interface (SPI0)

The serial peripheral interface (SPI) module provides access to a flexible, full-duplex synchronous serial bus. The SPI can operate as a master or slave device in both 3-wire or 4-wire modes, and supports multiple masters and slaves on a single SPI bus. The slave-select (NSS) signal can be configured as an input to select the SPI in slave mode, or to disable master mode operation in a multi-master environment, avoiding contention on the SPI bus when more than one master attempts simultaneous data transfers. NSS can also be configured as a firmware-controlled chip-select output in master mode, or disabled to reduce the number of pins required. Additional general purpose port I/O pins can be used to select multiple slave devices in master mode.

The SPI module includes the following features:

- Supports 3- or 4-wire operation in master or slave modes.
- Supports external clock frequencies up to  $\text{SYSCLK} / 2$  in master mode and  $\text{SYSCLK} / 10$  in slave mode.
- Support for four clock phase and polarity options.
- 8-bit dedicated clock rate generator.
- Support for multiple masters on the same data lines.

## System Management Bus / I2C (SMB0)

The SMBus I/O interface is a two-wire, bi-directional serial bus. The SMBus is compliant with the System Management Bus Specification, version 1.1, and compatible with the I<sup>2</sup>C serial bus.

The SMBus module includes the following features:

- Standard (up to 100 kbps) and Fast (400 kbps) transfer speeds.
- Support for master, slave, and multi-master modes.
- Hardware synchronization and arbitration for multi-master mode.
- Clock low extending (clock stretching) to interface with faster masters.
- Hardware support for 7-bit slave and general call address recognition.
- Firmware support for 10-bit slave address decoding.
- Ability to inhibit all slave states.
- Programmable data setup/hold times.

## 16-bit CRC (CRC0)

The cyclic redundancy check (CRC) module performs a CRC using a 16-bit polynomial. CRC0 accepts a stream of 8-bit data and posts the 16-bit result to an internal register. In addition to using the CRC block for data manipulation, hardware can automatically CRC the flash contents of the device.

The CRC module is designed to provide hardware calculations for flash memory verification and communications protocols. The CRC module supports the standard CCITT-16 16-bit polynomial (0x1021), and includes the following features:

- Support for CCITT-16 polynomial
- Byte-level bit reversal
- Automatic CRC of flash contents on one or more 256-byte blocks
- Initial seed selection of 0x0000 or 0xFFFF



## 3.7 Analog

### Capacitive Sense (CS0)

The Capacitive Sense subsystem uses a capacitance-to-digital circuit to determine the capacitance on a port pin. The module can take measurements from different port pins using the module's analog multiplexer. The module can be configured to take measurements on one port pin, a group of port pins one-by-one using auto-scan, or the total capacitance on multiple channels together. A selectable gain circuit allows the designer to adjust the maximum allowable capacitance. An accumulator is also included, which can be configured to average multiple conversions on an input channel. Interrupts can be generated when the CS0 peripheral completes a conversion or when the measured value crosses a configurable threshold.

The Capacitive Sense module includes the following features:

- Measure multiple pins one-by-one using auto-scan or total capacitance on multiple channels together.
- Configurable input gain.
- Hardware auto-accumulate and average.
- Multiple internal start-of-conversion sources.
- Operational in Suspend when all other clocks are disabled.
- Interrupts available at the end of a conversion or when the measured value crosses a configurable threshold.

### Programmable Current Reference (IREF0)

The programmable current reference (IREF0) module enables current source or sink with two output current settings: Low Power Mode and High Current Mode. The maximum current output in Low Power Mode is 63  $\mu\text{A}$  (1  $\mu\text{A}$  steps) and the maximum current output in High Current Mode is 504  $\mu\text{A}$  (8  $\mu\text{A}$  steps).

The IREF module includes the following features:

- Capable of sourcing or sinking current in programmable steps.
- Two operational modes: Low Power Mode and High Current Mode.
- Fine-tuning mode for higher output precision available in conjunction with the PCA0 module.

### 12-Bit Analog-to-Digital Converter (ADC0)

The ADC is a successive-approximation-register (SAR) ADC with 12-, 10-, and 8-bit modes, integrated track-and hold and a programmable window detector. The ADC is fully configurable under software control via several registers. The ADC may be configured to measure different signals using the analog multiplexer. The voltage reference for the ADC is selectable between internal and external reference sources.

- Up to 10 external inputs.
- Single-ended 12-bit and 10-bit modes.
- Supports an output update rate of 75 ksp/s samples per second in 12-bit mode or 300 ksp/s samples per second in 10-bit mode.
- Operation in low power modes at lower conversion speeds.
- Asynchronous hardware conversion trigger, selectable between software, external I/O and internal timer sources.
- Output data window comparator allows automatic range checking.
- Support for burst mode, which produces one set of accumulated data per conversion-start trigger with programmable power-on settling and tracking time.
- Conversion complete and window compare interrupts supported.
- Flexible output data formatting.
- Includes an internal 1.65 V fast-settling reference and support for external reference.
- Integrated temperature sensor.

## Low Current Comparator (CMP0)

An analog comparator is used to compare the voltage of two analog inputs, with a digital output indicating which input voltage is higher. External input connections to device I/O pins and internal connections are available through separate multiplexers on the positive and negative inputs. Hysteresis, response time, and current consumption may be programmed to suit the specific needs of the application.

The comparator module includes the following features:

- Input options in addition to the pins:
  - Capacitive Sense Comparator output.
  - VDD.
  - VDD divided by 2.
  - Internal connection to LDO output.
  - Direct connection to GND.
- Synchronous and asynchronous outputs can be routed to pins via crossbar.
- Programmable hysteresis between 0 and  $\pm 20$  mV.
- Programmable response time.
- Interrupts generated on rising, falling, or both edges.

## 3.8 Reset Sources

Reset circuitry allows the controller to be easily placed in a predefined default condition. On entry to this reset state, the following occur:

- The core halts program execution.
- Module registers are initialized to their defined reset values unless the bits reset only with a power-on reset.
- External port pins are forced to a known state.
- Interrupts and timers are disabled.

All registers are reset to the predefined values noted in the register descriptions unless the bits only reset with a power-on reset. The contents of RAM are unaffected during a reset; any previously stored data is preserved as long as power is not lost. The Port I/O latches are reset to 1 in open-drain mode. Weak pullups are enabled during and after the reset. For Supply Monitor and power-on resets, the RSTb pin is driven low until the device exits the reset state. On exit from the reset state, the program counter (PC) is reset, and the system clock defaults to an internal oscillator. The Watchdog Timer is enabled, and program execution begins at location 0x0000.

Reset sources on the device include the following:

- Power-on reset
- External reset pin
- Comparator reset
- Software-triggered reset
- Supply monitor reset (monitors VDD supply)
- Watchdog timer reset
- Missing clock detector reset
- Flash error reset
- RTC0 alarm or oscillator failure

## 3.9 Debugging

The EFM8SB1 devices include an on-chip Silicon Labs 2-Wire (C2) debug interface to allow flash programming and in-system debugging with the production part installed in the end application. The C2 interface uses a clock signal (C2CK) and a bi-directional C2 data signal (C2D) to transfer information between the device and a host system. See the C2 Interface Specification for details on the C2 protocol.

### 3.10 Bootloader

All devices come pre-programmed with a UART bootloader. This bootloader resides in the last page of flash and can be erased if it is not needed.

The byte before the Lock Byte is the Bootloader Signature Byte. Setting this byte to a value of 0xA5 indicates the presence of the bootloader in the system. Any other value in this location indicates that the bootloader is not present in flash.

When a bootloader is present, the device will jump to the bootloader vector after any reset, allowing the bootloader to run. The bootloader then determines if the device should stay in bootload mode or jump to the reset vector located at 0x0000. When the bootloader is not present, the device will jump to the reset vector of 0x0000 after any reset.

More information about the bootloader protocol and usage can be found in *AN945: EFM8 Factory Bootloader User Guide*. Application notes can be found on the Silicon Labs website ([www.silabs.com/8bit-appnotes](http://www.silabs.com/8bit-appnotes)) or within Simplicity Studio by using the [Application Notes] tile.

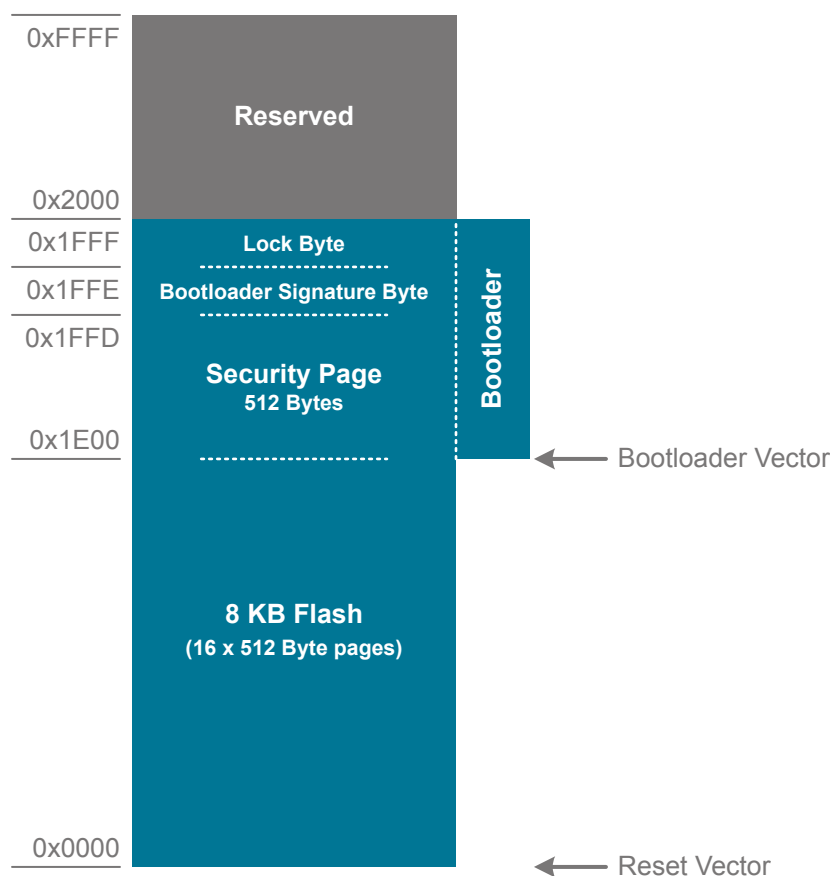


Figure 3.2. Flash Memory Map with Bootloader—8 kB Devices

Table 3.2. Summary of Pins for Bootloader Communication

| Bootloader | Pins for Bootload Communication |
|------------|---------------------------------|
| UART       | TX – P0.4                       |
|            | RX – P0.5                       |

**Table 3.3. Summary of Pins for Bootload Mode Entry**

| Device Package | Pin for Bootload Mode Entry |
|----------------|-----------------------------|
| QFN20          | P2.7 / C2D                  |
| QFN24          | P2.7 / C2D                  |
| QSOP24         | P2.7 / C2D                  |
| CSP16          | P2.7 / C2D                  |

## 4. Electrical Specifications

### 4.1 Electrical Characteristics

All electrical parameters in all tables are specified under the conditions listed in [Table 4.1 Recommended Operating Conditions on page 13](#), unless stated otherwise.

#### 4.1.1 Recommended Operating Conditions

**Table 4.1. Recommended Operating Conditions**

| Parameter  | Symbol              | Test Condition    | Min | Typ | Max | Unit |
|--|---------------------|-------------------|-----|-----|-----|------|
| Operating Supply Voltage on VDD                        | V <sub>DD</sub>     |                   | 1.8 | 2.4 | 3.6 | V    |
| Minimum RAM Data Retention Voltage on VDD <sup>1</sup> | V <sub>RAM</sub>    | Not in Sleep Mode | —   | 1.4 | —   | V    |
|  |                     | Sleep Mode        | —   | 0.3 | 0.5 | V    |
| System Clock Frequency                                 | f <sub>SYSCLK</sub> |                   | 0   | —   | 25  | MHz  |
| Operating Ambient Temperature                          | T <sub>A</sub>      |                   | −40 | —   | 85  | °C   |
| <b>Note:</b><br>1. All voltages with respect to GND.   |                     |                   |     |     |     |      |

## 4.1.2 Power Consumption

**Table 4.2. Power Consumption**

| Parameter   | Symbol              | Conditions   | Min | Typ  | Max | Units  |
|---|---------------------|--|-----|------|-----|--------|
| <b>Digital Supply Current</b>   |                     |  |     |      |     |        |
| Normal Mode supply current - Full speed with code executing from flash <sup>3, 4, 5</sup> | I <sub>DD</sub>     | V <sub>DD</sub> = 1.8–3.6 V, f <sub>SYSClk</sub> = 24.5 MHz          | —   | 3.6  | 4.5 | mA     |
|   |                     | V <sub>DD</sub> = 1.8–3.6 V, f <sub>SYSClk</sub> = 20 MHz            | —   | 3.1  | —   | mA     |
|   |                     | V <sub>DD</sub> = 1.8–3.6 V, f <sub>SYSClk</sub> = 32.768 kHz        | —   | 84   | —   | μA     |
| Normal Mode supply current frequency sensitivity <sup>1, 3, 5</sup>                       | I <sub>DDFREQ</sub> | V <sub>DD</sub> = 1.8–3.6 V, T = 25 °C, f <sub>SYSClk</sub> < 14 MHz | —   | 174  | —   | μA/MHz |
|   |                     | V <sub>DD</sub> = 1.8–3.6 V, T = 25 °C, f <sub>SYSClk</sub> > 14 MHz | —   | 88   | —   | μA/MHz |
| Idle Mode supply current - Core halted with peripherals running <sup>4, 6</sup>           | I <sub>DD</sub>     | V <sub>DD</sub> = 1.8–3.6 V, f <sub>SYSClk</sub> = 24.5 MHz          | —   | 1.8  | 3.0 | mA     |
|   |                     | V <sub>DD</sub> = 1.8–3.6 V, f <sub>SYSClk</sub> = 20 MHz            | —   | 1.4  | —   | mA     |
|   |                     | V <sub>DD</sub> = 1.8–3.6 V, f <sub>SYSClk</sub> = 32.768 kHz        | —   | 82   | —   | μA     |
| Idle Mode Supply Current Frequency Sensitivity <sup>1, 6</sup>                            | I <sub>DDFREQ</sub> | V <sub>DD</sub> = 1.8–3.6 V, T = 25 °C                               | —   | 67   | —   | μA/MHz |
| Suspend Mode Supply Current   | I <sub>DD</sub>     | V <sub>DD</sub> = 1.8–3.6 V  | —   | 77   | —   | μA     |
| Sleep Mode Supply Current with RTC running from 32.768 kHz crystal                        | I <sub>DD</sub>     | 1.8 V, T = 25 °C   | —   | 0.60 | —   | μA     |
|   |                     | 3.6 V, T = 25 °C   | —   | 0.80 | —   | μA     |
|   |                     | 1.8 V, T = 85 °C   | —   | 0.80 | —   | μA     |
|   |                     | 3.6 V, T = 85 °C   | —   | 1.00 | —   | μA     |
| Sleep Mode Supply Current with RTC running from internal LFO                              | I <sub>DD</sub>     | 1.8 V, T = 25 °C   | —   | 0.30 | —   | μA     |
|   |                     | 3.6 V, T = 25 °C   | —   | 0.50 | —   | μA     |
|   |                     | 1.8 V, T = 85 °C   | —   | 0.50 | —   | μA     |
|   |                     | 3.6 V, T = 85 °C   | —   | 0.80 | —   | μA     |
| Sleep Mode Supply Current (RTC off)   | I <sub>DD</sub>     | 1.8 V, T = 25 °C   | —   | 0.05 | —   | μA     |
|   |                     | 3.6 V, T = 25 °C   | —   | 0.08 | —   | μA     |
|   |                     | 1.8 V, T = 85 °C   | —   | 0.20 | —   | μA     |
|   |                     | 3.6 V, T = 85 °C   | —   | 0.28 | —   | μA     |
| V <sub>DD</sub> Monitor Supply Current  | I <sub>VMON</sub>   |  | —   | 7    | —   | μA     |
| Oscillator Supply Current   | I <sub>HFOSC0</sub> | 25 °C  | —   | 300  | —   | μA     |

| Parameter   | Symbol              | Conditions  | Min | Typ | Max | Units |
|---|---------------------|---|-----|-----|-----|-------|
| ADC0 Always-on Power Supply Current <sup>7</sup>                    | I <sub>ADC</sub>    | 300 ksps, 10-bit conversions or<br>75 ksps, 12-bit conversions<br>Normal bias settings<br>V <sub>DD</sub> = 3.0 V     | —   | 740 | —   | μA    |
|   |                     | 150 ksps, 10-bit conversions or<br>37.5 ksps 12-bit conversions<br>Low power bias settings<br>V <sub>DD</sub> = 3.0 V | —   | 400 | —   | μA    |
| Comparator 0 (CMP0) Supply Current                                  | I <sub>CMP</sub>    | CPMD = 11   | —   | 0.4 | —   | μA    |
|   |                     | CPMD = 10   | —   | 2.6 | —   | μA    |
|   |                     | CPMD = 01   | —   | 8.8 | —   | μA    |
|   |                     | CPMD = 00   | —   | 23  | —   | μA    |
| Internal Fast-Settling 1.65V ADC0 Reference, Always-on <sup>8</sup> | I <sub>VREFFS</sub> | Normal Power Mode   | —   | 260 | —   | μA    |
|   |                     | Low Power Mode  | —   | 140 | —   | μA    |
| Temp sensor Supply Current  | I <sub>TSENSE</sub> |   | —   | 35  | —   | μA    |
| Capacitive Sense Module (CS0) Supply Current                        | I <sub>CS0</sub>    | CS module bias current, 25 °C   | —   | 50  | 60  | μA    |
|   |                     | CS module alone, maximum code output, 25 °C   | —   | 90  | 125 | μA    |
|   |                     | Wake-on-CS threshold (suspend mode with regulator and CS module on) <sup>9</sup>                                      | —   | 130 | 180 | μA    |
| Programmable Current Reference (IREF0) Supply Current <sup>10</sup> | I <sub>IREF0</sub>  | Current Source, Either Power Mode, Any Output Code  | —   | 10  | —   | μA    |
|   |                     | Low Power Mode, Current Sink<br>IREF0DAT = 000001   | —   | 1   | —   | μA    |
|   |                     | Low Power Mode, Current Sink<br>IREF0DAT = 111111   | —   | 11  | —   | μA    |
|   |                     | High Current Mode, Current Sink<br>IREF0DAT = 000001  | —   | 12  | —   | μA    |
|   |                     | High Current Mode, Current Sink<br>IREF0DAT = 111111  | —   | 81  | —   | μA    |

| Parameter   | Symbol | Conditions | Min | Typ | Max | Units |
|---|--------|------------|-----|-----|-----|-------|
| <b>Note:</b>  |        |            |     |     |     |       |
| 1. Based on device characterization data; Not production tested.  |        |            |     |     |     |       |
| 2. SYSCLK must be at least 32 kHz to enable debugging.  |        |            |     |     |     |       |
| 3. Digital Supply Current depends upon the particular code being executed. The values in this table are obtained with the CPU executing an “sjmp \$” loop, which is the compiled form of a while(1) loop in C. One iteration requires 3 CPU clock cycles, and the flash memory is read on each cycle. The supply current will vary slightly based on the physical location of the sjmp instruction and the number of flash address lines that toggle as a result. In the worst case, current can increase by up to 30% if the sjmp loop straddles a 64-byte flash address boundary (e.g., 0x007F to 0x0080). Real-world code with larger loops and longer linear sequences will have few transitions across the 64-byte address boundaries. |        |            |     |     |     |       |
| 4. Includes supply current from regulator and oscillator source (24.5 MHz high-frequency oscillator, 20 MHz low-power oscillator, 1 MHz external oscillator, or 32.768 kHz RTC oscillator).   |        |            |     |     |     |       |
| 5. IDD can be estimated for frequencies < 14 MHz by simply multiplying the frequency of interest by the frequency sensitivity number for that range, then adding an offset of 84 μA. When using these numbers to estimate I <sub>DD</sub> for > 14 MHz, the estimate should be the current at 25 MHz minus the difference in current indicated by the frequency sensitivity number. For example: V <sub>DD</sub> = 3.0 V; F = 20 MHz, I <sub>DD</sub> = 3.6 mA – (25 MHz – 20 MHz) x 0.088 mA/MHz = 3.16 mA assuming the same oscillator setting.   |        |            |     |     |     |       |
| 6. Idle IDD can be estimated by taking the current at 25 MHz minus the difference in current indicated by the frequency sensitivity number. For example: V <sub>DD</sub> = 3.0 V; F = 5 MHz, Idle I <sub>DD</sub> = 1.75 mA – (25 MHz – 5 MHz) x 0.067 mA/MHz = 0.41 mA.  |        |            |     |     |     |       |
| 7. ADC0 always-on power excludes internal reference supply current.   |        |            |     |     |     |       |
| 8. The internal reference is enabled as-needed when operating the ADC in burst mode to save power.  |        |            |     |     |     |       |
| 9. Includes only current from regulator, CS module, and MCU in suspend mode.  |        |            |     |     |     |       |
| 10. IREF0 supply current only. Does not include current sourced or sunk from IREF0 output pin.  |        |            |     |     |     |       |

#### 4.1.3 Reset and Supply Monitor

Table 4.3. Reset and Supply Monitor

| Parameter   | Symbol            | Test Condition  | Min  | Typ  | Max  | Unit |
|---|-------------------|---|------|------|------|------|
| VDD Supply Monitor Threshold                                      | V <sub>VDDM</sub> | Reset Trigger   | 1.7  | 1.75 | 1.8  | V    |
|   | V <sub>WARN</sub> | Early Warning   | 1.8  | 1.85 | 1.9  | V    |
| VDD Supply Monitor Turn-On Time                                   | t <sub>MON</sub>  |   | —    | 300  | —    | ns   |
| Power-On Reset (POR) Monitor Threshold                            | V <sub>POR</sub>  | Rising Voltage on V <sub>DD</sub>                       | —    | 1.75 | —    | V    |
|   |                   | Falling Voltage on V <sub>DD</sub>                      | 0.75 | 1.0  | 1.3  | V    |
| V <sub>DD</sub> Ramp Time   | t <sub>RMP</sub>  | Time to V <sub>DD</sub> ≥ 1.8 V                         | —    | —    | 3    | ms   |
| Reset Delay from non-POR source                                   | t <sub>RST</sub>  | Time between release of reset source and code execution | —    | 10   | —    | μs   |
| Reset Delay from POR  | t <sub>POR</sub>  | Relative to V <sub>DD</sub> > V <sub>POR</sub>          | 3    | 10   | 31   | ms   |
| RST Low Time to Generate Reset                                    | t <sub>RSTL</sub> |   | 15   | —    | —    | μs   |
| Missing Clock Detector Response Time (final rising edge to reset) | t <sub>MCD</sub>  | F <sub>SYSCLK</sub> > 1 MHz                             | 100  | 650  | 1000 | μs   |
| Missing Clock Detector Trigger Frequency                          | F <sub>MCD</sub>  |   | —    | 7    | 10   | kHz  |



#### 4.1.4 Flash Memory

**Table 4.4. Flash Memory**

| Parameter                      | Symbol             | Test Condition                          | Min  | Typ   | Max | Units  |
|--------------------------------|--------------------|---|------|-------|-----|--------|
| Write Time <sup>1</sup>        | t <sub>WRITE</sub> | One Byte                                | 57   | 64    | 71  | μs     |
| Erase Time <sup>1</sup>        | t <sub>ERASE</sub> | One Page                                | 28   | 32    | 36  | ms     |
| Endurance (Write/Erase Cycles) | N <sub>WE</sub>    |   | 20 k | 100 k | —   | Cycles |
| CRC Calculation Time           | t <sub>CRC</sub>   | One 256-Byte Block<br>SYSCLK = 24.5 MHz | —    | 21.5  | —   | μs     |

**Note:**

1. Does not include sequencing time before and after the write/erase operation, which may be multiple SYSCLK cycles.
2. Data Retention Information is published in the Quarterly Quality and Reliability Report.

#### 4.1.5 Power Management Timing

**Table 4.5. Power Management Timing**

| Parameter                 | Symbol                       | Test Condition                               | Min | Typ | Max | Units   |
|---------------------------|------------------------------|--|-----|-----|-----|---------|
| Idle Mode Wake-up Time    | t <sub>IDLEWK</sub>          |  | 2   | —   | 3   | SYSCLKs |
| Suspend Mode Wake-up Time | t <sub>SUS-<br/>PENDWK</sub> | CLKDIV = 0x00<br>Low Power or Precision Osc. | —   | 400 | —   | ns      |
| Sleep Mode Wake-up Time   | t <sub>SLEEPWK</sub>         |  | —   | 2   | —   | μs      |

#### 4.1.6 Internal Oscillators

**Table 4.6. Internal Oscillators**

| Parameter  | Symbol              | Test Condition                    | Min  | Typ  | Max  | Unit |
|--|---------------------|-----------------------------------|------|------|------|------|
| <b>High Frequency Oscillator 0 (24.5 MHz)</b>                      |                     |                                   |      |      |      |      |
| Oscillator Frequency   | f <sub>HFOSC0</sub> | Full Temperature and Supply Range | 24   | 24.5 | 25   | MHz  |
| <b>Low Power Oscillator (20 MHz)</b>                               |                     |                                   |      |      |      |      |
| Oscillator Frequency   | f <sub>LPOSC</sub>  | Full Temperature and Supply Range | 18   | 20   | 22   | MHz  |
| <b>Low Frequency Oscillator (16.4 kHz internal RTC oscillator)</b> |                     |                                   |      |      |      |      |
| Oscillator Frequency   | f <sub>LFOSC</sub>  | Full Temperature and Supply Range | 13.1 | 16.4 | 19.7 | kHz  |

#### 4.1.7 Crystal Oscillator

**Table 4.7. Crystal Oscillator**

| Parameter             | Symbol     | Test Condition | Min  | Typ | Max | Unit    |
|-----------------------|------------|----------------|------|-----|-----|---------|
| Crystal Frequency     | $f_{XTAL}$ |                | 0.02 | —   | 25  | MHz     |
| Crystal Drive Current | $I_{XTAL}$ | XFCN = 0       | —    | 0.5 | —   | $\mu$ A |
|                       |            | XFCN = 1       | —    | 1.5 | —   | $\mu$ A |
|                       |            | XFCN = 2       | —    | 4.8 | —   | $\mu$ A |
|                       |            | XFCN = 3       | —    | 14  | —   | $\mu$ A |
|                       |            | XFCN = 4       | —    | 40  | —   | $\mu$ A |
|                       |            | XFCN = 5       | —    | 120 | —   | $\mu$ A |
|                       |            | XFCN = 6       | —    | 550 | —   | $\mu$ A |
|                       |            | XFCN = 7       | —    | 2.6 | —   | mA      |

#### 4.1.8 External Clock Input

**Table 4.8. External Clock Input**

| Parameter   | Symbol      | Test Condition | Min | Typ | Max | Unit |
|---|-------------|----------------|-----|-----|-----|------|
| External Input CMOS Clock Frequency (at EXTCLK pin) | $f_{CMOS}$  |                | 0   | —   | 25  | MHz  |
| External Input CMOS Clock High Time                 | $t_{CMOSH}$ |                | 18  | —   | —   | ns   |
| External Input CMOS Clock Low Time                  | $t_{CMOSL}$ |                | 18  | —   | —   | ns   |

#### 4.1.9 ADC

Table 4.9. ADC

| Parameter  | Symbol                       | Test Condition                                 | Min | Typ   | Max                  | Unit   |
|--|------------------------------|--|-----|-------|----------------------|--------|
| Resolution   | N <sub>bits</sub>            | 12 Bit Mode                                    | 12  |       |                      | Bits   |
|  |                              | 10 Bit Mode                                    | 10  |       |                      | Bits   |
| Throughput Rate  | f <sub>S</sub>               | 12 Bit Mode                                    | —   | —     | 75                   | ksps   |
|  |                              | 10 Bit Mode                                    | —   | —     | 300                  | ksps   |
| Tracking Time  | t <sub>TRK</sub>             | Initial Acquisition                            | 1.5 | —     | —                    | us     |
|  |                              | Subsequent Acquisitions (DC input, burst mode) | 1.1 | —     | —                    | us     |
| Power-On Time  | t <sub>PWR</sub>             |  | 1.5 | —     | —                    | μs     |
| SAR Clock Frequency  | f <sub>SAR</sub>             | High Speed Mode,                               | —   | —     | 8.33                 | MHz    |
|  |                              | Low Power Mode                                 | —   | —     | 4.4                  | MHz    |
| Conversion Time  | T <sub>CNV</sub>             | 10-Bit Conversion                              | 13  | —     | —                    | Clocks |
| Sample/Hold Capacitor  | C <sub>SAR</sub>             | Gain = 1                                       | —   | 16    | —                    | pF     |
|  |                              | Gain = 0.5                                     | —   | 13    | —                    | pF     |
| Input Pin Capacitance  | C <sub>IN</sub>              |  | —   | 20    | —                    | pF     |
| Input Mux Impedance  | R <sub>MUX</sub>             |  | —   | 5     | —                    | kΩ     |
| Voltage Reference Range  | V <sub>REF</sub>             |  | 1   | —     | V <sub>DD</sub>      | V      |
| Input Voltage Range <sup>1</sup>   | V <sub>IN</sub>              | Gain = 1                                       | 0   | —     | V <sub>REF</sub>     | V      |
|  |                              | Gain = 0.5                                     | 0   | —     | 2 x V <sub>REF</sub> | V      |
| Power Supply Rejection Ratio   | PSRR <sub>ADC</sub>          | Internal High Speed VREF                       | —   | 67    | —                    | dB     |
|  |                              | External VREF                                  | —   | 74    | —                    | dB     |
| <b>DC Performance</b>  |                              |  |     |       |                      |        |
| Integral Nonlinearity  | INL                          | 12 Bit Mode                                    | —   | ±1    | ±1.5                 | LSB    |
|  |                              | 10 Bit Mode                                    | —   | ±0.5  | ±1                   | LSB    |
| Differential Nonlinearity (Guaranteed Monotonic)                                       | DNL                          | 12 Bit Mode                                    | —   | ±0.8  | ±1                   | LSB    |
|  |                              | 10 Bit Mode                                    | —   | ±0.5  | ±1                   | LSB    |
| Offset Error   | E <sub>OFF</sub>             | 12 Bit Mode, VREF = 1.65 V                     | -3  | 0     | 3                    | LSB    |
|  |                              | 10 Bit Mode, VREF = 1.65 V                     | -2  | 0     | 2                    | LSB    |
| Offset Temperature Coefficient   | T <sub>C<sub>OFF</sub></sub> |  | —   | 0.004 | —                    | LSB/°C |
| Slope Error  | E <sub>M</sub>               | 12 Bit Mode                                    | —   | ±0.02 | ±0.1                 | %      |
|  |                              | 10 Bit Mode                                    | —   | ±0.06 | ±0.24                | %      |
| <b>Dynamic Performance 10 kHz Sine Wave Input 1dB below full scale, Max throughput</b> |                              |  |     |       |                      |        |
| Signal-to-Noise  | SNR                          | 12 Bit Mode                                    | 62  | 65    | —                    | dB     |
|  |                              | 10 Bit Mode                                    | 54  | 58    | —                    | dB     |

| Parameter                                      | Symbol | Test Condition | Min | Typ | Max | Unit |
|--|--------|----------------|-----|-----|-----|------|
| Signal-to-Noise Plus Distortion                | SNDR   | 12 Bit Mode    | 62  | 65  | —   | dB   |
|  |        | 10 Bit Mode    | 54  | 58  | —   | dB   |
| Total Harmonic Distortion (Up to 5th Harmonic) | THD    | 12 Bit Mode    | —   | -76 | —   | dB   |
|  |        | 10 Bit Mode    | —   | -73 | —   | dB   |
| Spurious-Free Dynamic Range                    | SFDR   | 12 Bit Mode    | —   | 82  | —   | dB   |
|  |        | 10 Bit Mode    | —   | 75  | —   | dB   |

**Note:**

1. Absolute input pin voltage is limited by the  $V_{DD}$  supply.
2. INL and DNL specifications for 12-bit mode do not include the first or last four ADC codes.
3. The maximum code in 12-bit mode is 0xFFFC. The Full Scale Error is referenced from the maximum code.

#### 4.1.10 Voltage Reference

**Table 4.10. Voltage Reference**

| Parameter                               | Symbol          | Test Condition                            | Min  | Typ  | Max      | Unit   |
|---|-----------------|---|------|------|----------|--------|
| <b>Internal Fast Settling Reference</b> |                 |   |      |      |          |        |
| Output Voltage                          | $V_{REFFS}$     |   | 1.62 | 1.65 | 1.68     | V      |
| Temperature Coefficient                 | $TC_{REFFS}$    |   | —    | 50   | —        | ppm/°C |
| Turn-on Time                            | $t_{REFFS}$     |   | —    | —    | 1.5      | μs     |
| Power Supply Rejection                  | $PSRR_{REF FS}$ |   | —    | 400  | —        | ppm/V  |
| <b>External Reference</b>               |                 |   |      |      |          |        |
| Input Voltage                           | $V_{EXTREF}$    |   | 1    | —    | $V_{DD}$ | V      |
| Input Current                           | $I_{EXTREF}$    | Sample Rate = 300 ksps; $V_{REF} = 3.0$ V | —    | 5.25 | —        | μA     |

#### 4.1.11 Temperature Sensor

**Table 4.11. Temperature Sensor**

| Parameter                 | Symbol           | Test Condition        | Min | Typ  | Max | Unit  |
|---------------------------|------------------|-----------------------|-----|------|-----|-------|
| Offset                    | V <sub>OFF</sub> | T <sub>A</sub> = 0 °C | —   | 940  | —   | mV    |
| Offset Error <sup>1</sup> | E <sub>OFF</sub> | T <sub>A</sub> = 0 °C | —   | 18   | —   | mV    |
| Slope                     | M                |                       | —   | 3.40 | —   | mV/°C |
| Slope Error <sup>1</sup>  | E <sub>M</sub>   |                       | —   | 40   | —   | μV/°C |
| Linearity                 |                  |                       | —   | ±1   | —   | °C    |
| Turn-on Time              | t <sub>PWR</sub> |                       | —   | 1.8  | —   | μs    |

**Note:**

1. Represents one standard deviation from the mean.

4.1.12 Comparators

Table 4.12. Comparators

| Parameter                                    | Symbol      | Test Condition       | Min | Typ  | Max | Unit    |
|--|-------------|----------------------|-----|------|-----|---------|
| Response Time, CPMD = 00<br>(Highest Speed)  | $t_{RESP0}$ | +100 mV Differential | —   | 120  | —   | ns      |
|  |             | –100 mV Differential | —   | 110  | —   | ns      |
| Response Time, CPMD = 11 (Low-<br>est Power) | $t_{RESP3}$ | +100 mV Differential | —   | 1.25 | —   | $\mu$ s |
|  |             | –100 mV Differential | —   | 3.2  | —   | $\mu$ s |
| Positive Hysteresis<br>Mode 0 (CPMD = 00)    | $HYS_{CP+}$ | CPHYP = 00           | —   | 0.4  | —   | mV      |
|  |             | CPHYP = 01           | —   | 8    | —   | mV      |
|  |             | CPHYP = 10           | —   | 16   | —   | mV      |
|  |             | CPHYP = 11           | —   | 32   | —   | mV      |
| Negative Hysteresis<br>Mode 0 (CPMD = 00)    | $HYS_{CP-}$ | CPHYN = 00           | —   | -0.4 | —   | mV      |
|  |             | CPHYN = 01           | —   | -8   | —   | mV      |
|  |             | CPHYN = 10           | —   | -16  | —   | mV      |
|  |             | CPHYN = 11           | —   | -32  | —   | mV      |
| Positive Hysteresis<br>Mode 1 (CPMD = 01)    | $HYS_{CP+}$ | CPHYP = 00           | —   | 0.5  | —   | mV      |
|  |             | CPHYP = 01           | —   | 6    | —   | mV      |
|  |             | CPHYP = 10           | —   | 12   | —   | mV      |
|  |             | CPHYP = 11           | —   | 24   | —   | mV      |
| Negative Hysteresis<br>Mode 1 (CPMD = 01)    | $HYS_{CP-}$ | CPHYN = 00           | —   | -0.5 | —   | mV      |
|  |             | CPHYN = 01           | —   | -6   | —   | mV      |
|  |             | CPHYN = 10           | —   | -12  | —   | mV      |
|  |             | CPHYN = 11           | —   | -24  | —   | mV      |
| Positive Hysteresis<br>Mode 2 (CPMD = 10)    | $HYS_{CP+}$ | CPHYP = 00           | —   | 0.7  | —   | mV      |
|  |             | CPHYP = 01           | —   | 4.5  | —   | mV      |
|  |             | CPHYP = 10           | —   | 9    | —   | mV      |
|  |             | CPHYP = 11           | —   | 18   | —   | mV      |
| Negative Hysteresis<br>Mode 2 (CPMD = 10)    | $HYS_{CP-}$ | CPHYN = 00           | —   | -0.6 | —   | mV      |
|  |             | CPHYN = 01           | —   | -4.5 | —   | mV      |
|  |             | CPHYN = 10           | —   | -9   | —   | mV      |
|  |             | CPHYN = 11           | —   | -18  | —   | mV      |
| Positive Hysteresis<br>Mode 3 (CPMD = 11)    | $HYS_{CP+}$ | CPHYP = 00           | —   | 1.5  | —   | mV      |
|  |             | CPHYP = 01           | —   | 4    | —   | mV      |
|  |             | CPHYP = 10           | —   | 8    | —   | mV      |
|  |             | CPHYP = 11           | —   | 16   | —   | mV      |

| Parameter                                 | Symbol             | Test Condition         | Min   | Typ  | Max                   | Unit  |
|---|--------------------|------------------------|-------|------|-----------------------|-------|
| Negative Hysteresis<br>Mode 3 (CPMD = 11) | HYS <sub>CP-</sub> | CPHYN = 00             | —     | -1.5 | —                     | mV    |
|   |                    | CPHYN = 01             | —     | -4   | —                     | mV    |
|   |                    | CPHYN = 10             | —     | -8   | —                     | mV    |
|   |                    | CPHYN = 11             | —     | -16  | —                     | mV    |
| Input Range (CP+ or CP-)                  | V <sub>IN</sub>    |                        | -0.25 | —    | V <sub>DD</sub> +0.25 | V     |
| Input Pin Capacitance                     | C <sub>CP</sub>    |                        | —     | 12   | —                     | pF    |
| Common-Mode Rejection Ratio               | CMRR <sub>CP</sub> |                        | —     | 70   | —                     | dB    |
| Power Supply Rejection Ratio              | PSRR <sub>CP</sub> |                        | —     | 72   | —                     | dB    |
| Input Offset Voltage                      | V <sub>OFF</sub>   | T <sub>A</sub> = 25 °C | -10   | 0    | 10                    | mV    |
| Input Offset Tempco                       | TC <sub>OFF</sub>  |                        | —     | 3.5  | —                     | μV/°C |

#### 4.1.13 Programmable Current Reference (IREF0)

Table 4.13. Programmable Current Reference (IREF0)

| Parameter  | Symbol              | Conditions                    | Min | Typ   | Max                   | Units |
|--|---------------------|-------------------------------|-----|-------|-----------------------|-------|
| <b>Static Performance</b>  |                     |                               |     |       |                       |       |
| Resolution   | N <sub>bits</sub>   |                               | 6   |       |                       | bits  |
| Output Compliance Range  | V <sub>IOUT</sub>   | Low Power Mode, Source        | 0   | —     | V <sub>DD</sub> - 0.4 | V     |
|  |                     | High Current Mode, Source     | 0   | —     | V <sub>DD</sub> - 0.8 | V     |
|  |                     | Low Power Mode, Sink          | 0.3 | —     | V <sub>DD</sub>       | V     |
|  |                     | High Current Mode, Sink       | 0.8 | —     | V <sub>DD</sub>       | V     |
| Integral Nonlinearity  | INL                 |                               | —   | <±0.2 | ±1.0                  | LSB   |
| Differential Nonlinearity  | DNL                 |                               | —   | <±0.2 | ±1.0                  | LSB   |
| Offset Error   | E <sub>OFF</sub>    |                               | —   | <±0.1 | ±0.5                  | LSB   |
| Full Scale Error   | E <sub>FS</sub>     | Low Power Mode, Source        | —   | —     | ±5                    | %     |
|  |                     | High Current Mode, Source     | —   | —     | ±6                    | %     |
|  |                     | Low Power Mode, Sink          | —   | —     | ±8                    | %     |
|  |                     | High Current Mode, Sink       | —   | —     | ±8                    | %     |
| Absolute Current Error   | E <sub>ABS</sub>    | Low Power Mode Sourcing 20 μA | —   | <±1   | ±3                    | %     |
| <b>Dynamic Performance</b>   |                     |                               |     |       |                       |       |
| Output Settling Time to 1/2 LSB  | t <sub>SETTLE</sub> |                               | —   | 300   | —                     | ns    |
| Startup Time   | t <sub>PWR</sub>    |                               | —   | 1     | —                     | μs    |
| <b>Note:</b>   |                     |                               |     |       |                       |       |
| 1. The PCA block may be used to improve IREF0 resolution by PWMing the two LSBs. |                     |                               |     |       |                       |       |

#### 4.1.14 Capacitive Sense (CS0)

**Table 4.14. Capacitive Sense (CS0)**

| Parameter                           | Symbol              | Conditions                          | Min | Typ | Max  | Units    |
|-------------------------------------|---------------------|-------------------------------------|-----|-----|------|----------|
| Single Conversion Time <sup>1</sup> | t <sub>CNV</sub>    | 12-bit Mode                         | 20  | 25  | 40   | μs       |
|                                     |                     | 13-bit Mode (default)               | 21  | 27  | 42.5 | μs       |
|                                     |                     | 14-bit Mode                         | 23  | 29  | 45   | μs       |
|                                     |                     | 16-bit Mode                         | 26  | 33  | 50   | μs       |
| Number of Channels                  | N <sub>CHAN</sub>   | 24-pin Packages                     | 14  |     |      | Channels |
|                                     |                     | 20-pin Packages                     | 13  |     |      | Channels |
|                                     |                     | 16-pin Packages                     | 12  |     |      | Channels |
| Capacitance per Code                | C <sub>LSB</sub>    | Default Configuration, 16-bit codes | —   | 1   | —    | fF       |
| Maximum External Capacitive Load    | C <sub>EXTMAX</sub> | CS0CG = 111b (Default)              | —   | 45  | —    | pF       |
|                                     |                     | CS0CG = 000b                        | —   | 500 | —    | pF       |
| Maximum External Series Impedance   | R <sub>EXTMAX</sub> | CS0CG = 111b (Default)              | —   | 50  | —    | kΩ       |

**Note:**

1. Conversion time is specified with the default configuration.
2. RMS Noise is equivalent to one standard deviation. Peak-to-peak noise encompasses ±3.3 standard deviations. The RMS noise value is specified with the default configuration.



#### 4.1.15 Port I/O

Table 4.15. Port I/O

| Parameter                                     | Symbol          | Test Condition                                   | Min                   | Typ | Max                   | Unit |
|---|-----------------|--|-----------------------|-----|-----------------------|------|
| Output High Voltage (High Drive) <sup>1</sup> | V <sub>OH</sub> | I <sub>OH</sub> = -3 mA                          | V <sub>DD</sub> - 0.7 | —   | —                     | V    |
| Output Low Voltage (High Drive) <sup>1</sup>  | V <sub>OL</sub> | I <sub>OL</sub> = 8.5 mA                         | —                     | —   | 0.6                   | V    |
| Output High Voltage (Low Drive) <sup>1</sup>  | V <sub>OH</sub> | I <sub>OH</sub> = -1 mA                          | V <sub>DD</sub> - 0.7 | —   | —                     | V    |
| Output Low Voltage (Low Drive) <sup>1</sup>   | V <sub>OL</sub> | I <sub>OL</sub> = 1.4 mA                         | —                     | —   | 0.6                   | V    |
| Input High Voltage                            | V <sub>IH</sub> | V <sub>DD</sub> = 2.0 to 3.6 V                   | V <sub>DD</sub> - 0.6 | —   | —                     | V    |
|   |                 | V <sub>DD</sub> = 1.8 to 2.0 V                   | 0.7 x V <sub>DD</sub> | —   | —                     | V    |
| Input Low Voltage                             | V <sub>IL</sub> | V <sub>DD</sub> = 2.0 to 3.6 V                   | —                     | —   | 0.6                   | V    |
|   |                 | V <sub>DD</sub> = 1.8 to 2.0 V                   | —                     | —   | 0.3 x V <sub>DD</sub> | V    |
| Weak Pull-Up Current                          | I <sub>PU</sub> | V <sub>DD</sub> = 1.8 V<br>V <sub>IN</sub> = 0 V | —                     | -4  | —                     | μA   |
|   |                 | V <sub>DD</sub> = 3.6 V<br>V <sub>IN</sub> = 0 V | -35                   | -20 | —                     | μA   |
|   |                 |  |                       |     |                       |      |
| Input Leakage                                 | I <sub>LK</sub> | Weak pullup disabled or pin in analog mode       | -1                    | —   | 1                     | μA   |

**Note:**

1. See [Figure 4.3 Typical V<sub>OH</sub> Curves on page 29](#) and [Figure 4.4 Typical V<sub>OL</sub> Curves on page 30](#) for more information.

4.1.16 SMBus

Table 4.16. SMBus Peripheral Timing Performance (Master Mode)

| Parameter                                       | Symbol        | Test Condition | Min     | Typ | Max     | Unit    |
|---|---------------|----------------|---------|-----|---------|---------|
| <b>Standard Mode (100 kHz Class)</b>            |               |                |         |     |         |         |
| I2C Operating Frequency                         | $f_{I2C}$     |                | 0       | —   | $70^2$  | kHz     |
| SMBus Operating Frequency                       | $f_{SMB}$     |                | $40^1$  | —   | $70^2$  | kHz     |
| Bus Free Time Between STOP and START Conditions | $t_{BUF}$     |                | 9.4     | —   | —       | $\mu s$ |
| Hold Time After (Repeated) START Condition      | $t_{HD:STA}$  |                | 4.7     | —   | —       | $\mu s$ |
| Repeated START Condition Setup Time             | $t_{SU:STA}$  |                | 9.4     | —   | —       | $\mu s$ |
| STOP Condition Setup Time                       | $t_{SU:STO}$  |                | 9.4     | —   | —       | $\mu s$ |
| Data Hold Time                                  | $t_{HD:DAT}$  |                | $489^3$ | —   | —       | ns      |
| Data Setup Time                                 | $t_{SU:DAT}$  |                | $448^3$ | —   | —       | ns      |
| Detect Clock Low Timeout                        | $t_{TIMEOUT}$ |                | 25      | —   | —       | ms      |
| Clock Low Period                                | $t_{LOW}$     |                | 4.7     | —   | —       | $\mu s$ |
| Clock High Period                               | $t_{HIGH}$    |                | 9.4     | —   | $50^4$  | $\mu s$ |
| <b>Fast Mode (400 kHz Class)</b>                |               |                |         |     |         |         |
| I2C Operating Frequency                         | $f_{I2C}$     |                | 0       | —   | $255^2$ | kHz     |
| SMBus Operating Frequency                       | $f_{SMB}$     |                | $40^1$  | —   | $255^2$ | kHz     |
| Bus Free Time Between STOP and START Conditions | $t_{BUF}$     |                | 2.6     | —   | —       | $\mu s$ |
| Hold Time After (Repeated) START Condition      | $t_{HD:STA}$  |                | 1.3     | —   | —       | $\mu s$ |
| Repeated START Condition Setup Time             | $t_{SU:STA}$  |                | 2.6     | —   | —       | $\mu s$ |
| STOP Condition Setup Time                       | $t_{SU:STO}$  |                | 2.6     | —   | —       | $\mu s$ |
| Data Hold Time                                  | $t_{HD:DAT}$  |                | $489^3$ | —   | —       | ns      |
| Data Setup Time                                 | $t_{SU:DAT}$  |                | $448^3$ | —   | —       | ns      |
| Detect Clock Low Timeout                        | $t_{TIMEOUT}$ |                | 25      | —   | —       | ms      |
| Clock Low Period                                | $t_{LOW}$     |                | 1.3     | —   | —       | $\mu s$ |
| Clock High Period                               | $t_{HIGH}$    |                | 2.6     | —   | $50^4$  | $\mu s$ |

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|-----------|--------|----------------|-----|-----|-----|------|
|-----------|--------|----------------|-----|-----|-----|------|

**Note:**

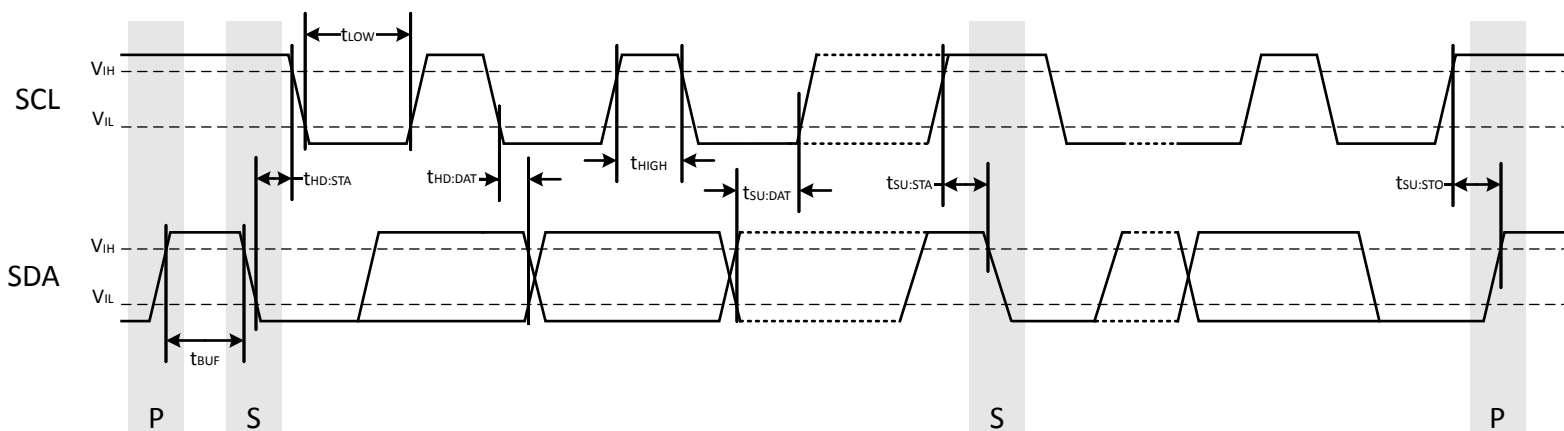
1. The minimum SMBus frequency is limited by the maximum Clock High Period requirement of the SMBus specification.
2. The maximum I2C and SMBus frequencies are limited by the minimum Clock Low Period requirements of their respective specifications. The maximum frequency cannot be achieved with all combinations of oscillators and dividers available, but the effective frequency must not exceed 256 kHz.
3. Data setup and hold timing at 25 MHz or lower with EXTHOLD set to 1.
4. SMBus has a maximum requirement of 50  $\mu$ s for Clock High Period. Operating frequencies lower than 40 kHz will be longer than 50  $\mu$ s. I2C can support periods longer than 50  $\mu$ s.

**Table 4.17. SMBus Peripheral Timing Formulas (Master Mode)**

| Parameter                                       | Symbol       | Clocks        |
|---|--------------|---------------|
| SMBus Operating Frequency                       | $f_{SMB}$    | $f_{CSO} / 3$ |
| Bus Free Time Between STOP and START Conditions | $t_{BUF}$    | $2 / f_{CSO}$ |
| Hold Time After (Repeated) START Condition      | $t_{HD:STA}$ | $1 / f_{CSO}$ |
| Repeated START Condition Setup Time             | $t_{SU:STA}$ | $2 / f_{CSO}$ |
| STOP Condition Setup Time                       | $t_{SU:STO}$ | $2 / f_{CSO}$ |
| Clock Low Period                                | $t_{LOW}$    | $1 / f_{CSO}$ |
| Clock High Period                               | $t_{HIGH}$   | $2 / f_{CSO}$ |

**Note:**

1.  $f_{CSO}$  is the SMBus peripheral clock source overflow frequency.



**Figure 4.1. SMBus Peripheral Timing Diagram (Master Mode)**

## 4.2 Thermal Conditions

**Table 4.18. Thermal Conditions**

| Parameter   | Symbol        | Test Condition   | Min | Typ | Max | Unit |
|---|---------------|------------------|-----|-----|-----|------|
| Thermal Resistance*   | $\theta_{JA}$ | QFN-24 Packages  | —   | 35  | —   | °C/W |
|   |               | QFN-20 Packages  | —   | 60  | —   | °C/W |
|   |               | QSOP-24 Packages | —   | 65  | —   | °C/W |
| <b>Note:</b>  |               |                  |     |     |     |      |
| 1. Thermal resistance assumes a multi-layer PCB with any exposed pad soldered to a PCB pad. |               |                  |     |     |     |      |

## 4.3 Absolute Maximum Ratings

Stresses above those listed in [Table 4.19 Absolute Maximum Ratings on page 28](#) may cause permanent damage to the device. This is a stress rating only and functional operation of the devices at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability. For more information on the available quality and reliability data, see the Quality and Reliability Monitor Report at <http://www.silabs.com/support/quality/pages/default.aspx>.

**Table 4.19. Absolute Maximum Ratings**

| Parameter   | Symbol      | Test Condition | Min     | Max            | Unit |
|---|-------------|----------------|---------|----------------|------|
| Ambient Temperature Under Bias  | $T_{BIAS}$  |                | -55     | 125            | °C   |
| Storage Temperature   | $T_{STG}$   |                | -65     | 150            | °C   |
| Voltage on $V_{DD}$   | $V_{DD}$    |                | GND-0.3 | 4.0            | V    |
| Voltage on I/O pins or RSTb   | $V_{IN}$    |                | GND-0.3 | $V_{DD} + 0.3$ | V    |
| Total Current Sunk into Supply Pin  | $I_{VDD}$   |                | —       | 400            | mA   |
| Total Current Sourced out of Ground Pin   | $I_{GND}$   |                | 400     | —              | mA   |
| Current Sourced or Sunk by Any I/O Pin or RSTb  | $I_{IO}$    |                | -100    | 100            | mA   |
| Maximum Total Current through all Port Pins   | $I_{IOTOT}$ |                | —       | 200            | mA   |
| Operating Junction Temperature  | $T_J$       |                | -40     | 105            | °C   |
| Exposure to maximum rating conditions for extended periods may affect device reliability. |             |                |         |                |      |

#### 4.4 Typical Performance Curves

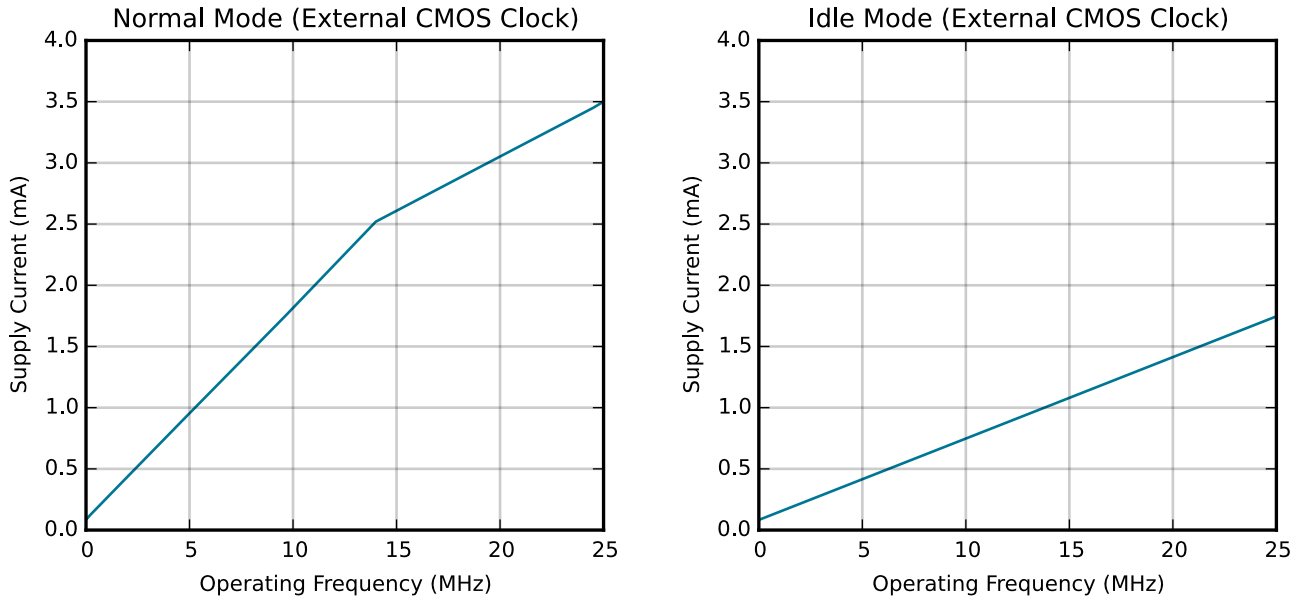


Figure 4.2. Typical Operating Supply Current (full supply voltage range)

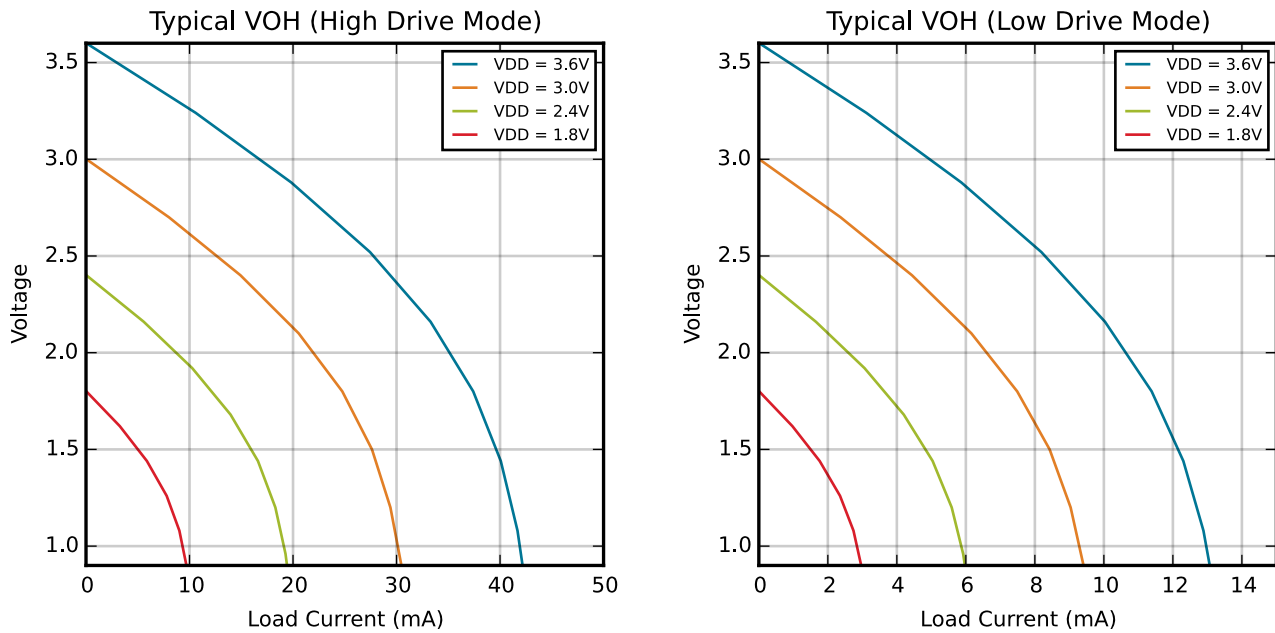


Figure 4.3. Typical  $V_{OH}$  Curves

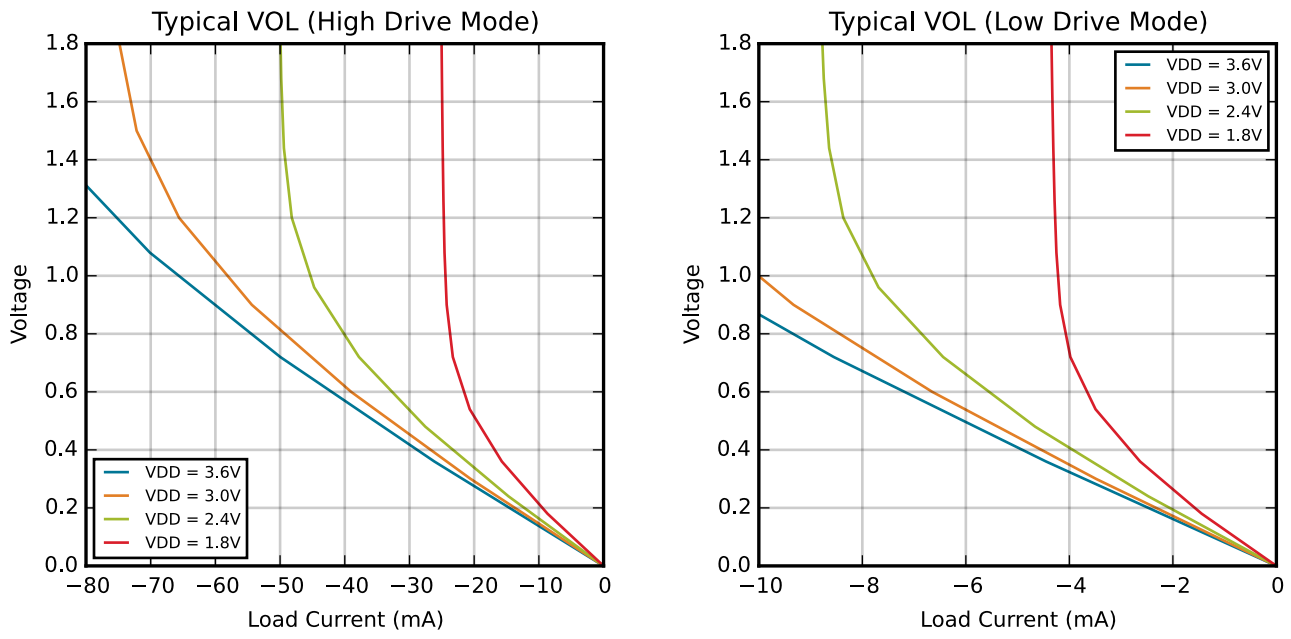


Figure 4.4. Typical  $V_{OL}$  Curves

## 5. Typical Connection Diagrams

### 5.1 Power

Figure 5.1 Power Connection Diagram on page 31 shows a typical connection diagram for the power pins of the EFM8SB1 devices.

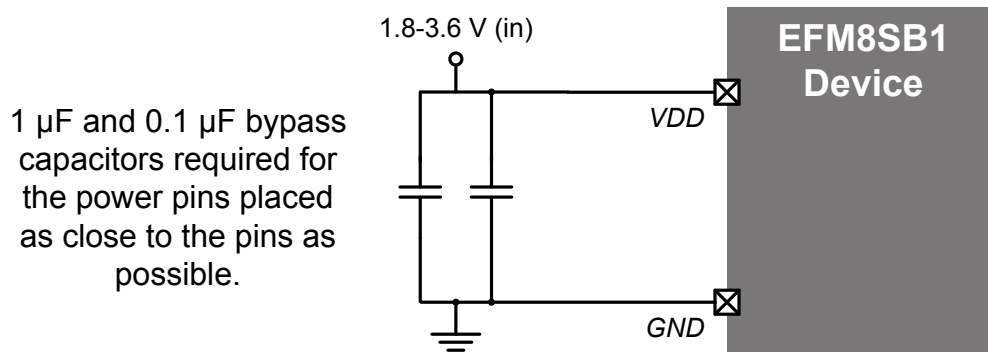


Figure 5.1. Power Connection Diagram

### 5.2 Debug

The diagram below shows a typical connection diagram for the debug connections pins. The pin sharing resistors are only required if the functionality on the C2D (a GPIO pin) and the C2CK (RSTb) is routed to external circuitry. For example, if the RSTb pin is connected to an external switch with debouncing filter or if the GPIO sharing with the C2D pin is connected to an external circuit, the pin sharing resistors and connections to the debug adapter must be placed on the hardware. Otherwise, these components and connections can be omitted.

For more information on debug connections, see the example schematics and information available in AN127: "Pin Sharing Techniques for the C2 Interface." Application notes can be found on the Silicon Labs website (<http://www.silabs.com/8bit-appnotes>) or in Simplicity Studio.

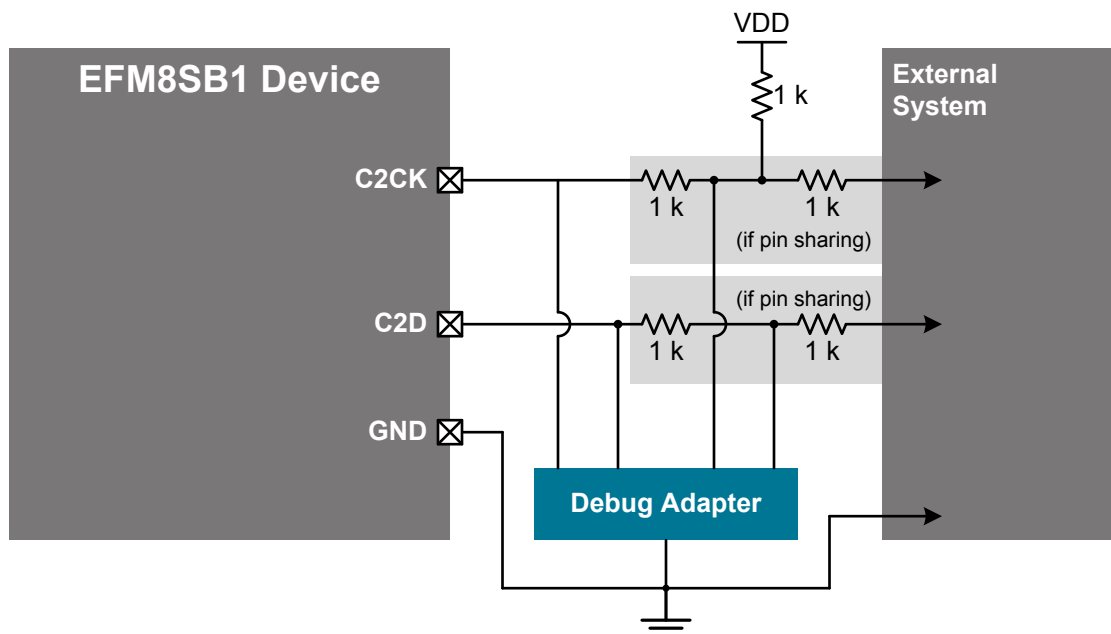


Figure 5.2. Debug Connection Diagram

### 5.3 Other Connections

Other components or connections may be required to meet the system-level requirements. Application note, "AN203: 8-bit MCU Printed Circuit Board Design Notes", contains detailed information on these connections. Application Notes can be accessed on the Silicon Labs website ([www.silabs.com/8bit-appnotes](http://www.silabs.com/8bit-appnotes)).



## 6. Pin Definitions

6.1 EFM8SB1x-QFN20 Pin Definitions

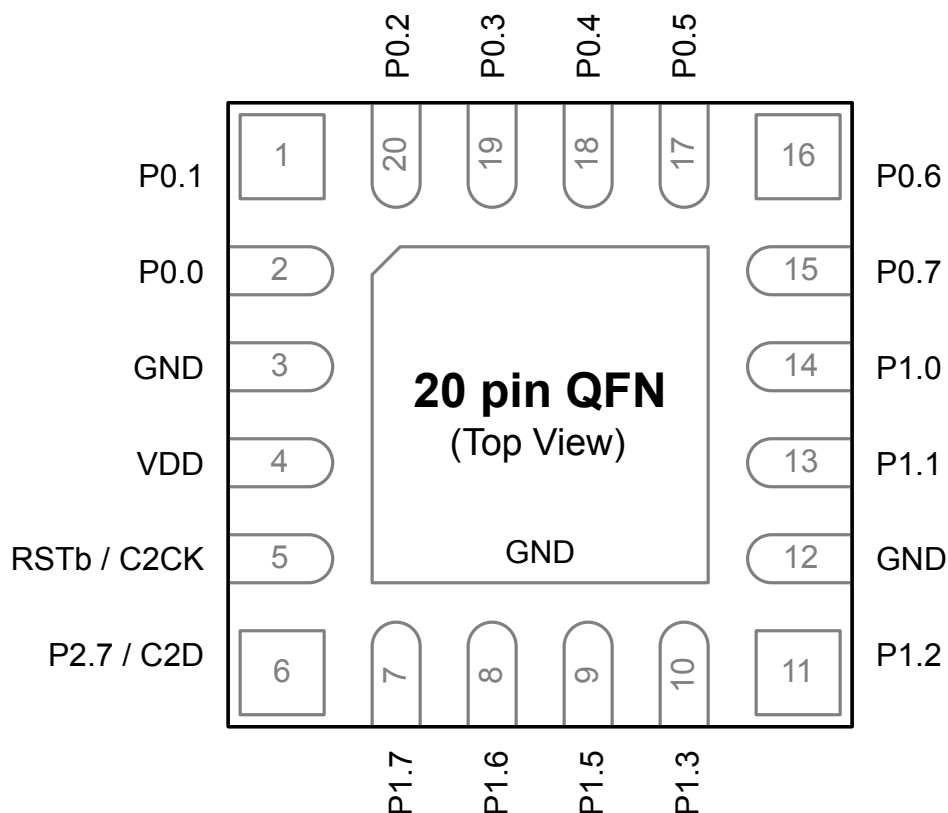


Figure 6.1. EFM8SB1x-QFN20 Pinout

Table 6.1. Pin Definitions for EFM8SB1x-QFN20

| Pin Number | Pin Name | Description        | Crossbar Capability | Additional Digital Functions | Analog Functions        |
|------------|----------|--------------------|---------------------|------------------------------|-------------------------|
| 1          | P0.1     | Multifunction I/O  | Yes                 | P0MAT.1<br>INT0.1<br>INT1.1  | ADC0.1<br>CS0.1<br>AGND |
| 2          | P0.0     | Multifunction I/O  | Yes                 | P0MAT.0<br>INT0.0<br>INT1.0  | CS0.0<br>VREF           |
| 3          | GND      | Ground             |                     |                              |                         |
| 4          | VDD      | Supply Power Input |                     |                              |                         |

| Pin Number | Pin Name       | Description                          | Crossbar Capability | Additional Digital Functions                     | Analog Functions         |
|------------|----------------|--------------------------------------|---------------------|--|--------------------------|
| 5          | RSTb /<br>C2CK | Active-low Reset /<br>C2 Debug Clock |                     |  |                          |
| 6          | P2.7 /<br>C2D  | Multifunction I/O /<br>C2 Debug Data |                     |  |                          |
| 7          | P1.7           | Multifunction I/O                    | Yes                 | P1MAT.7  | XTAL4                    |
| 8          | P1.6           | Multifunction I/O                    | Yes                 | P1MAT.6  | XTAL3                    |
| 9          | P1.5           | Multifunction I/O                    | Yes                 | P1MAT.5  | CS0.13                   |
| 10         | P1.3           | Multifunction I/O                    | Yes                 | P1MAT.3  | ADC0.11<br>CS0.11        |
| 11         | P1.2           | Multifunction I/O                    | Yes                 | P1MAT.2  | ADC0.10<br>CS0.10        |
| 12         | GND            | Ground                               |                     |  |                          |
| 13         | P1.1           | Multifunction I/O                    | Yes                 | P1MAT.1  | CMP0N.4<br>CS0.9         |
| 14         | P1.0           | Multifunction I/O                    | Yes                 | P1MAT.0  | CMP0P.4<br>CS0.8         |
| 15         | P0.7           | Multifunction I/O                    | Yes                 | P0MAT.7<br>INT0.7<br>INT1.7                      | ADC0.7<br>CS0.7<br>IREF0 |
| 16         | P0.6           | Multifunction I/O                    | Yes                 | P0MAT.6<br>CNVSTR<br>INT0.6<br>INT1.6            | ADC0.6<br>CS0.6          |
| 17         | P0.5           | Multifunction I/O                    | Yes                 | P0MAT.5<br>INT0.5<br>INT1.5                      | ADC0.5<br>CS0.5          |
| 18         | P0.4           | Multifunction I/O                    | Yes                 | P0MAT.4<br>INT0.4<br>INT1.4                      | ADC0.4<br>CS0.4          |
| 19         | P0.3           | Multifunction I/O                    | Yes                 | P0MAT.3<br>EXTCLK<br>WAKEOUT<br>INT0.3<br>INT1.3 | ADC0.3<br>CS0.3<br>XTAL2 |

| Pin Number | Pin Name | Description       | Crossbar Capability | Additional Digital Functions          | Analog Functions         |
|------------|----------|-------------------|---------------------|---------------------------------------|--------------------------|
| 20         | P0.2     | Multifunction I/O | Yes                 | P0MAT.2<br>RTCOUT<br>INT0.2<br>INT1.2 | ADC0.2<br>CS0.2<br>XTAL1 |
| Center     | GND      | Ground            |                     |                                       |                          |

6.2 EFM8SB1x-QFN24 Pin Definitions

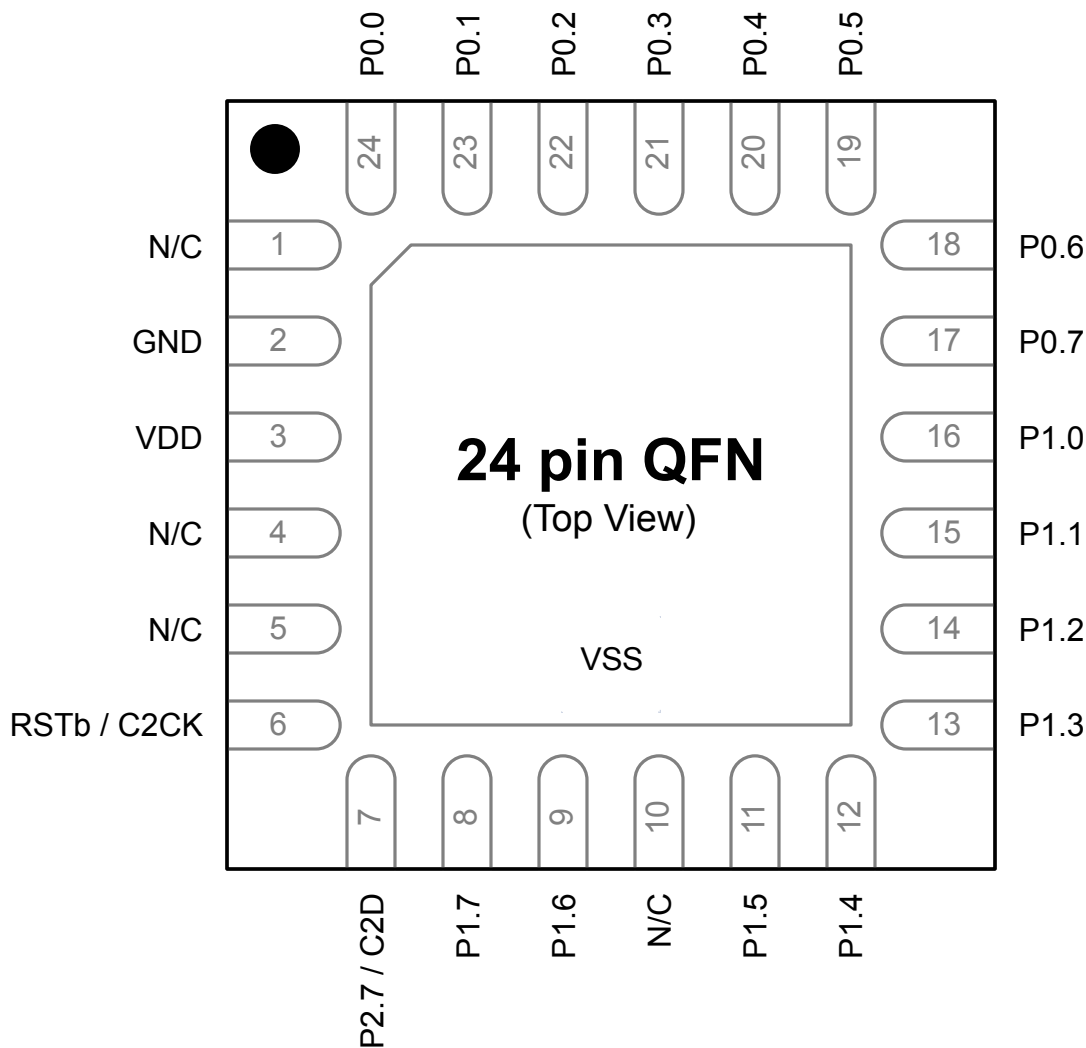


Figure 6.2. EFM8SB1x-QFN24 Pinout

Table 6.2. Pin Definitions for EFM8SB1x-QFN24

| Pin Number | Pin Name | Description        | Crossbar Capability | Additional Digital Functions | Analog Functions |
|------------|----------|--------------------|---------------------|------------------------------|------------------|
| 1          | N/C      | No Connection      |                     |                              |                  |
| 2          | GND      | Ground             |                     |                              |                  |
| 3          | VDD      | Supply Power Input |                     |                              |                  |
| 4          | N/C      | No Connection      |                     |                              |                  |
| 5          | N/C      | No Connection      |                     |                              |                  |

| Pin Number | Pin Name       | Description                          | Crossbar Capability | Additional Digital Functions                     | Analog Functions         |
|------------|----------------|--------------------------------------|---------------------|--|--------------------------|
| 6          | RSTb /<br>C2CK | Active-low Reset /<br>C2 Debug Clock |                     |  |                          |
| 7          | P2.7 /<br>C2D  | Multifunction I/O /<br>C2 Debug Data |                     |  |                          |
| 8          | P1.7           | Multifunction I/O                    | Yes                 | P1MAT.7  | XTAL4                    |
| 9          | P1.6           | Multifunction I/O                    | Yes                 | P1MAT.6  | XTAL3                    |
| 10         | N/C            | No Connection                        |                     |  |                          |
| 11         | P1.5           | Multifunction I/O                    | Yes                 | P1MAT.5  | CS0.13                   |
| 12         | P1.4           | Multifunction I/O                    | Yes                 | P1MAT.4  | ADC0.12<br>CS0.12        |
| 13         | P1.3           | Multifunction I/O                    | Yes                 | P1MAT.3  | ADC0.11<br>CS0.11        |
| 14         | P1.2           | Multifunction I/O                    | Yes                 | P1MAT.2  | ADC0.10<br>CS0.10        |
| 15         | P1.1           | Multifunction I/O                    | Yes                 | P1MAT.1  | CMP0N.4<br>CS0.9         |
| 16         | P1.0           | Multifunction I/O                    | Yes                 | P1MAT.0  | CMP0P.4<br>CS0.8         |
| 17         | P0.7           | Multifunction I/O                    | Yes                 | P0MAT.7<br>INT0.7<br>INT1.7                      | ADC0.7<br>CS0.7<br>IREF0 |
| 18         | P0.6           | Multifunction I/O                    | Yes                 | P0MAT.6<br>CNVSTR<br>INT0.6<br>INT1.6            | ADC0.6<br>CS0.6          |
| 19         | P0.5           | Multifunction I/O                    | Yes                 | P0MAT.5<br>INT0.5<br>INT1.5                      | ADC0.5<br>CS0.5          |
| 20         | P0.4           | Multifunction I/O                    | Yes                 | P0MAT.4<br>INT0.4<br>INT1.4                      | ADC0.4<br>CS0.4          |
| 21         | P0.3           | Multifunction I/O                    | Yes                 | P0MAT.3<br>EXTCLK<br>WAKEOUT<br>INT0.3<br>INT1.3 | ADC0.3<br>CS0.3<br>XTAL2 |

| Pin Number | Pin Name | Description       | Crossbar Capability | Additional Digital Functions          | Analog Functions         |
|------------|----------|-------------------|---------------------|---------------------------------------|--------------------------|
| 22         | P0.2     | Multifunction I/O | Yes                 | P0MAT.2<br>RTCOUT<br>INT0.2<br>INT1.2 | ADC0.2<br>CS0.2<br>XTAL1 |
| 23         | P0.1     | Multifunction I/O | Yes                 | P0MAT.1<br>INT0.1<br>INT1.1           | ADC0.1<br>CS0.1<br>AGND  |
| 24         | P0.0     | Multifunction I/O | Yes                 | P0MAT.0<br>INT0.0<br>INT1.0           | CS0.0<br>VREF            |
| Center     | GND      | Ground            |                     |                                       |                          |

6.3 EFM8SB1x-QSOP24 Pin Definitions

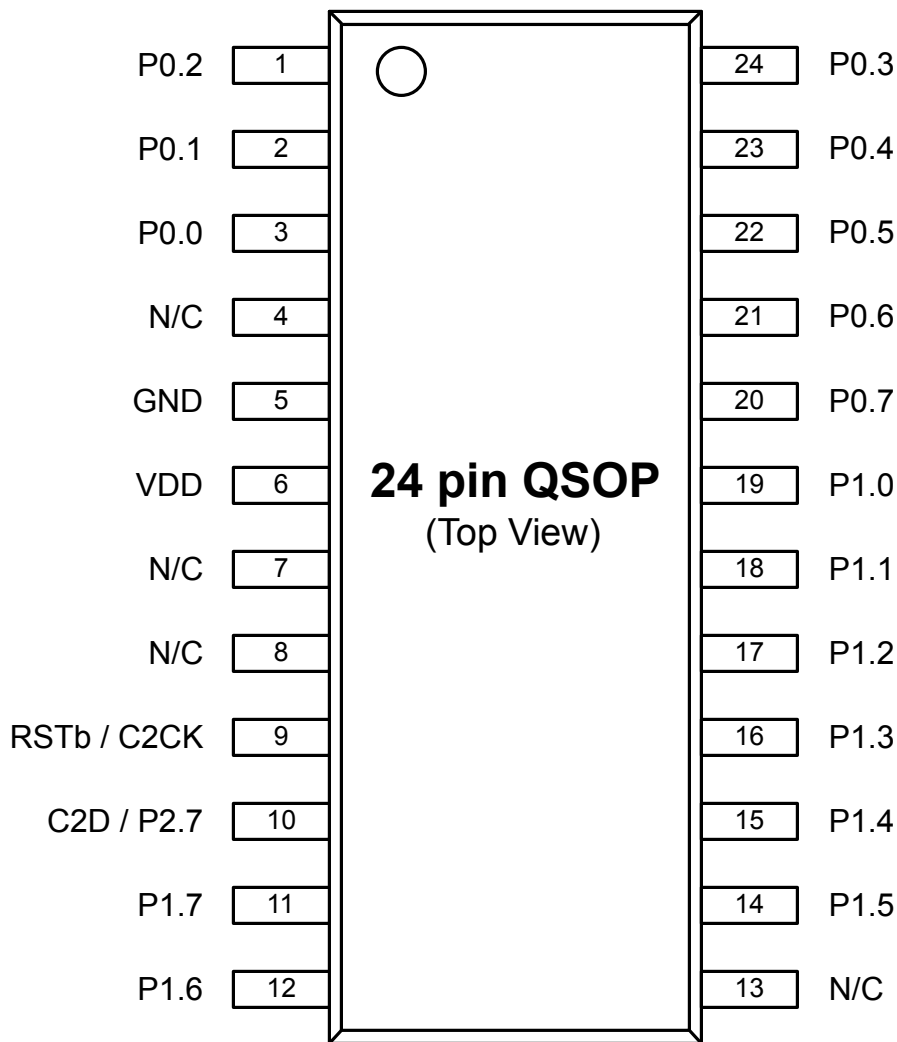


Figure 6.3. EFM8SB1x-QSOP24 Pinout

Table 6.3. Pin Definitions for EFM8SB1x-QSOP24

| Pin Number | Pin Name | Description       | Crossbar Capability | Additional Digital Functions          | Analog Functions         |
|------------|----------|-------------------|---------------------|---------------------------------------|--------------------------|
| 1          | P0.2     | Multifunction I/O | Yes                 | P0MAT.2<br>RTCOUT<br>INT0.2<br>INT1.2 | ADC0.2<br>CS0.2<br>XTAL1 |
| 2          | P0.1     | Multifunction I/O | Yes                 | P0MAT.1<br>INT0.1<br>INT1.1           | ADC0.1<br>CS0.1<br>AGND  |

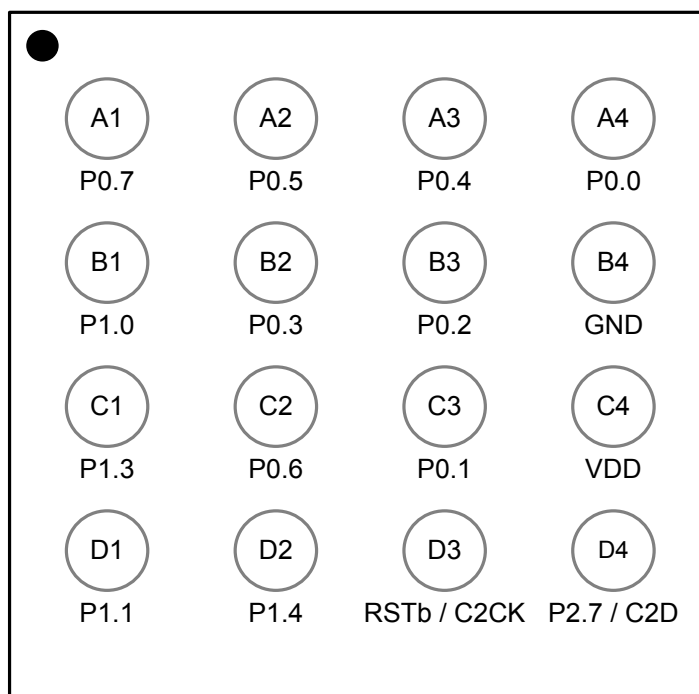


| Pin Number | Pin Name       | Description                          | Crossbar Capability | Additional Digital Functions          | Analog Functions         |
|------------|----------------|--------------------------------------|---------------------|---------------------------------------|--------------------------|
| 3          | P0.0           | Multifunction I/O                    | Yes                 | P0MAT.0<br>INT0.0<br>INT1.0           | CS0.0<br>VREF            |
| 4          | N/C            | No Connection                        |                     |                                       |                          |
| 5          | GND            | Ground                               |                     |                                       |                          |
| 6          | VDD            | Supply Power Input                   |                     |                                       |                          |
| 7          | N/C            | No Connection                        |                     |                                       |                          |
| 8          | N/C            | No Connection                        |                     |                                       |                          |
| 9          | RSTb /<br>C2CK | Active-low Reset /<br>C2 Debug Clock |                     |                                       |                          |
| 10         | P2.7 /<br>C2D  | Multifunction I/O /<br>C2 Debug Data |                     |                                       |                          |
| 11         | P1.7           | Multifunction I/O                    | Yes                 | P1MAT.7                               | XTAL4                    |
| 12         | P1.6           | Multifunction I/O                    | Yes                 | P1MAT.6                               | XTAL3                    |
| 13         | N/C            | No Connection                        |                     |                                       |                          |
| 14         | P1.5           | Multifunction I/O                    | Yes                 | P1MAT.5                               | CS0.13                   |
| 15         | P1.4           | Multifunction I/O                    | Yes                 | P1MAT.4                               | ADC0.12<br>CS0.12        |
| 16         | P1.3           | Multifunction I/O                    | Yes                 | P1MAT.3                               | ADC0.11<br>CS0.11        |
| 17         | P1.2           | Multifunction I/O                    | Yes                 | P1MAT.2                               | ADC0.10<br>CS0.10        |
| 18         | P1.1           | Multifunction I/O                    | Yes                 | P1MAT.1                               | CMP0N.4<br>CS0.9         |
| 19         | P1.0           | Multifunction I/O                    | Yes                 | P1MAT.0                               | CMP0P.4<br>CS0.8         |
| 20         | P0.7           | Multifunction I/O                    | Yes                 | P0MAT.7<br>INT0.7<br>INT1.7           | ADC0.7<br>CS0.7<br>IREF0 |
| 21         | P0.6           | Multifunction I/O                    | Yes                 | P0MAT.6<br>CNVSTR<br>INT0.6<br>INT1.6 | ADC0.6<br>CS0.6          |
| 22         | P0.5           | Multifunction I/O                    | Yes                 | P0MAT.5<br>INT0.5<br>INT1.5           | ADC0.5<br>CS0.5          |

| Pin Number | Pin Name | Description       | Crossbar Capability | Additional Digital Functions                     | Analog Functions         |
|------------|----------|-------------------|---------------------|--|--------------------------|
| 23         | P0.4     | Multifunction I/O | Yes                 | P0MAT.4<br>INT0.4<br>INT1.4                      | ADC0.4<br>CS0.4          |
| 24         | P0.3     | Multifunction I/O | Yes                 | P0MAT.3<br>EXTCLK<br>WAKEOUT<br>INT0.3<br>INT1.3 | ADC0.3<br>CS0.3<br>XTAL2 |

### 6.4 EFM8SB1x-CSP16 Pin Definitions

CSP devices can be handled and soldered using industry standard surface mount assembly techniques. However, because CSP devices are essentially a piece of silicon and are not encapsulated in plastic, they are susceptible to mechanical damage and may be sensitive to light. When CSP packages must be used in an environment exposed to light, it may be necessary to cover the top and sides with an opaque material.



**16 pin CSP**  
(Top View)

Figure 6.4. EFM8SB1x-CSP16 Pinout

Table 6.4. Pin Definitions for EFM8SB1x-CSP16

| Pin Number | Pin Name | Description       | Crossbar Capability | Additional Digital Functions | Analog Functions         |
|------------|----------|-------------------|---------------------|------------------------------|--------------------------|
| A1         | P0.7     | Multifunction I/O | Yes                 | P0MAT.7<br>INT0.7<br>INT1.7  | ADC0.7<br>CS0.7<br>IREF0 |
| A2         | P0.5     | Multifunction I/O | Yes                 | P0MAT.5<br>INT0.5<br>INT1.5  | ADC0.5<br>CS0.5          |
| A3         | P0.4     | Multifunction I/O | Yes                 | P0MAT.4<br>INT0.4<br>INT1.4  | ADC0.4<br>CS0.4          |

| Pin Number | Pin Name       | Description                          | Crossbar Capability | Additional Digital Functions                     | Analog Functions         |
|------------|----------------|--------------------------------------|---------------------|--|--------------------------|
| A4         | P0.0           | Multifunction I/O                    | Yes                 | P0MAT.0<br>INT0.0<br>INT1.0                      | CS0.0<br>VREF            |
| B1         | P1.0           | Multifunction I/O                    | Yes                 | P1MAT.0  | CMP0P.4<br>CS0.8         |
| B2         | P0.3           | Multifunction I/O                    | Yes                 | P0MAT.3<br>EXTCLK<br>WAKEOUT<br>INT0.3<br>INT1.3 | ADC0.3<br>CS0.3<br>XTAL2 |
| B3         | P0.2           | Multifunction I/O                    | Yes                 | P0MAT.2<br>RTCOU<br>INT0.2<br>INT1.2             | ADC0.2<br>CS0.2<br>XTAL1 |
| B4         | GND            | Ground                               |                     |  |                          |
| C1         | P1.3           | Multifunction I/O                    | Yes                 | P1MAT.3  | ADC0.11<br>CS0.11        |
| C2         | P0.6           | Multifunction I/O                    | Yes                 | P0MAT.6<br>CNVSTR<br>INT0.6<br>INT1.6            | ADC0.6<br>CS0.6          |
| C3         | P0.1           | Multifunction I/O                    | Yes                 | P0MAT.1<br>INT0.1<br>INT1.1                      | ADC0.1<br>CS0.1<br>AGND  |
| C4         | VDD            | Supply Power Input                   |                     |  |                          |
| D1         | P1.1           | Multifunction I/O                    | Yes                 | P1MAT.1  | CMP0N.4<br>CS0.9         |
| D2         | P1.4           | Multifunction I/O                    | Yes                 | P1MAT.4  | ADC0.12<br>CS0.12        |
| D3         | RSTb /<br>C2CK | Active-low Reset /<br>C2 Debug Clock |                     |  |                          |
| D4         | P2.7 /<br>C2D  | Multifunction I/O /<br>C2 Debug Data |                     |  |                          |

## 7. CSP16 Package Specifications

### 7.1 CSP16 Package Dimensions

**Note:** CSP devices can be handled and soldered using industry standard surface mount assembly techniques. However, because CSP devices are essentially a piece of silicon and are not encapsulated in plastic, they are susceptible to mechanical damage and may be sensitive to light. When CSP packages must be used in an environment exposed to light, it may be necessary to cover the top and sides with an opaque material.

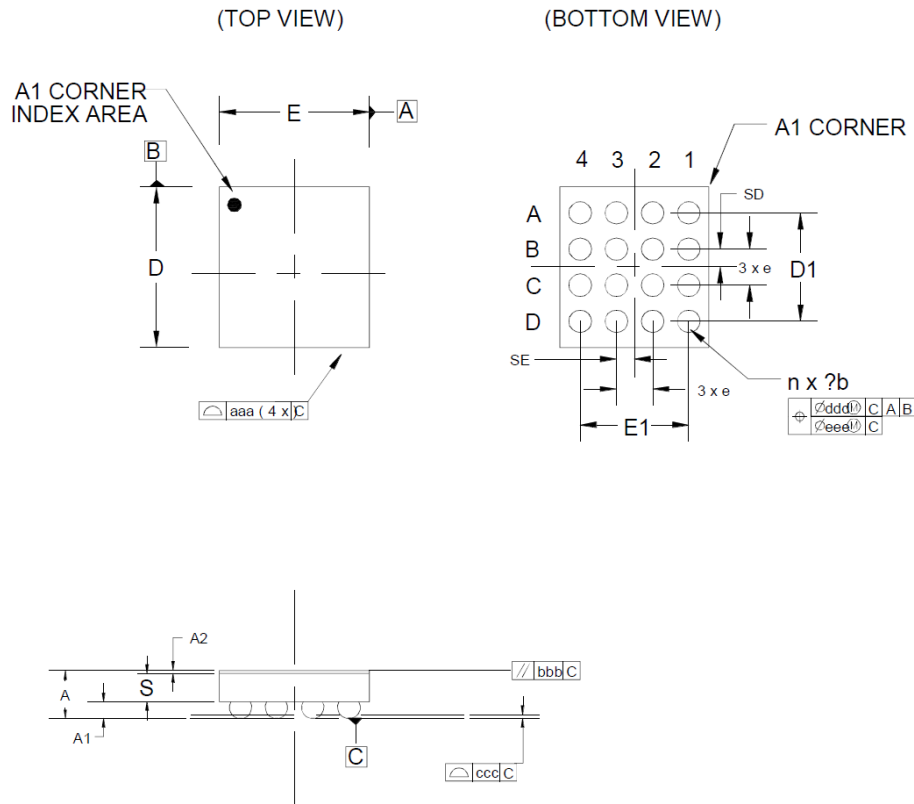


Figure 7.1. CSP16 Package Drawing

Table 7.1. CSP16 Package Dimensions

| Dimension | Min       | Typ   | Max    |
|-----------|-----------|-------|--------|
| A         | 0.491     | 0.55  | 0.609  |
| A1        | 0.17      | —     | 0.23   |
| A2        | 0.036     | 0.040 | 0.044  |
| b         | 0.23      | —     | 0.29   |
| S         | 0.3075    | 0.31  | 0.3125 |
| D         | 1.781 BSC |       |        |
| E         | 1.659 BSC |       |        |
| e         | 0.40 BSC  |       |        |
| D1        | 1.20 BSC  |       |        |

| Dimension | Min | Typ      | Max |
|-----------|-----|----------|-----|
| E1        |     | 1.20 BSC |     |
| SD        |     | 0.2      |     |
| SE        |     | 0.2      |     |
| n         |     | 16       |     |
| aaa       |     | 0.03     |     |
| bbb       |     | 0.06     |     |
| ccc       |     | 0.05     |     |
| ddd       |     | 0.015    |     |

**Note:**

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. Primary datum "C" and seating plane are defined by the spherical crowns of the solder balls.
4. Dimension "b" is measured at the maximum solder bump diameter, parallel to primary datum "C".
5. Recommended card reflow profile is per the JEDEC/IPC J-STD-020C specification for Small Body Components.

7.2 CSP16 PCB Land Pattern

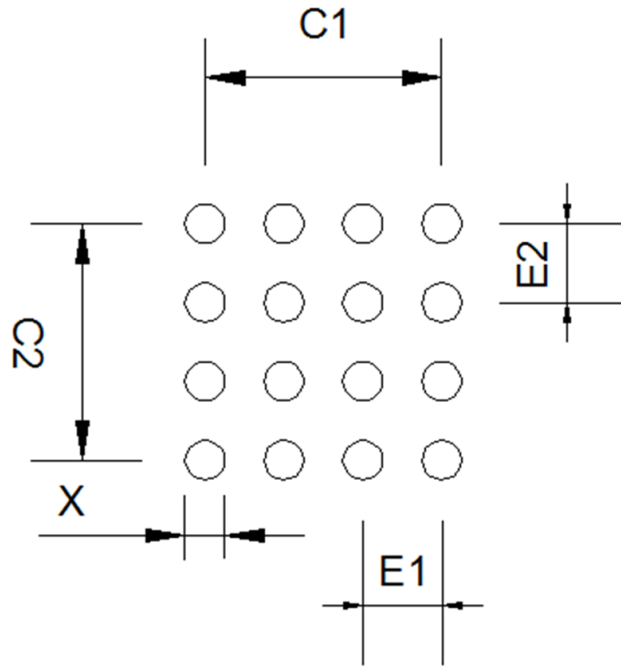


Figure 7.2. CSP16 PCB Land Pattern Drawing

Table 7.2. CSP16 PCB Land Pattern Dimensions

| Dimension | Min | Max  |
|-----------|-----|------|
| X         |     | 0.20 |
| C1        |     | 1.20 |
| C2        |     | 1.20 |
| E1        |     | 0.40 |
| E2        |     | 0.40 |

**Note:**

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing is per the ANSI Y14.5M-1994 specification.
3. This Land Pattern Design is based on the IPC-7351 guidelines.
4. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60  $\mu\text{m}$  minimum, all the way around the pad.
5. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
6. The stencil thickness should be 0.075 mm (3 mils).
7. A stencil of square aperture (0.22 x 0.22 mm) is recommended.
8. A No-Clean, Type-3 solder paste is recommended.
9. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

### 7.3 CSP16 Package Marking

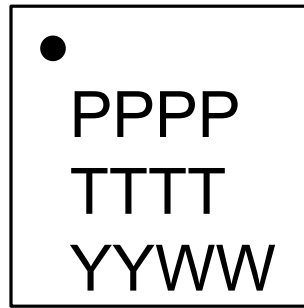


Figure 7.3. CSP16 Package Marking

The package marking consists of:

- PPPP – The part number designation.
- TTTT – A trace or manufacturing code.
- YY – The last 2 digits of the assembly year.
- WW – The 2-digit workweek when the device was assembled.



## 8. QFN20G Package Specifications

**Note:** This section includes packaging information for G-grade devices.

### 8.1 QFN20 Package Dimensions

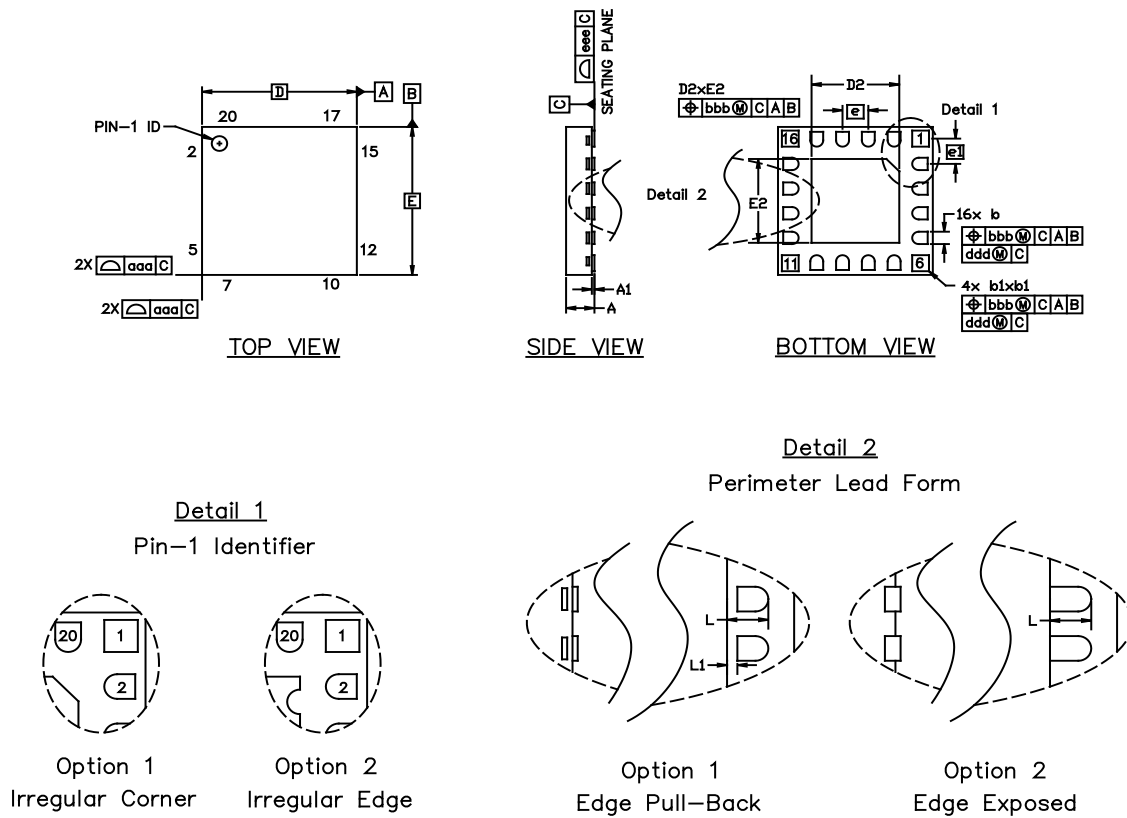


Figure 8.1. QFN20 Package Drawing

Table 8.1. QFN20 Package Dimensions

| Dimension | Min       | Typ   | Max   |
|-----------|-----------|-------|-------|
| A         | 0.50      | 0.55  | 0.60  |
| A1        | 0.00      | —     | 0.05  |
| b         | 0.20      | 0.25  | 0.30  |
| b1        | 0.275     | 0.325 | 0.375 |
| D         | 3.00 BSC  |       |       |
| D2        | 1.6       | 1.70  | 1.80  |
| e         | 0.50 BSC  |       |       |
| e1        | 0.513 BSC |       |       |
| E         | 3.00 BSC  |       |       |
| E2        | 1.60      | 1.70  | 1.80  |
| L         | 0.35      | 0.40  | 0.45  |
| L1        | 0.00      | —     | 0.10  |
| aaa       | —         | 0.10  | —     |

| Dimension | Min | Typ  | Max  |
|-----------|-----|------|------|
| bbb       | —   | 0.10 | —    |
| ddd       | —   | 0.05 | —    |
| eee       | —   | —    | 0.08 |

**Note:**

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing is based upon JEDEC Solid State Product Outline MO-248 but includes custom features which are toleranced per supplier designation.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

8.2 QFN20 PCB Land Pattern

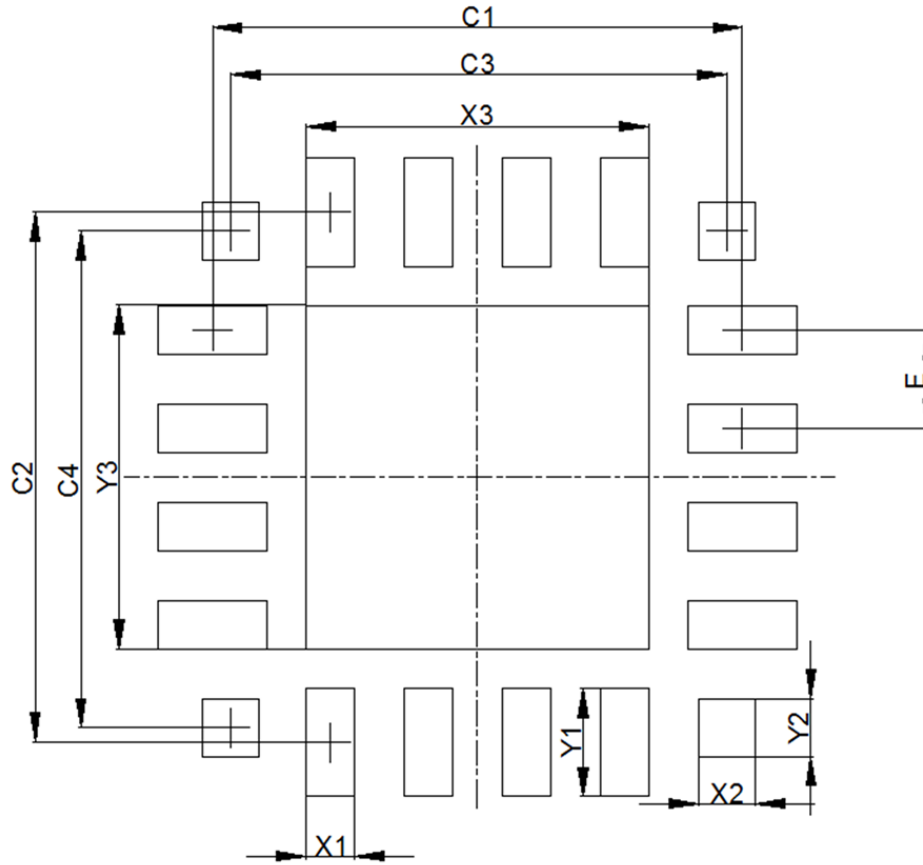


Figure 8.2. QFN20 PCB Land Pattern Drawing

Table 8.2. QFN20 PCB Land Pattern Dimensions

| Dimension | Min  | Max      |
|-----------|------|----------|
| C1        |      | 2.70     |
| C2        |      | 2.70     |
| C3        |      | 2.53     |
| C4        |      | 2.53     |
| E         |      | 0.50 REF |
| X1        | 0.20 | 0.30     |
| X2        | 0.24 | 0.34     |
| X3        | 1.70 | 1.80     |
| Y1        | 0.50 | 0.60     |
| Y2        | 0.24 | 0.34     |
| Y3        | 1.70 | 1.80     |

| Dimension  | Min | Max |
|--|-----|-----|
| <p><b>Note:</b></p> <ol style="list-style-type: none"> <li>1. All dimensions shown are in millimeters (mm) unless otherwise noted.</li> <li>2. Dimensioning and Tolerancing is per the ANSI Y14.5M-1994 specification.</li> <li>3. This Land Pattern Design is based on the IPC-7351 guidelines.</li> <li>4. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.</li> <li>5. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.</li> <li>6. The stencil thickness should be 0.125 mm (5 mils).</li> <li>7. The ratio of stencil aperture to land pad size should be 1:1 for the perimeter pads.</li> <li>8. A 2x2 array of 0.75 mm openings on a 0.95 mm pitch should be used for the center pad to assure proper paste volume.</li> <li>9. A No-Clean, Type-3 solder paste is recommended.</li> <li>10. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.</li> </ol> |     |     |

### 8.3 QFN20 Package Marking

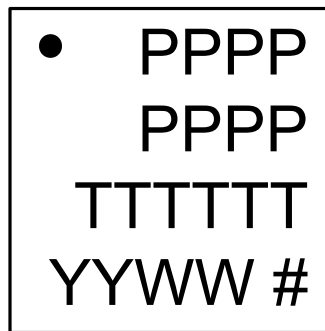


Figure 8.3. QFN20 Package Marking

The package marking consists of:

- P P P P P P P P – The part number designation.
- T T T T T T – A trace or manufacturing code.
- Y Y – The last 2 digits of the assembly year.
- W W – The 2-digit workweek when the device was assembled.
- # – The device revision (A, B, etc.).

## 9. QFN20A Package Specifications

**Note:** This section includes packaging information for A-grade devices.

9.1 QFN20 Package Dimensions

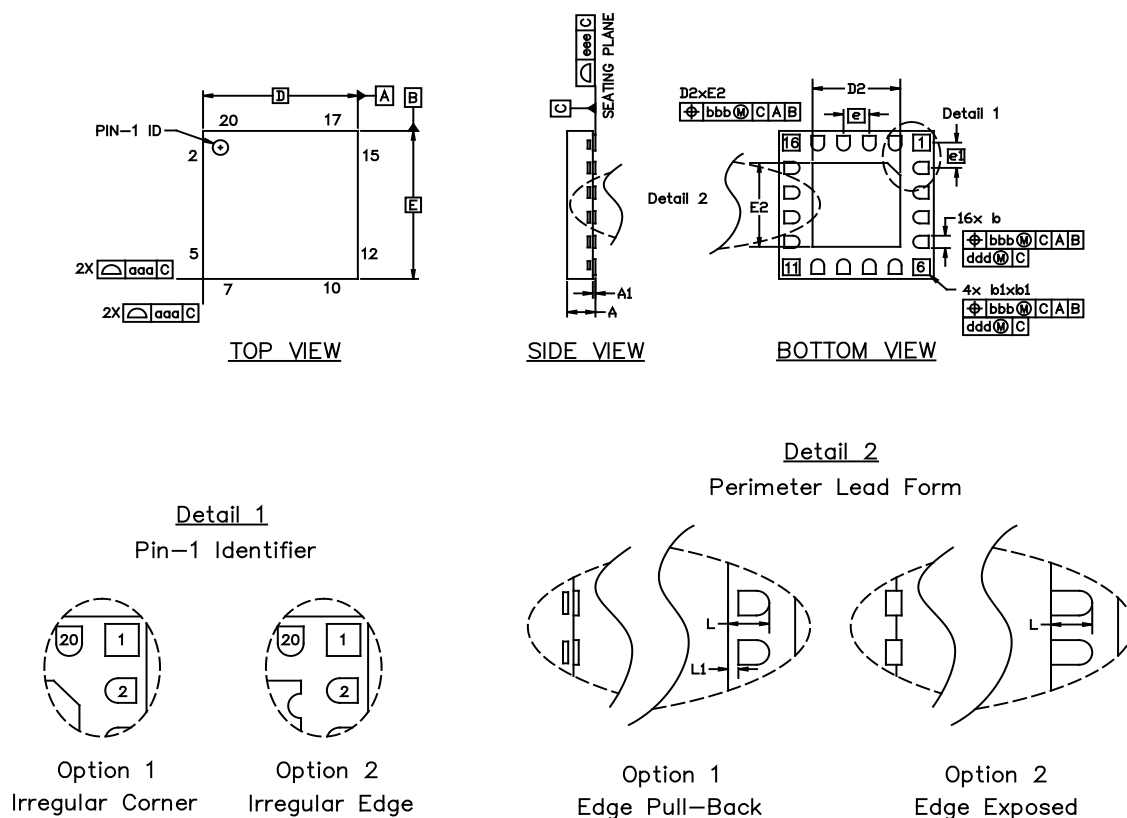


Figure 9.1. QFN20 Package Drawing

Table 9.1. QFN20 Package Dimensions

| Dimension | Min       | Typ   | Max  |
|-----------|-----------|-------|------|
| A         | 0.70      | 0.75  | 0.80 |
| A1        | 0.00      | 0.035 | 0.05 |
| b         | 0.20      | 0.25  | 0.30 |
| b1        | 0.25      | 0.30  | 0.35 |
| D         | 3.00 BSC  |       |      |
| D2        | 1.60      | 1.70  | 1.80 |
| e         | 0.50 BSC  |       |      |
| e1        | 0.513 BSC |       |      |
| E         | 3.00 BSC  |       |      |
| E2        | 1.60      | 1.70  | 1.80 |
| L         | 0.35      | 0.40  | 0.45 |
| L1        | 0.00      | —     | 0.10 |
| aaa       | —         | 0.10  | —    |

| Dimension | Min | Typ  | Max  |
|-----------|-----|------|------|
| bbb       | —   | 0.10 | —    |
| ddd       | —   | 0.05 | —    |
| eee       | —   | —    | 0.08 |

**Note:**

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing is based upon JEDEC Solid State Product Outline MO-248 but includes custom features which are toleranced per supplier designation.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.



9.2 QFN20 PCB Land Pattern

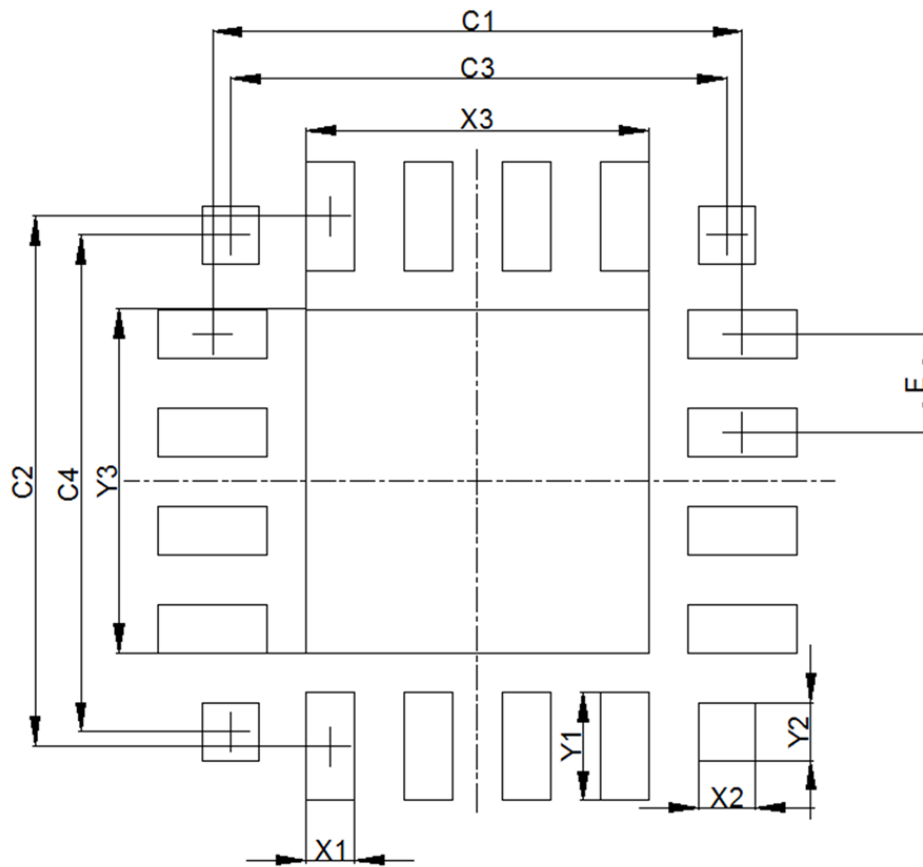


Figure 9.2. QFN20 PCB Land Pattern Drawing

Table 9.2. QFN20 PCB Land Pattern Dimensions

| Dimension | Min  | Max      |
|-----------|------|----------|
| C1        |      | 2.70     |
| C2        |      | 2.70     |
| C3        |      | 2.53     |
| C4        |      | 2.53     |
| E         |      | 0.50 REF |
| X1        | 0.20 | 0.30     |
| X2        | 0.24 | 0.34     |
| X3        | 1.70 | 1.80     |
| Y1        | 0.50 | 0.60     |
| Y2        | 0.24 | 0.34     |
| Y3        | 1.70 | 1.80     |

| Dimension  | Min | Max |
|--|-----|-----|
| <p><b>Note:</b></p> <ol style="list-style-type: none"> <li>1. All dimensions shown are in millimeters (mm) unless otherwise noted.</li> <li>2. Dimensioning and Tolerancing is per the ANSI Y14.5M-1994 specification.</li> <li>3. This Land Pattern Design is based on the IPC-7351 guidelines.</li> <li>4. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.</li> <li>5. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.</li> <li>6. The stencil thickness should be 0.125 mm (5 mils).</li> <li>7. The ratio of stencil aperture to land pad size should be 1:1 for the perimeter pads.</li> <li>8. A 2x2 array of 0.75 mm openings on a 0.95 mm pitch should be used for the center pad to assure proper paste volume.</li> <li>9. A No-Clean, Type-3 solder paste is recommended.</li> <li>10. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.</li> </ol> |     |     |

### 9.3 QFN20 Package Marking

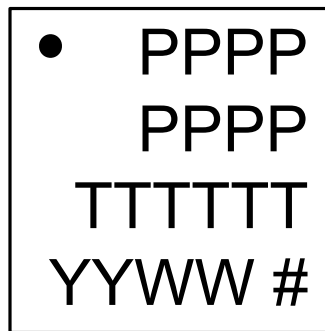


Figure 9.3. QFN20 Package Marking

The package marking consists of:

- P P P P P P P P – The part number designation.
- T T T T T T – A trace or manufacturing code.
- Y Y – The last 2 digits of the assembly year.
- W W – The 2-digit workweek when the device was assembled.
- # – The device revision (A, B, etc.).

## 10. QFN24 Package Specifications

### 10.1 QFN24 Package Dimensions

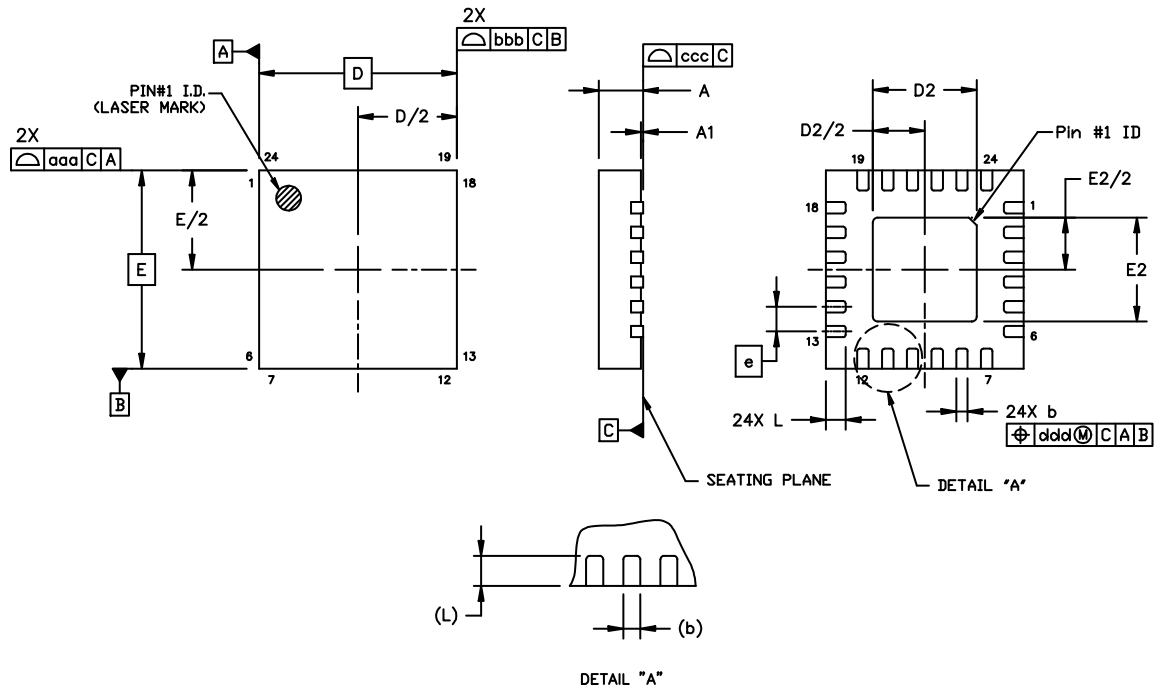


Figure 10.1. QFN24 Package Drawing

Table 10.1. QFN24 Package Dimensions

| Dimension | Min      | Typ  | Max  |
|-----------|----------|------|------|
| A         | 0.70     | 0.75 | 0.80 |
| A1        | 0.00     | —    | 0.05 |
| b         | 0.18     | 0.25 | 0.30 |
| D         | 4.00 BSC |      |      |
| D2        | 2.35     | 2.45 | 2.55 |
| e         | 0.50 BSC |      |      |
| E         | 4.00 BSC |      |      |
| E2        | 2.35     | 2.45 | 2.55 |
| L         | 0.30     | 0.40 | 0.50 |
| aaa       | —        | —    | 0.10 |
| bbb       | —        | —    | 0.10 |
| ccc       | —        | —    | 0.08 |
| ddd       | —        | —    | 0.10 |

| Dimension   | Min | Typ | Max |
|---|-----|-----|-----|
| <p><b>Note:</b></p> <ol style="list-style-type: none"><li>1. All dimensions shown are in millimeters (mm) unless otherwise noted.</li><li>2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.</li><li>3. This drawing conforms to JEDEC Solid State Outline MO-220.</li><li>4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020C specification for Small Body Components.</li></ol> |     |     |     |

10.2 QFN24 PCB Land Pattern

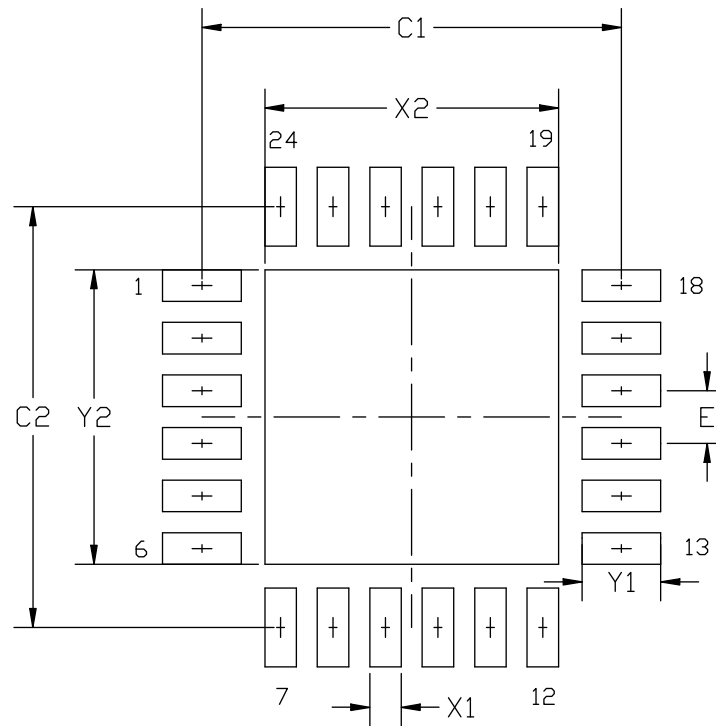


Figure 10.2. QFN24 PCB Land Pattern Drawing

Table 10.2. QFN24 PCB Land Pattern Dimensions

| Dimension | Min      | Max  |
|-----------|----------|------|
| C1        | 3.90     | 4.00 |
| C2        | 3.90     | 4.00 |
| E         | 0.50 BSC |      |
| X1        | 0.20     | 0.30 |
| X2        | 2.70     | 2.80 |
| Y1        | 0.65     | 0.75 |
| Y2        | 2.70     | 2.80 |

| Dimension  | Min | Max |
|--|-----|-----|
| <p><b>Note:</b></p> <ol style="list-style-type: none"> <li>1. All dimensions shown are in millimeters (mm) unless otherwise noted.</li> <li>2. This Land Pattern Design is based on the IPC-7351 guidelines.</li> <li>3. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 μm minimum, all the way around the pad.</li> <li>4. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.</li> <li>5. The stencil thickness should be 0.125 mm (5 mils).</li> <li>6. The ratio of stencil aperture to land pad size should be 1:1 for all perimeter pads.</li> <li>7. A 2 x 2 array of 1.10 mm x 1.10 mm openings on 1.30 mm pitch should be used for the center ground pad.</li> <li>8. A No-Clean, Type-3 solder paste is recommended.</li> <li>9. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.</li> </ol> |     |     |

### 10.3 QFN24 Package Marking



Figure 10.3. QFN24 Package Marking

The package marking consists of:

- P P P P P P P P – The part number designation.
- T T T T T T – A trace or manufacturing code.
- Y Y – The last 2 digits of the assembly year.
- W W – The 2-digit workweek when the device was assembled.
- # – The device revision (A, B, etc.).

## 11. QSOP24 Package Specifications

### 11.1 QSOP24 Package Dimensions

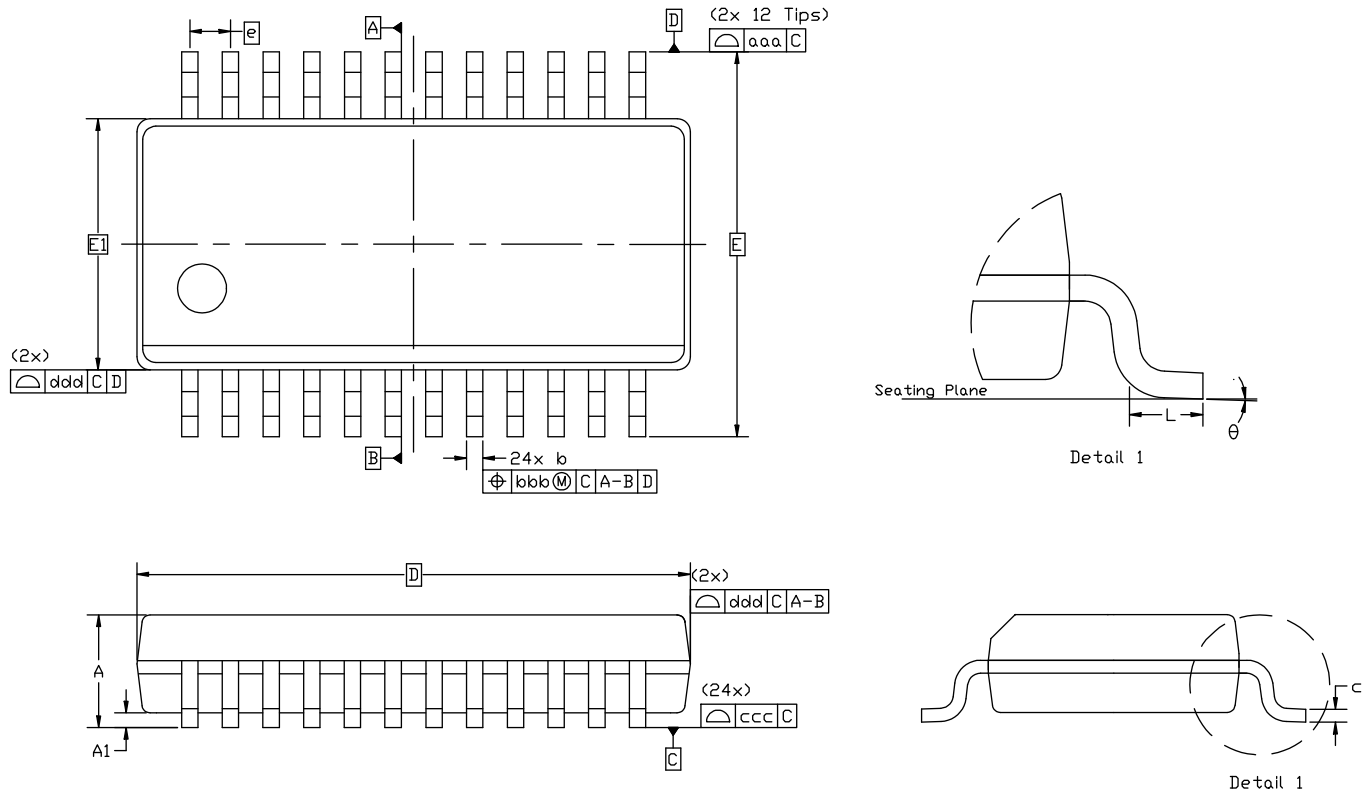


Figure 11.1. QSOP24 Package Drawing

Table 11.1. QSOP24 Package Dimensions

| Dimension | Min       | Typ | Max  |
|-----------|-----------|-----|------|
| A         | —         | —   | 1.75 |
| A1        | 0.10      | —   | 0.25 |
| b         | 0.20      | —   | 0.30 |
| c         | 0.10      | —   | 0.25 |
| D         | 8.65 BSC  |     |      |
| E         | 6.00 BSC  |     |      |
| E1        | 3.90 BSC  |     |      |
| e         | 0.635 BSC |     |      |

| Dimension | Min  | Typ | Max  |
|-----------|------|-----|------|
| L         | 0.40 | —   | 1.27 |
| theta     | 0°   | —   | 8°   |
| aaa       | 0.20 |     |      |
| bbb       | 0.18 |     |      |
| ccc       | 0.10 |     |      |
| ddd       | 0.10 |     |      |

**Note:**

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to JEDEC outline MO-137, variation AE.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.



11.2 QSOP24 PCB Land Pattern

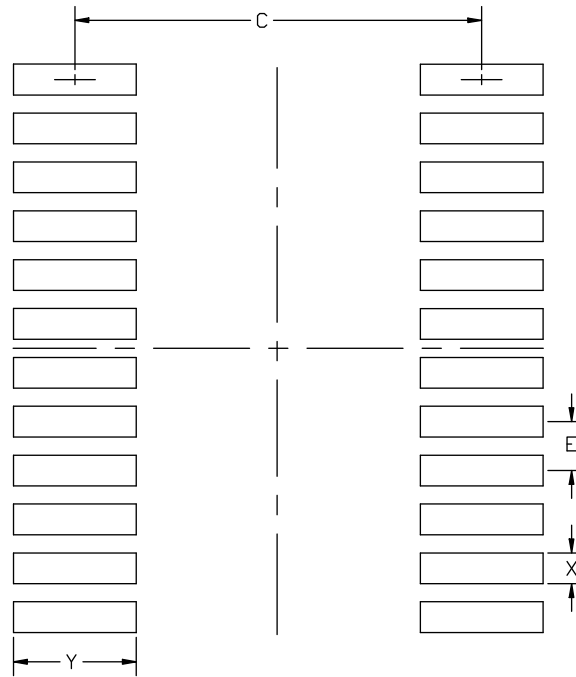


Figure 11.2. QSOP24 PCB Land Pattern Drawing

Table 11.2. QSOP24 PCB Land Pattern Dimensions

| Dimension | Min       | Max  |
|-----------|-----------|------|
| C         | 5.20      | 5.30 |
| E         | 0.635 BSC |      |
| X         | 0.30      | 0.40 |
| Y         | 1.50      | 1.60 |

**Note:**

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. This land pattern design is based on the IPC-7351 guidelines.
3. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60  $\mu\text{m}$  minimum, all the way around the pad.
4. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
5. The stencil thickness should be 0.125 mm (5 mils).
6. The ratio of stencil aperture to land pad size should be 1:1 for all perimeter pads.
7. A No-Clean, Type-3 solder paste is recommended.
8. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

### 11.3 QSOP24 Package Marking



Figure 11.3. QSOP24 Package Marking

The package marking consists of:

- P P P P P P P P – The part number designation.
- T T T T T T – A trace or manufacturing code.
- Y Y – The last 2 digits of the assembly year.
- W W – The 2-digit workweek when the device was assembled.
- # – The device revision (A, B, etc.).

## 12. Revision History

### 12.1 Revision 1.4

February 24, 2017

Updated A-grade QFN20 packaging information. The G-grade QFN20 and A-grade QFN20 devices now have different packages. Also fixed a typo in the X2 dimension for the QFN20G package.

### 12.2 Revision 1.3

September 23, 2016

Added A-grade parts.

Added [5.2 Debug](#).

Added bootloader pinout information and a reference to *AN945: EFM8 Factory Bootloader User Guide* in [3.10 Bootloader](#).

Added specifications for [4.1.16 SMBus](#).

Added CRC Calculation Time to [4.1.4 Flash Memory](#).

Added a note linking to the Typical VOH and VOL Performance graphs in [4.1.15 Port I/O](#).

Added the  $t_{POR}$  and adjusted the  $V_{POR}$  falling specifications in [4.1.3 Reset and Supply Monitor](#).

Added a note to [3.1 Introduction](#) referencing the Reference Manual.

Added a note to [3.2 Power](#) to clarify that entering Sleep may disconnect the active debug session.

Specified that the UART has a 1-byte FIFO in [3.6 Communications and Other Digital Peripherals](#).

### 12.3 Revision 1.2

Added CSP16 package.

Updated the "C2D / P2.0" pin on the QSOP24 pinout diagram to "C2D / P2.7."

Added crystal oscillator drive current typical values to [Table 4.7 Crystal Oscillator on page 18](#).

Corrected the number of capacitive sense channels for 24- and 20-pin packages in [Table 4.14 Capacitive Sense \(CS0\) on page 24](#).

Corrected E dimension shown in [Figure 8.2 QFN20 PCB Land Pattern Drawing on page 52](#).

Added more information to [3.10 Bootloader](#).

### 12.4 Revision 1.1

Initial release.

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# Table of Contents

|  |           |
|--|-----------|
| <b>1. Feature List</b>                           | <b>1</b>  |
| <b>2. Ordering Information</b>                   | <b>2</b>  |
| <b>3. System Overview</b>                        | <b>4</b>  |
| 3.1 Introduction                                 | 4         |
| 3.2 Power  | 5         |
| 3.3 I/O  | 5         |
| 3.4 Clocking                                     | 6         |
| 3.5 Counters/Timers and PWM                      | 6         |
| 3.6 Communications and Other Digital Peripherals | 7         |
| 3.7 Analog                                       | 9         |
| 3.8 Reset Sources                                | 10        |
| 3.9 Debugging                                    | 10        |
| 3.10 Bootloader                                  | 11        |
| <b>4. Electrical Specifications</b>              | <b>13</b> |
| 4.1 Electrical Characteristics                   | 13        |
| 4.1.1 Recommended Operating Conditions           | 13        |
| 4.1.2 Power Consumption                          | 14        |
| 4.1.3 Reset and Supply Monitor                   | 16        |
| 4.1.4 Flash Memory                               | 17        |
| 4.1.5 Power Management Timing                    | 17        |
| 4.1.6 Internal Oscillators                       | 17        |
| 4.1.7 Crystal Oscillator                         | 18        |
| 4.1.8 External Clock Input                       | 18        |
| 4.1.9 ADC  | 19        |
| 4.1.10 Voltage Reference                         | 20        |
| 4.1.11 Temperature Sensor                        | 21        |
| 4.1.12 Comparators                               | 22        |
| 4.1.13 Programmable Current Reference (IREF0)    | 23        |
| 4.1.14 Capacitive Sense (CS0)                    | 24        |
| 4.1.15 Port I/O                                  | 25        |
| 4.1.16 SMBus                                     | 26        |
| 4.2 Thermal Conditions                           | 28        |
| 4.3 Absolute Maximum Ratings                     | 28        |
| 4.4 Typical Performance Curves                   | 29        |
| <b>5. Typical Connection Diagrams</b>            | <b>31</b> |
| 5.1 Power  | 31        |
| 5.2 Debug  | 31        |
| 5.3 Other Connections                            | 32        |

|  |           |
|--|-----------|
| <b>6. Pin Definitions . . . . .</b>                | <b>33</b> |
| 6.1 EFM8SB1x-QFN20 Pin Definitions . . . . .       | .34       |
| 6.2 EFM8SB1x-QFN24 Pin Definitions . . . . .       | .37       |
| 6.3 EFM8SB1x-QSOP24 Pin Definitions . . . . .      | .40       |
| 6.4 EFM8SB1x-CSP16 Pin Definitions . . . . .       | .43       |
| <b>7. CSP16 Package Specifications . . . . .</b>   | <b>45</b> |
| 7.1 CSP16 Package Dimensions . . . . .             | .45       |
| 7.2 CSP16 PCB Land Pattern . . . . .               | .47       |
| 7.3 CSP16 Package Marking . . . . .                | .48       |
| <b>8. QFN20G Package Specifications . . . . .</b>  | <b>49</b> |
| 8.1 QFN20 Package Dimensions . . . . .             | .50       |
| 8.2 QFN20 PCB Land Pattern . . . . .               | .52       |
| 8.3 QFN20 Package Marking . . . . .                | .53       |
| <b>9. QFN20A Package Specifications . . . . .</b>  | <b>54</b> |
| 9.1 QFN20 Package Dimensions . . . . .             | .55       |
| 9.2 QFN20 PCB Land Pattern . . . . .               | .57       |
| 9.3 QFN20 Package Marking . . . . .                | .58       |
| <b>10. QFN24 Package Specifications . . . . .</b>  | <b>59</b> |
| 10.1 QFN24 Package Dimensions . . . . .            | .59       |
| 10.2 QFN24 PCB Land Pattern . . . . .              | .61       |
| 10.3 QFN24 Package Marking . . . . .               | .62       |
| <b>11. QSOP24 Package Specifications . . . . .</b> | <b>63</b> |
| 11.1 QSOP24 Package Dimensions . . . . .           | .63       |
| 11.2 QSOP24 PCB Land Pattern . . . . .             | .65       |
| 11.3 QSOP24 Package Marking . . . . .              | .66       |
| <b>12. Revision History . . . . .</b>              | <b>67</b> |
| 12.1 Revision 1.4 . . . . .                        | .67       |
| 12.2 Revision 1.3 . . . . .                        | .67       |
| 12.3 Revision 1.2 . . . . .                        | .67       |
| 12.4 Revision 1.1 . . . . .                        | .67       |
| <b>Table of Contents . . . . .</b>                 | <b>68</b> |

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