

## Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... -65°C to +150°C

Ambient Temperature with

Power Applied ..... -55°C to +125°C

Supply Voltage to Ground Potential ..... -0.5V to +7.0V

DC Voltage Applied to Outputs

in High Z State<sup>[2]</sup> ..... -0.5V to +7.0V

DC Input Voltage<sup>[2]</sup> ..... -0.5V to +7.0V

Output Current into Outputs (LOW) ..... 20 mA

Static Discharge Voltage ..... >2001V  
(per MIL-STD-883, Method 3015)

Latch-Up Current ..... >200 mA

## Operating Range

Range	Ambient Temperature	V <sub>CC</sub>
Commercial	0°C to +70°C	5V ± 10%
Industrial	-40°C to +85°C	5V ± 10%

## Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions	-15		-20		-25, -35		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
V <sub>OH</sub>	Output HIGH Voltage	V <sub>CC</sub> = Min., I <sub>OH</sub> = -4.0 mA	2.4		2.4		2.4		V
V <sub>OL</sub>	Output LOW Voltage	V <sub>CC</sub> = Min., I <sub>OL</sub> = 8.0 mA		0.4		0.4		0.4	V
V <sub>IH</sub>	Input HIGH Voltage		2.2	V <sub>CC</sub> + 0.3V	2.2	V <sub>CC</sub> + 0.3V	2.2	V <sub>CC</sub> + 0.3V	V
V <sub>IL</sub>	Input LOW Voltage <sup>[2]</sup>		-0.5	0.8	-0.5	0.8	-0.5	0.8	V
I <sub>IX</sub>	Input Leakage Current	GND ≤ V <sub>I</sub> ≤ V <sub>CC</sub>	-5	+5	-5	+5	-5	+5	μA
I <sub>OZ</sub>	Output Leakage Current	GND ≤ V <sub>I</sub> ≤ V <sub>CC</sub> , Output Disabled	-5	+5	-5	+5	-5	+5	μA
I <sub>CC</sub>	V <sub>CC</sub> Operating Supply Current	V <sub>CC</sub> = Max., I <sub>OUT</sub> = 0 mA		130		110		100	mA
I <sub>SB1</sub>	Automatic Power-Down Current	Max. V <sub>CC</sub> , CE <sub>1</sub> ≥ V <sub>IH</sub> or CE <sub>2</sub> ≤ V <sub>IL</sub> , Min. Duty Cycle = 100%		40		20		20	mA
I <sub>SB2</sub>	Automatic Power-Down Current	Max. V <sub>CC</sub> , CE <sub>1</sub> ≥ V <sub>CC</sub> - 0.3V, or CE <sub>2</sub> ≤ 0.3V V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.3V or V <sub>IN</sub> ≤ 0.3V		15		15		15	mA

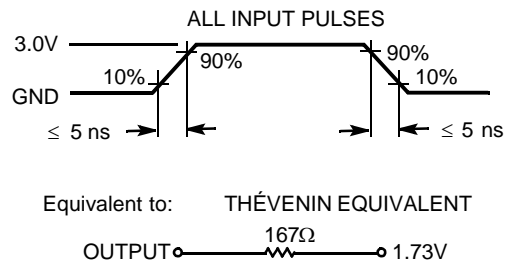
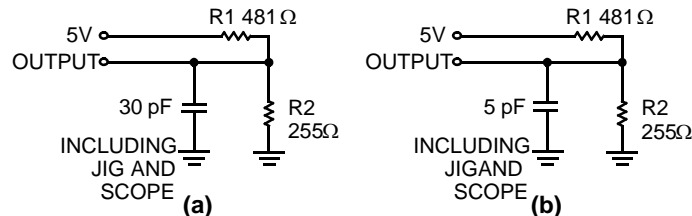
## Capacitance<sup>[3]</sup>

Parameter	Description	Test Conditions	Max.	Unit
C <sub>IN</sub>	Input Capacitance	T <sub>A</sub> = 25°C, f = 1 MHz, V <sub>CC</sub> = 5.0V	7	pF
C <sub>OUT</sub>	Output Capacitance		7	pF

### Notes:

- Minimum voltage is equal to -3.0V for pulse durations less than 30 ns.
- Tested initially and after any design or process changes that may affect these parameters.

## AC Test Loads and Waveforms



## Switching Characteristics Over the Operating Range<sup>[4]</sup>

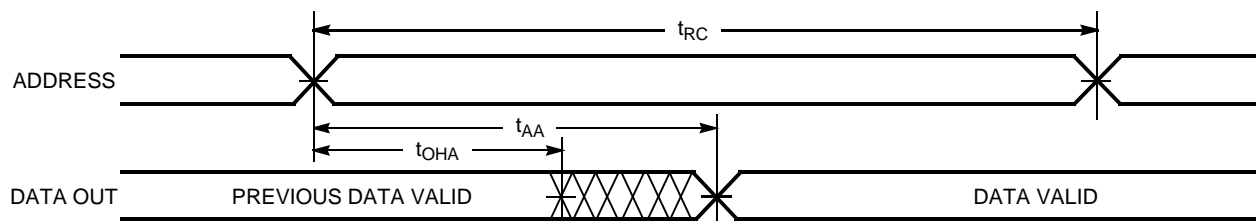
Parameter	Description	-15		-20		-25		-35		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle										
t <sub>RC</sub>	Read Cycle Time	15		20		25		35		ns
t <sub>AA</sub>	Address to Data Valid		15		20		25		35	ns
t <sub>OHA</sub>	Data Hold from Address Change	3		5		5		5		ns
t <sub>ACE1</sub>	$\overline{CE}_1$ LOW to Data Valid		15		20		25		35	ns
t <sub>ACE2</sub>	CE <sub>2</sub> HIGH to Data Valid		15		20		25		35	ns
t <sub>DOE</sub>	$\overline{OE}$ LOW to Data Valid		8		9		12		15	ns
t <sub>LZOE</sub>	$\overline{OE}$ LOW to Low Z	3		3		3		3		ns
t <sub>HZOE</sub>	$\overline{OE}$ HIGH to High Z <sup>[5]</sup>		7		8		10		10	ns
t <sub>LZCE1</sub>	$\overline{CE}_1$ LOW to Low Z <sup>[6]</sup>	3		5		5		5		ns
t <sub>LZCE2</sub>	CE <sub>2</sub> HIGH to Low Z	3		3		3		3		ns
t <sub>HZCE</sub>	$\overline{CE}_1$ HIGH to High Z <sup>[5, 6]</sup> CE <sub>2</sub> LOW to High Z		7		8		10		10	ns
t <sub>PU</sub>	$\overline{CE}_1$ LOW to Power-Up CE <sub>2</sub> to HIGH to Power-Up	0		0		0		0		ns
t <sub>PD</sub>	$\overline{CE}_1$ HIGH to Power-Down CE <sub>2</sub> LOW to Power-Down		15		20		20		20	ns
Write Cycle <sup>[7]</sup>										
t <sub>WC</sub>	Write Cycle Time	15		20		25		35		ns
t <sub>SCE1</sub>	$\overline{CE}_1$ LOW to Write End	12		15		20		20		ns
t <sub>SCE2</sub>	CE <sub>2</sub> HIGH to Write End	12		15		20		20		ns
t <sub>AW</sub>	Address Set-up to Write End	12		15		20		25		ns
t <sub>HA</sub>	Address Hold from Write End	0		0		0		0		ns
t <sub>SA</sub>	Address Set-up to Write Start	0		0		0		0		ns
t <sub>PWE</sub>	$\overline{WE}$ Pulse Width	12		15		15		20		ns
t <sub>SD</sub>	Data Set-up to Write End	8		10		10		12		ns
t <sub>HD</sub>	Data Hold from Write End	0		0		0		0		ns
t <sub>HZWE</sub>	$\overline{WE}$ LOW to High Z <sup>[5]</sup>		7		7		7		8	ns
t <sub>LZWE</sub>	$\overline{WE}$ HIGH to Low Z	3		5		5		5		ns

### Notes:

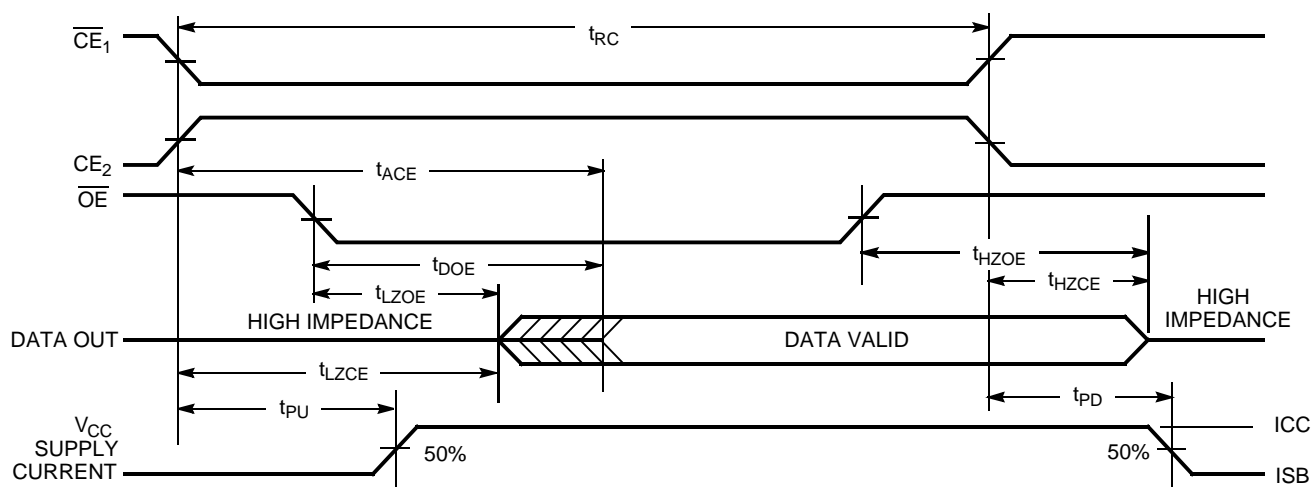
- Test conditions assume signal transition time of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified  $I_{OL}/I_{OH}$  and 30-pF load capacitance.
- $t_{HZOE}$ ,  $t_{HZCE}$ , and  $t_{HZWE}$  are specified with  $C_L = 5$  pF as in part (b) of AC Test Loads. Transition is measured  $\pm 500$  mV from steady state voltage.
- At any given temperature and voltage condition,  $t_{HZCE}$  is less than  $t_{LZCE1}$  and  $t_{LZCE2}$  for any given device.
- The internal write time of the memory is defined by the overlap of  $\overline{CE}_1$  LOW,  $CE_2$  HIGH, and  $\overline{WE}$  LOW. All 3 signals must be active to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.

## Switching Waveforms

### Read Cycle No.1<sup>[8,9]</sup>

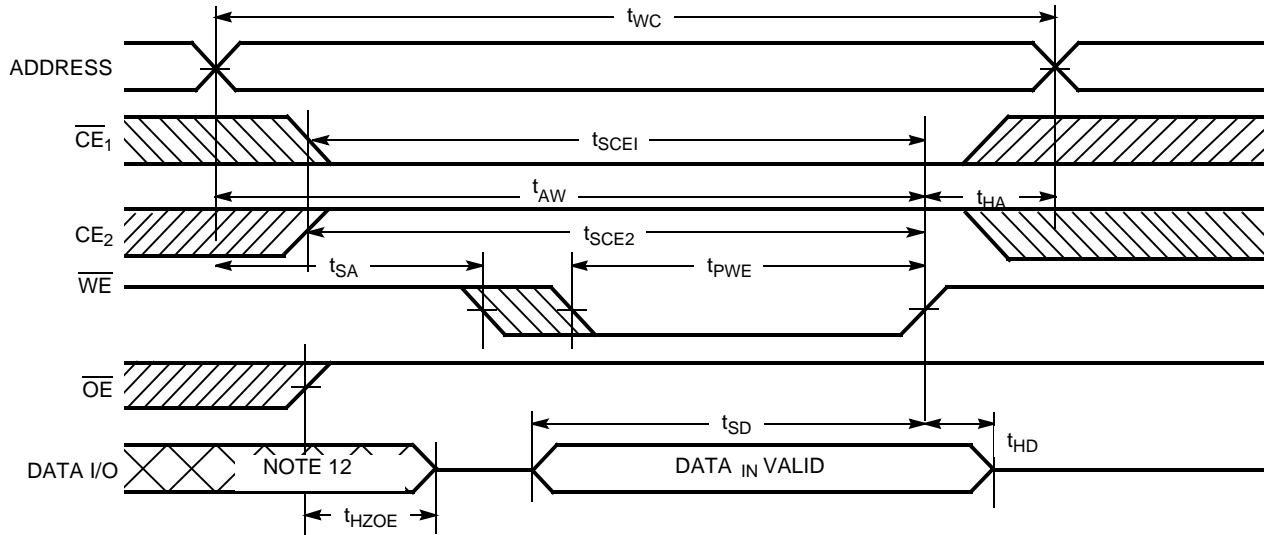
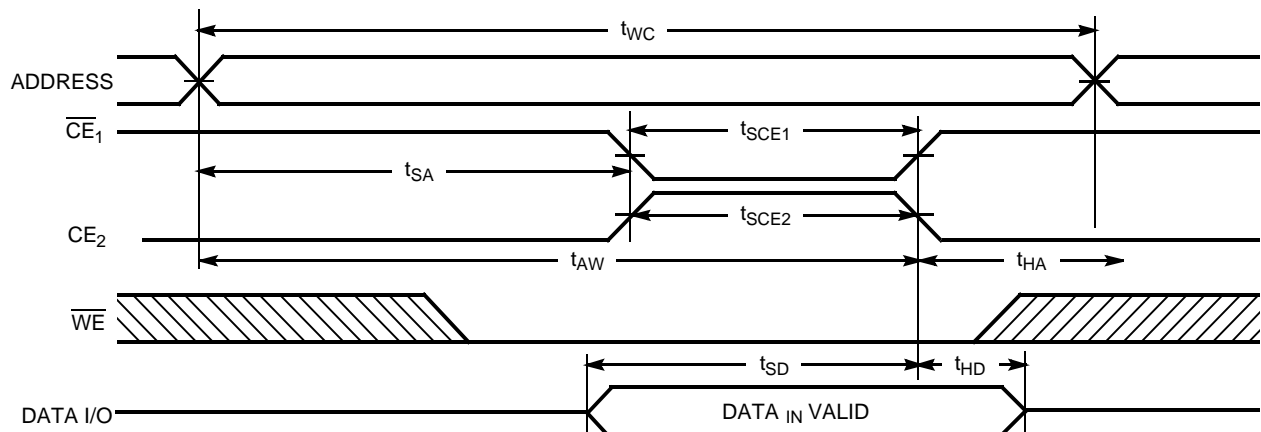


### Read Cycle No.2<sup>[10,11]</sup>

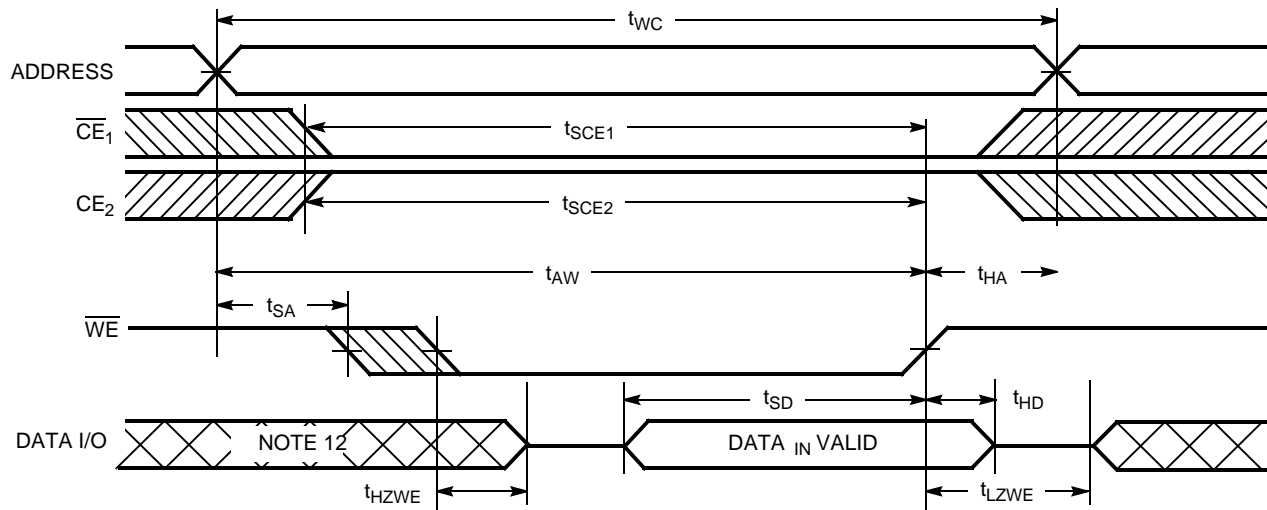


#### Notes:

8. Device is continuously selected.  $\overline{OE}$ ,  $\overline{CE}_1 = V_{IL}$ .  $CE_2 = V_{IH}$ .
9.  $\overline{WE}$  is HIGH for read cycle.
10. Data I/O is High Z if  $\overline{OE} = V_{IH}$ ,  $\overline{CE}_1 = V_{IH}$ ,  $\overline{WE} = V_{IL}$ , or  $CE_2 = V_{IL}$ .
11. The internal write time of the memory is defined by the overlap of  $\overline{CE}_1$  LOW,  $CE_2$  HIGH and  $\overline{WE}$  LOW.  $\overline{CE}_1$  and  $\overline{WE}$  must be LOW and  $CE_2$  must be HIGH to initiate write. A write can be terminated by  $\overline{CE}_1$  or  $\overline{WE}$  going HIGH or  $CE_2$  going LOW. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.

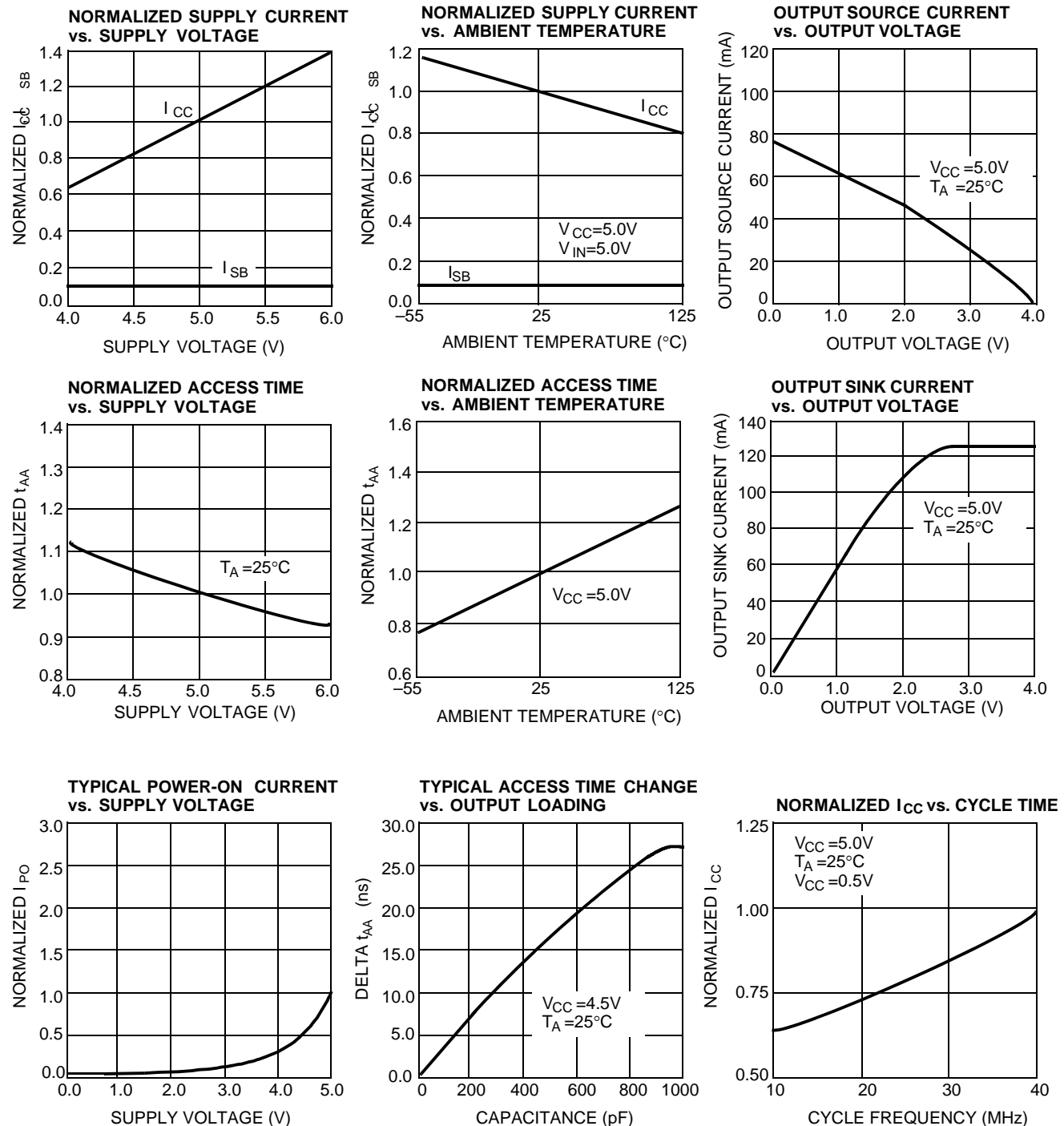
**Switching Waveforms (continued)**
**Write Cycle No. 1 ( $\overline{\text{WE}}$  Controlled)<sup>[9,11]</sup>**

**Write Cycle No. 2 ( $\overline{\text{CE}}$  Controlled)<sup>[11,12,13]</sup>**

**Notes:**

12. During this period, the I/Os are in the output state and input signals should not be applied.
13. The minimum write cycle time for write cycle #3 ( $\overline{\text{WE}}$  controlled,  $\overline{\text{OE}}$  LOW) is the sum of  $t_{\text{HZWE}}$  and  $t_{\text{SD}}$ .

**Switching Waveforms (continued)**
**Write Cycle No. 3 ( $\overline{\text{WE}}$  Controlled,  $\overline{\text{OE}}$  LOW)<sup>[11,12,13,14]</sup>**

**Note:**

14. If  $\overline{\text{CE}}_1$  goes HIGH or  $\text{CE}_2$  goes LOW simultaneously with  $\overline{\text{WE}}$  HIGH, the output remains in a high-impedance state.

## Typical DC and AC Characteristics



**Truth Table**

$\overline{CE}_1$	$\overline{CE}_2$	$\overline{WE}$	$\overline{OE}$	Input/Output	Mode
H	X	X	X	High Z	Deselect/Power-Down
X	L	X	X	High Z	Deselect/Power-Down
L	H	H	L	Data Out	Read
L	H	L	X	Data In	Write
L	H	H	H	High Z	Deselect

**Address Designators**

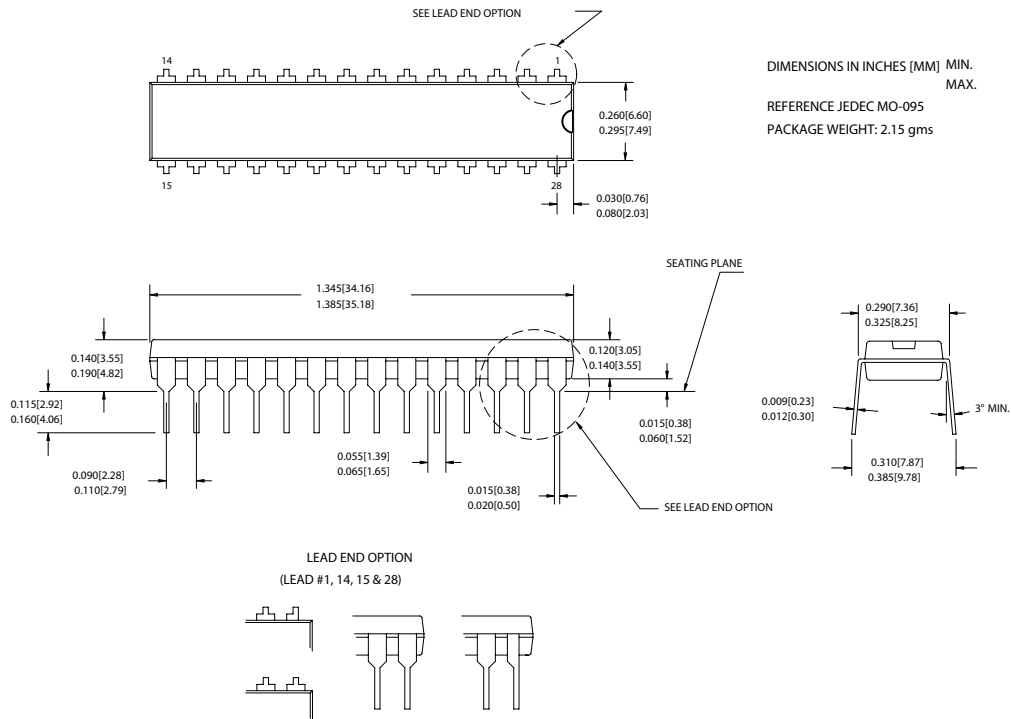
Address Name	Address Function	Pin Number
A4	X3	2
A5	X4	3
A6	X5	4
A7	X6	5
A8	X7	6
A9	Y1	7
A10	Y4	8
A11	Y3	9
A12	Y0	10
A0	Y2	21
A1	X0	23
A2	X1	24
A3	X2	25

**Ordering Information**

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
15	CY7C185-15VC	51-85031	28-pin (300-Mil) Molded SOJ	Commercial
	CY7C185-15VI		28-pin (300-Mil) Molded SOJ	Industrial
20	CY7C185-20PC	51-85014	28-pin (300-Mil) Molded DIP	Commercial
	CY7C185-20PXC		28-pin (300-Mil) Molded DIP (Pb-free)	
	CY7C185-20VC	51-85031	28-pin (300-Mil) Molded SOJ	
25	CY7C185-25PC	51-85014	28-pin (300-Mil) Molded DIP	Commercial
	CY7C185-25VC	51-85031	28-pin (300-Mil) Molded SOJ	
35	CY7C185-35PC	51-85014	28-pin (300-Mil) Molded DIP	Commercial
	CY7C185-35SC	51-85026	28-pin (300-Mil) Molded SOIC	

## Package Diagrams

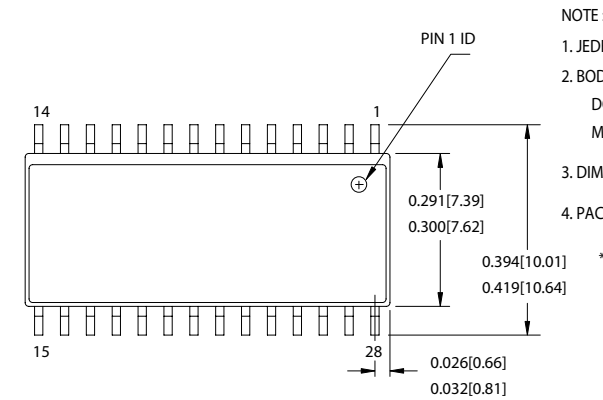
### 28-pin (300-Mil) PDIP (51-85014)





Package Diagrams (continued)

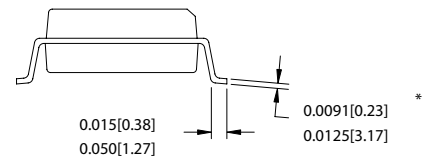
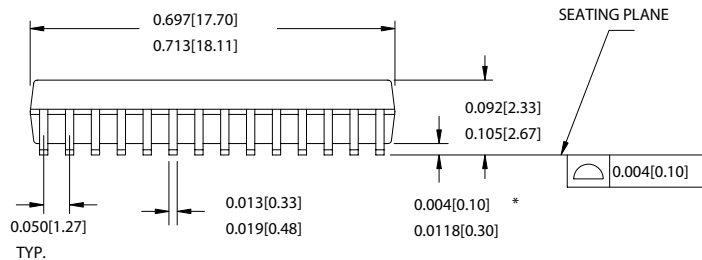
28-pin (300-Mil) Molded SOIC (51-85026)



NOTE:

1. JEDEC STD REF MO-119
2. BODY LENGTH DIMENSION DOES NOT INCLUDE MOLD PROTRUSION/END FLASH, BUT DOES INCLUDE MOLD MISMATCH AND ARE MEASURED AT THE MOLD PARTING LINE. MOLD PROTRUSION/END FLASH SHALL NOT EXCEED 0.010 in (0.254 mm) PER SIDE
3. DIMENSIONS IN INCHES - MIN. MAX.
4. PACKAGE WEIGHT 0.85gms

PART #	
S28.3	STANDARD PKG.
SZ28.3	LEAD FREE PKG.



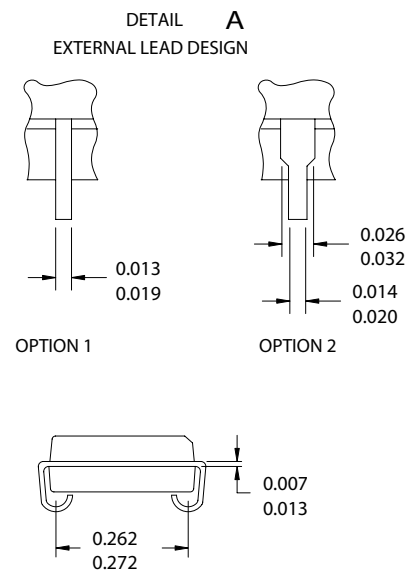
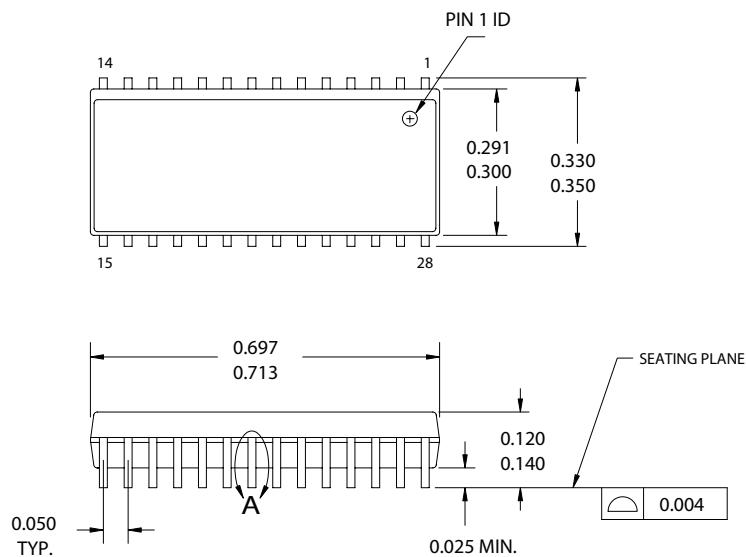
51-85026-\*D

## Package Diagrams (continued)

### 28-pin (300-Mil) Molded SOJ (51-85031)

NOTE :

1. JEDEC STD REF MO088
2. BODY LENGTH DIMENSION DOES NOT INCLUDE MOLD PROTRUSION/END FLASH  
MOLD PROTRUSION/END FLASH SHALL NOT EXCEED 0.006 in (0.152 mm) PER SIDE
3. DIMENSIONS IN INCHES                MIN.  
   MAX.



51-85031-\*C

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**Document History Page**

Document Title: CY7C185 8K x 8 Static RAM Document Number: 38-05043				
REV.	ECN NO.	Issue Date	Orig. of Change	Description of Change
**	107145	09/10/01	SZV	Change from Spec number: 38-00037 to 38-05043
*A	116470	09/16/02	CEA	Add applications foot note to data sheet
*B	486744	See ECN	NXR	Changed Low standby power from 220mW to 85mW Changed the description of $I_{IX}$ from Input Load Current to Input Leakage Current in DC Electrical Characteristics table Removed $I_{OS}$ parameter from DC Electrical Characteristics table Updated the Ordering Information table