

## Ordering Information

Device	8-Lead SOIC (w/Heat Slug) 4.90x3.90mm body 1.70mm height (max) 1.27mm pitch
CL330	CL330SG-G

-G indicates package is RoHS compliant ('Green')



## Absolute Maximum Ratings

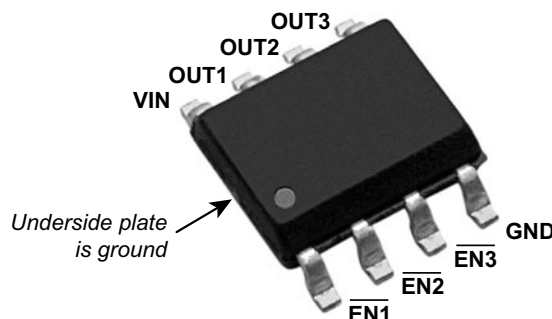
Parameter	Value
Supply voltage, $V_{IN}$	-0.5V to +100V
Output voltage, $V_{OUT}$	-0.5V to +100V
Enable voltage, $V_{EN}$	-0.5V to +6.5V
Operating temperature <sup>1</sup>	-40°C
Storage temperature	-65°C to +150°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied. Continuous operation of the device at the absolute rating level may affect device reliability. All voltages are referenced to device ground.

### Note:

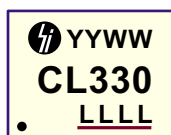
1. Maximum junction temperature internally limited.

## Pin Configuration



8-Lead SOIC (w/Heat Slug) (SG)

## Product Marking



YY = Year Sealed  
WW = Week Sealed  
L = Lot Number  
\_\_\_\_\_ = "Green" Packaging

8-Lead SOIC (w/Heat Slug) (SG)

## Recommended Operating Conditions (all voltages with respect to GND pin)

Sym	Parameter	Min	Typ	Max	Units	Conditions
$V_{IN}$	Supply voltage	6.5	-	90	V	---
$V_{OUT}$	Output voltage	4.0	-	15	V	$\overline{EN} = 0$
				90	V	$\overline{EN} = 1$
$f_{EN}$	Enable toggling frequency	0	-	100	kHz	---
$T_J$	Junction temperature	-40	-	119	°C	---
$C_{IN}$	$V_{IN}$ capacitor	-	100	-	nF	---

## Thermal Characteristics

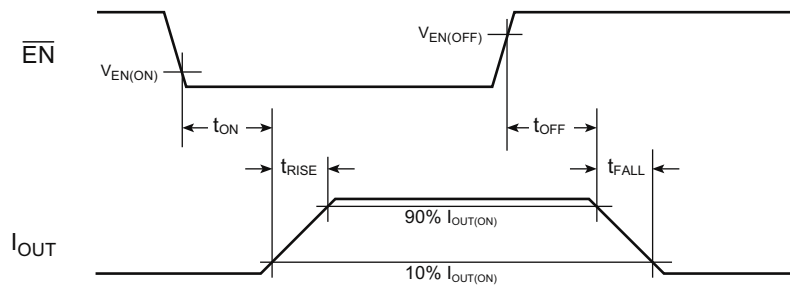
Sym	Parameter	Min	Typ	Max	Units	Conditions
$\theta_{JA}$	Thermal resistance, junction to ambient	-	48	-	°C/W	Mounted on JEDEC test PCB (2s 2p)
$T_{LIM}$	Over-temperature limit	120	135	150	°C	---
$T_{HYS}$	Over-temperature hysteresis	-	30	-	°C	---

## Electrical Characteristics

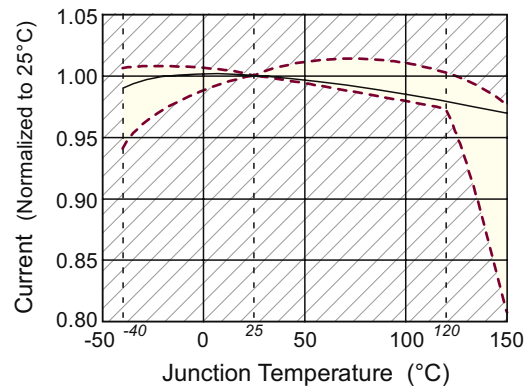
(Over recommended operating conditions.  $T_A$  @ 25°C unless otherwise specified.)

Sym	Parameter	Min	Typ	Max	Units	Conditions
$I_{IN}$	$V_{IN}$ supply current	-	220	250	$\mu A$	$\overline{EN}_{1-3} = 1$
		-	2.2	2.3	mA	$\overline{EN}_{1-3} = 0$
$I_{OUT(OFF)}$	Output current, off	-	4.0	10	$\mu A$	$\overline{EN}_x = 1$
$I_{OUT(ON)}$	Output current, on	-	-	31.8	mA	$\overline{EN}_x = 0, V_{OUT} = 0 - 4.0V$
		28.2	30.0	31.8		$\overline{EN}_x = 0, V_{OUT} = 4.0 - 15V$
		27.0	30.0	33.0		$\overline{EN}_x = 0, V_{OUT} = 15 - 90V$
$V_{EN(ON)}$	Enable voltage, on	-	-	0.8	V	---
$V_{EN(OFF)}$	Enable voltage, off	2.4	-	-	V	---
$C_{EN}$	Enable input capacitance	-	5.0	10	pF	---
$I_{ENL}$	Enable low input current	-	-	1.0	$\mu A$	$V_{EN} = 0V$
$I_{ENH}$	Enable high input current	-	-	1.0	$\mu A$	$V_{EN} = 5.0V$
$t_{ON}$	Enable on delay	-	2.0	2.4	$\mu s$	---
$t_{RISE}$	Output current rise time	-	1.0	1.2	$\mu s$	---
$t_{OFF}$	Enable off delay	-	440	800	ns	---
$t_{FALL}$	Output current fall time	-	170	250	ns	---

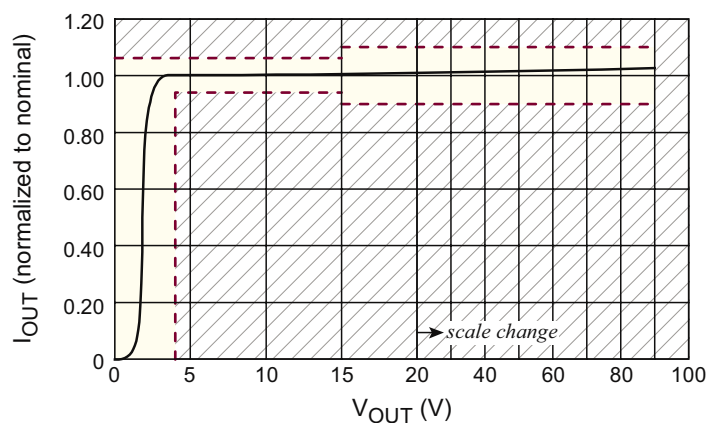
## Timing



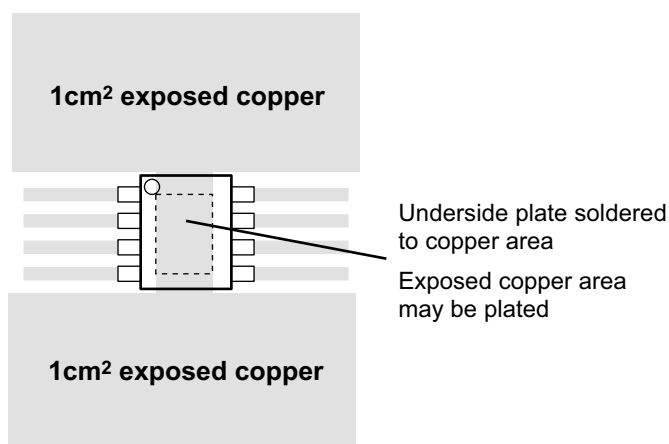
## Temperature Effects



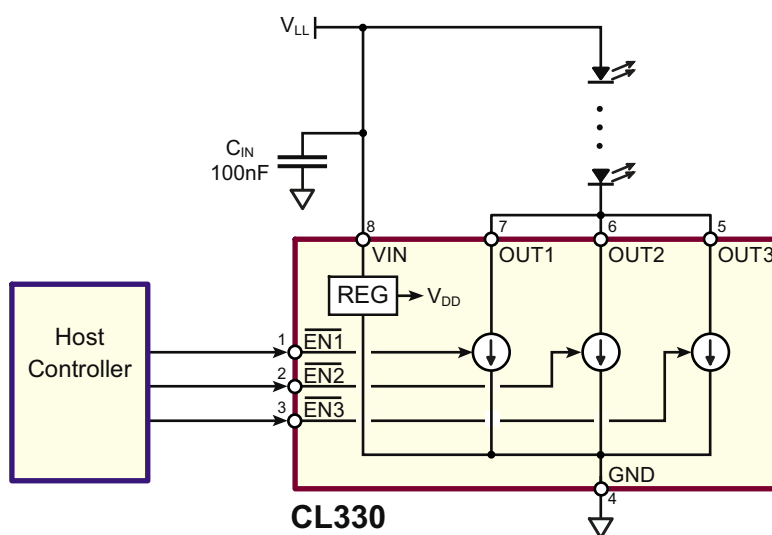
## Load Regulation



## Recommended PCB Layout

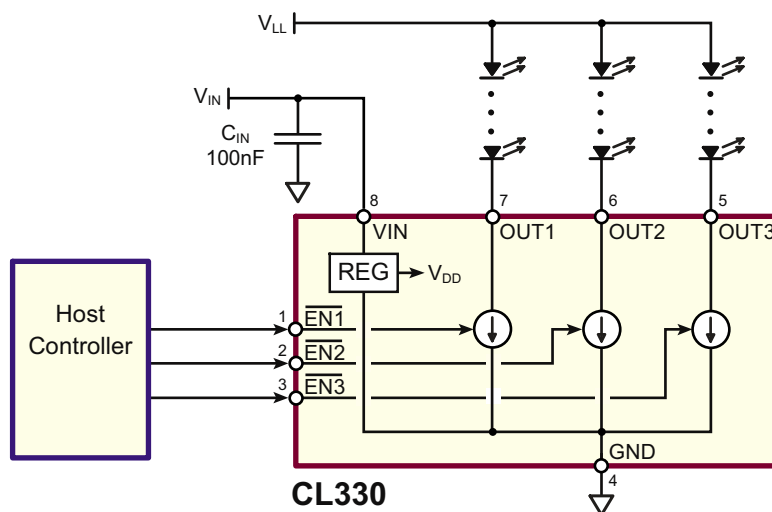


## Higher LED Current



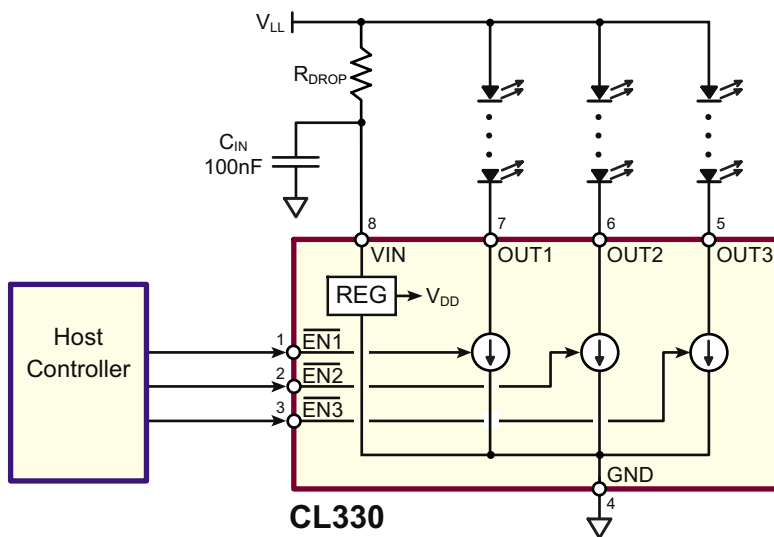
By paralleling outputs, higher LED currents can be achieved. In addition, linear dimming in 3 discrete steps may be obtained by enabling 1, 2, or 3 outputs.

## Lowering CL330 Power Dissipation: Separate $V_{IN}$ Supply



CL330 power dissipation may be lowered by supplying the CL330 from a voltage source ( $V_{IN}$ ) that is lower in voltage than the LED supply ( $V_{LL}$ ).

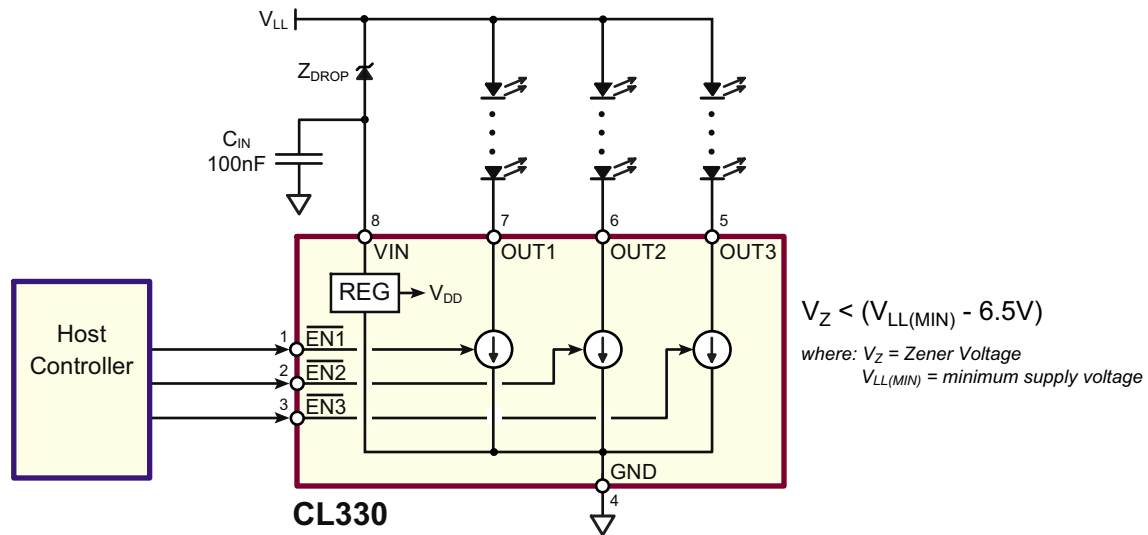
## Lowering CL330 Power Dissipation: Dropping Resistor



$$R_{DROP} < \frac{V_{LL(MIN)} - 6.5V}{2.3mA}$$

where:  $R_{DROP}$  = Dropping resistance  
 $V_{LL(MIN)}$  = minimum supply voltage

## Lowering CL330 Power Dissipation: Zener Diode

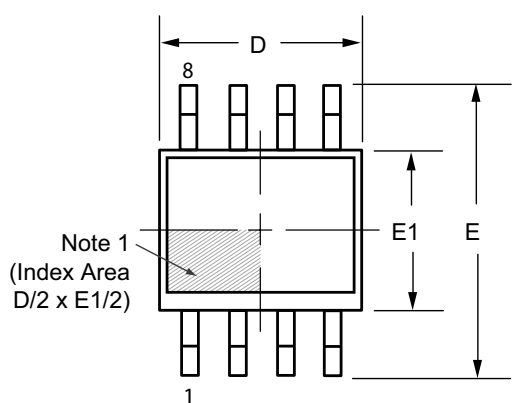


## Pin Description

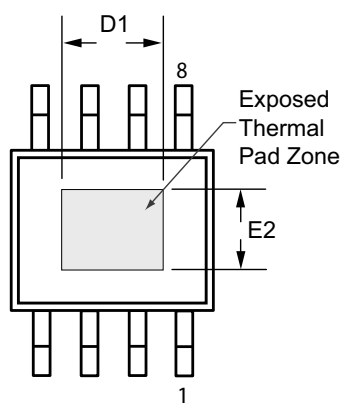
Pin #	Name	Description
1	$\overline{EN1}$	Output enable, active low.
2	$\overline{EN2}$	
3	$\overline{EN3}$	
4	GND	Circuit common.
5	OUT3	Constant current output (sinking). Connect the cathodes of the LEDs to these pins.
6	OUT2	
7	OUT1	
8	VIN	Supply voltage. 6.5 to 90V. Bypass locally with a 100nF capacitor to ground.
Underside Plate	GND	The exposed underside plate is internally connected to the GND pin. The plate may either be left floating or connected to ground. Solder the plate to an exposed copper area on the PCB for heatsinking purposes (see recommended layout).

## 8-Lead SOIC (Narrow Body w/Heat Slug) Package Outline (SG)

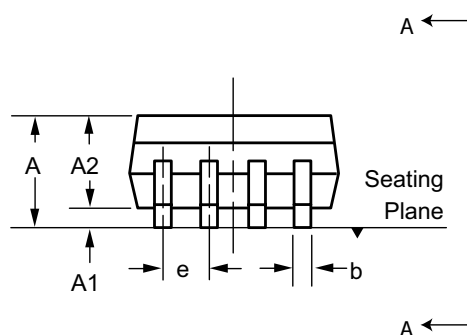
4.90x3.90mm body, 1.70mm height (max), 1.27mm pitch



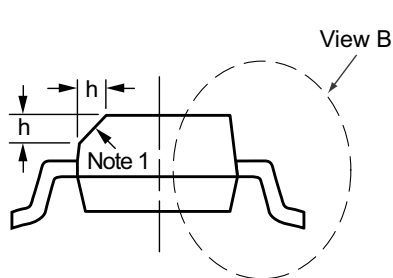
**Top View**



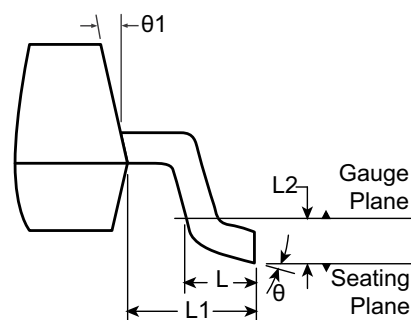
**Bottom View**



**Side View**



**View A - A**



**View B**

### Notes:

1. A Pin 1 identifier must be located in the index area indicated. The Pin 1 identifier can be: a molded mark/identifier; an embedded metal marker; or a printed indicator.

Symbol		A	A1	A2	b	D	D1	E	E1	E2	e	h	L	L1	L2	θ	θ1
Dimension (mm)	MIN	1.25*	0.00	1.25	0.31	4.80*	3.30 <sup>†</sup>	5.80*	3.80*	2.29 <sup>†</sup>	1.27 BSC	0.25	0.40	1.04 REF	0.25 BSC	0°	5°
	NOM	-	-	-	-	4.90	-	6.00	3.90	-		-	-			-	
	MAX	1.70	0.15	1.55*	0.51	5.00*	3.81 <sup>†</sup>	6.20*	4.00*	2.79 <sup>†</sup>		0.50	1.27			8°	15°

JEDEC Registration MS-012, Variation BA, Issue E, Sept. 2005.

\* This dimension is not specified in the original JEDEC drawing. The value listed is for reference only.

† This dimension is a non-JEDEC dimension.

**Drawings not to scale.**

**Supertex Doc. #: DSPD-8SOSG, Version C090408.**

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to <http://www.supertex.com/packaging.html>.)

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