**Static @ $T_J$ = 25°C (unless otherwise specified)**

| | Parameter | Min. | Typ. | Max. | Units | Conditions |
|---|---|---|---|---|---|---|
| $V_{(BR)DSS}$ | Drain-to-Source Breakdown Voltage | 300 | — | — | V | $V_{GS}$ = 0V, $I_D$ = 250µA |
| $\Delta V_{(BR)DSS}/\Delta T_J$ | Breakdown Voltage Temp. Coefficient | — | 0.39 | — | V/°C | Reference to 25°C, $I_D$ = 5.0mA |
| $R_{DS(on)}$ | Static Drain-to-Source On-Resistance | — | 148 | 185 | mΩ | $V_{GS}$ = 10V, $I_D$ = 11A ③ |
| $V_{GS(th)}$ | Gate Threshold Voltage | 3.0 | — | 5.0 | V | $V_{DS}$ = $V_{GS}$, $I_D$ = 150µA |
| gfs | Forward Trans conductance | 15 | — | — | S | $V_{DS}$ = 50V, $I_D$ = 11A |
| $I_{DSS}$ | Drain-to-Source Leakage Current | — | — | 20 | µA | $V_{DS}$ = 300V, $V_{GS}$ = 0V |
| | | — | — | 250 | | $V_{DS}$ = 300V,$V_{GS}$ = 0V,$T_J$ =125°C |
| $I_{GSS}$ | Gate-to-Source Forward Leakage | — | — | 100 | nA | $V_{GS}$ = 20V |
| | Gate-to-Source Reverse Leakage | — | — | -100 | | $V_{GS}$ = -20V |

**Dynamic Electrical Characteristics @ $T_J$ = 25°C (unless otherwise specified)**

| | | | | | | |
|---|---|---|---|---|---|---|
| $Q_g$ | Total Gate Charge | — | 38 | 57 | nC | $I_D$ = 11A |
| $Q_{gs}$ | Gate-to-Source Charge | — | 12 | — | | $V_{DS}$ = 150V |
| $Q_{gd}$ | Gate-to-Drain Charge | — | 13 | — | | $V_{GS}$ = 10V③ |
| $t_{d(on)}$ | Turn-On Delay Time | — | 15 | — | ns | $V_{DD}$ = 300V |
| $t_r$ | Rise Time | — | 16 | — | | $I_D$ = 11A |
| $t_{d(off)}$ | Turn-Off Delay Time | — | 22 | — | | $R_G$= 5.0Ω |
| $t_f$ | Fall Time | — | 10 | — | | $V_{GS}$ = 10V ③ |
| $L_D$ | Internal Drain Inductance | — | 4.5 | — | nH | Between lead, 6mm (0.25in.) from package and center of die contact |
| $L_S$ | Internal Source Inductance | — | 7.5 | — | | |
| $C_{iss}$ | Input Capacitance | — | 2340 | — | pF | $V_{GS}$ = 0V |
| $C_{oss}$ | Output Capacitance | — | 195 | — | | $V_{DS}$ = 25V |
| $C_{rss}$ | Reverse Transfer Capacitance | — | 40 | — | | $f$ = 1.0MHz |
| $C_{oss}$ | Output Capacitance | — | 1750 | — | | $V_{GS}$ = 0V, $V_{DS}$ = 1.0V $f$ = 1.0MHz |
| $C_{oss}$ | Output Capacitance | — | 66 | — | | $V_{GS}$ = 0V, $V_{DS}$ = 240V $f$ = 1.0MHz |
| $C_{oss\ eff.}$ | Effective Output Capacitance | — | 130 | — | | $V_{GS}$ = 0V, $V_{DS}$ = 0V to 240V ④ |

**Diode Characteristics**

| | Parameter | Min. | Typ. | Max. | Units | Conditions |
|---|---|---|---|---|---|---|
| $I_S$ | Continuous Source Current (Body Diode) | — | — | 19 | A | MOSFET symbol showing the integral reverse p-n junction diode. |
| $I_{SM}$ | Pulsed Source Current (Body Diode) ① | — | — | 100 | | |
| $V_{SD}$ | Diode Forward Voltage | — | — | 1.3 | V | $T_J$ = 25°C,$I_S$ = 11A,$V_{GS}$ = 0V ③ |
| $t_{rr}$ | Reverse Recovery Time | — | 190 | 285 | ns | $T_J$ = 25°C ,$I_F$ = 11A, $V_{DD}$ = 150V |
| $Q_{rr}$ | Reverse Recovery Charge | — | 990 | 1485 | nC | di/dt = 100A/µs ③ |
| $t_{on}$ | Forward Turn-On Time | Intrinsic turn-on time is negligible (turn-on is dominated by $L_S$+$L_D$) | | | | |

**Notes:**

① Repetitive rating; pulse width limited by max. junction temperature. (See fig. 11)

② Limited by $T_{Jmax}$, starting $T_J$ = 25°C, L = 3.6mH, $R_G$ = 50Ω, $I_{AS}$ = 11A, $V_{GS}$ =10V. Part not recommended for use above this value.

③ Pulse width ≤ 1.0ms; duty cycle ≤ 2%.

④ $C_{oss}$ eff. is a fixed capacitance that gives the same charging time as $C_{oss}$ while $V_{DS}$ is rising from 0 to 80% $V_{DSS}$.

⑤ Limited by $T_{Jmax}$ , see Fig.12a, 12b, 15, 16 for typical repetitive avalanche performance.

⑥ This value determined from sample failure population, starting $T_J$ = 25°C, L = 3.6mH, $R_G$ = 50Ω, $I_{AS}$ = 11A, $V_{GS}$ =10V.

⑦ This is applied to $D^2$Pak When mounted on 1" square PCB (FR-4 or G-10 Material). For recommended footprint and soldering techniques refer to application note #AN-994

⑧ $R_\theta$ is measured at $T_J$ approximately 90°C.

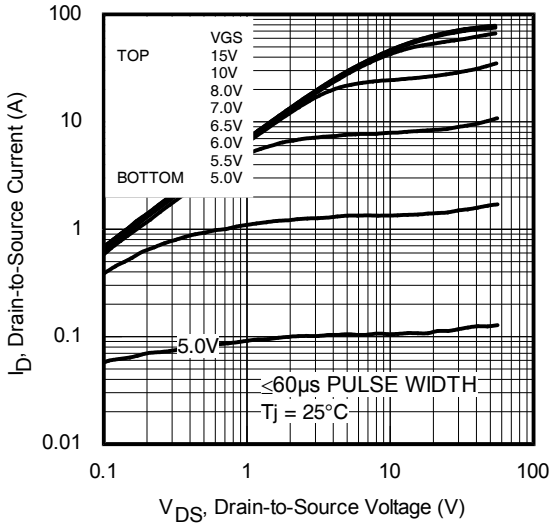



**Fig. 1** Typical Output Characteristics

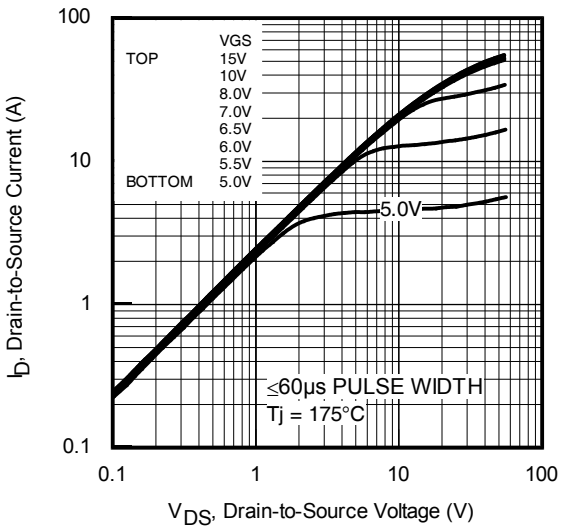



**Fig. 2** Typical Output Characteristics

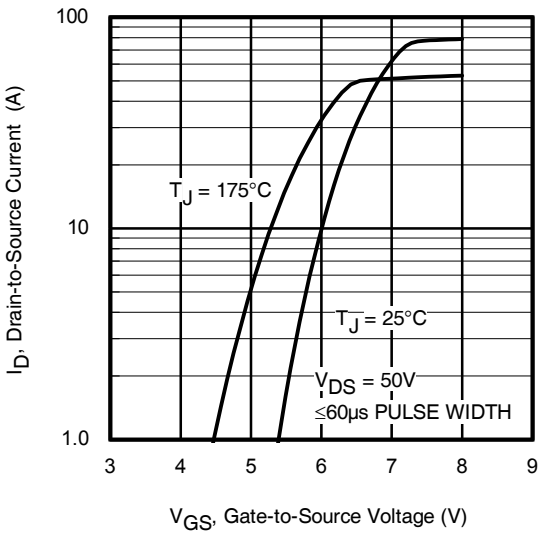



**Fig. 3** Typical Transfer Characteristics

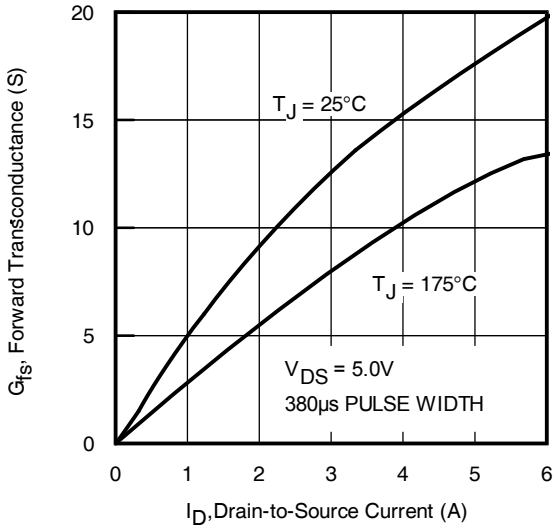



**Fig. 4** Typical Forward Trans conductance vs. Drain Current

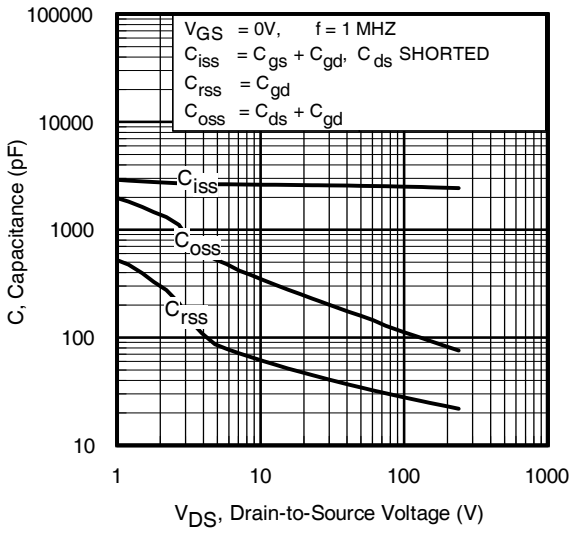



**Fig 5.** Typical Capacitance vs. Drain-to-Source Voltage

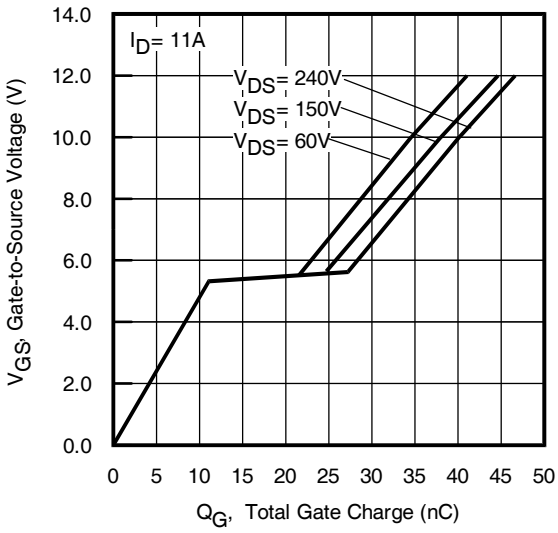



**Fig 6.** Typical Gate Charge vs. Gate-to-Source Voltage

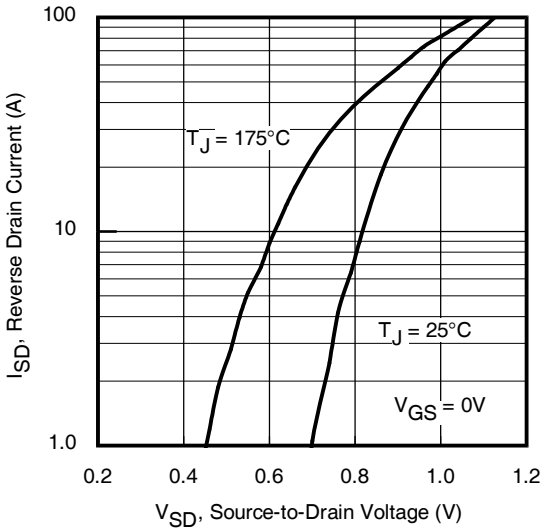



**Fig. 7** Typical Source-to-Drain Diode Forward Voltage

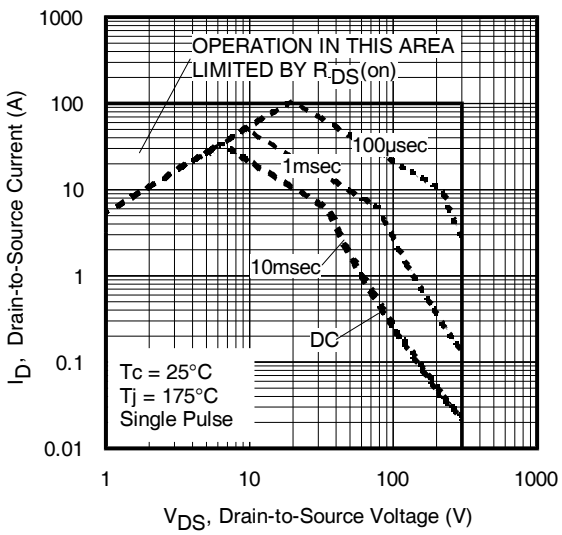



**Fig 8.** Maximum Safe Operating Area

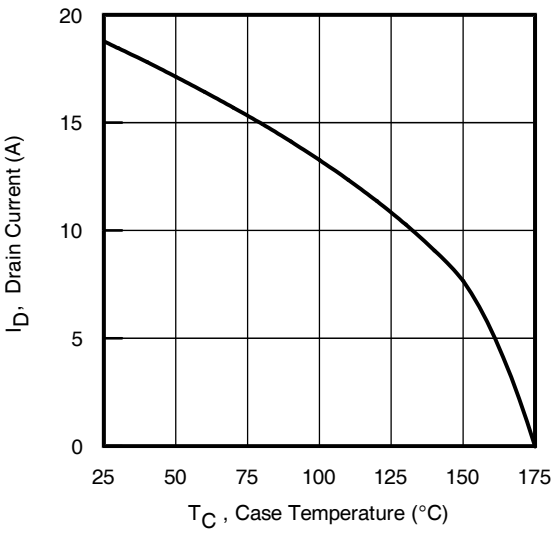



**Fig 9.** Maximum Drain Current vs. Case Temperature

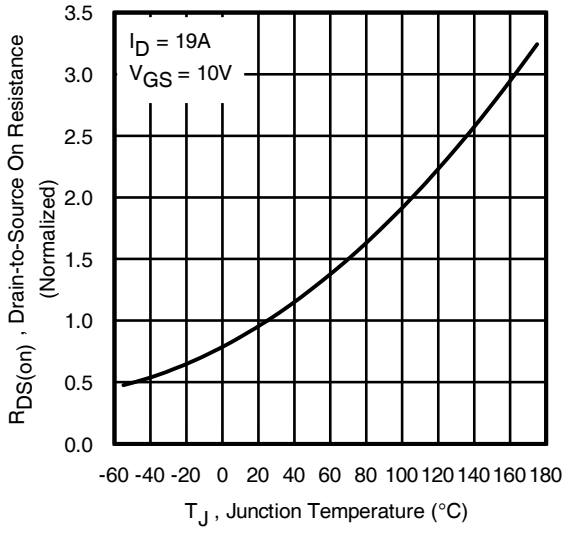



**Fig 10.** Normalized On-Resistance vs. Temperature

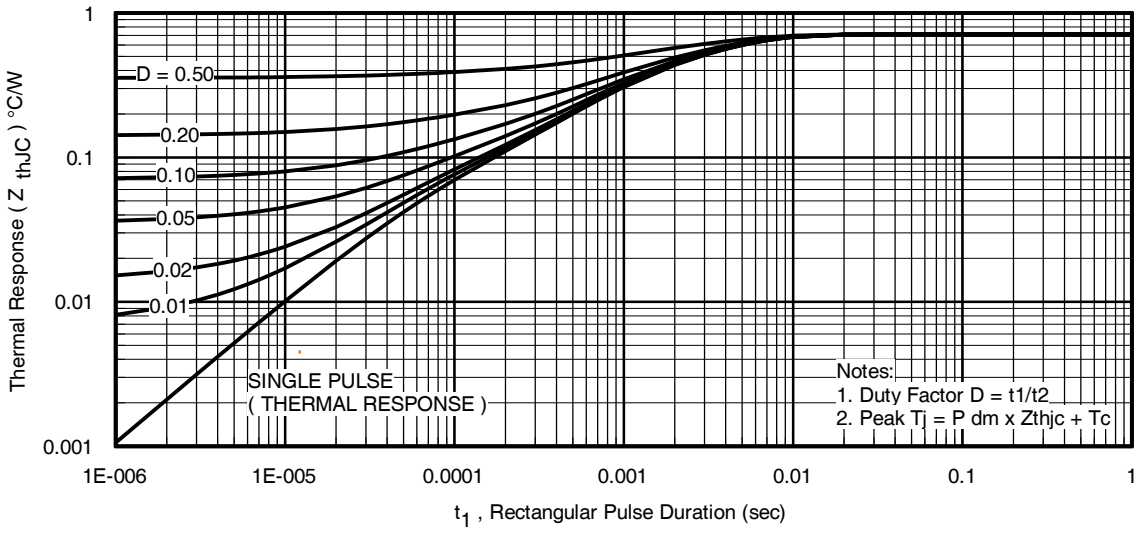



**Fig 11.** Maximum Effective Transient Thermal Impedance, Junction-to-Case

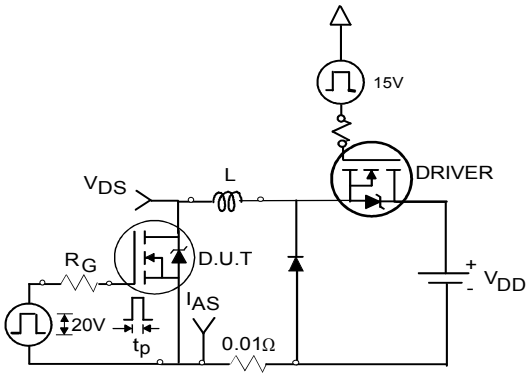



**Fig 12a.** Unclamped Inductive Test Circuit

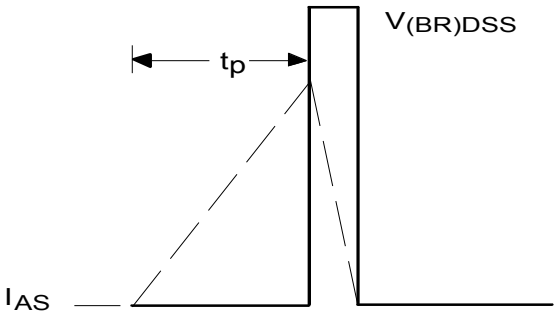



**Fig 12b.** Unclamped Inductive Waveforms

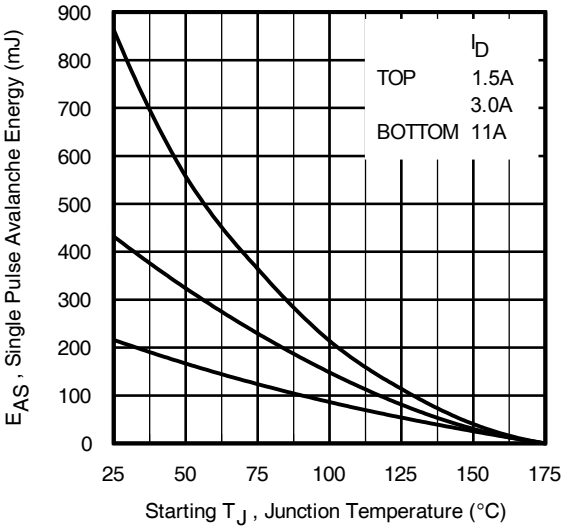



**Fig 12c.** Maximum Avalanche Energy vs. Drain Current

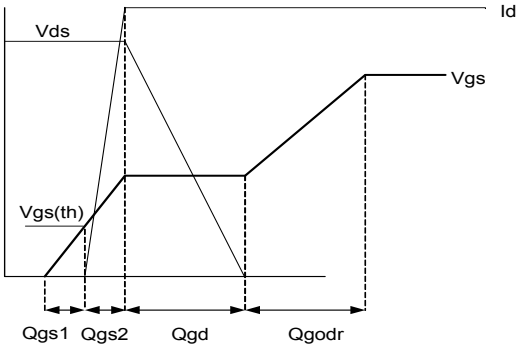



**Fig 13a.** Gate Charge Waveform

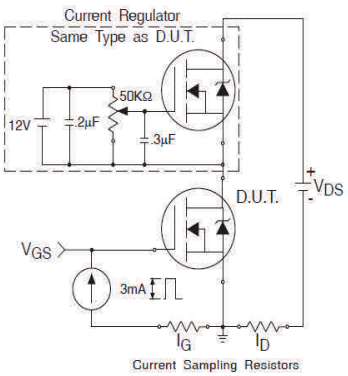



**Fig 13b.** Gate Charge Test Circuit

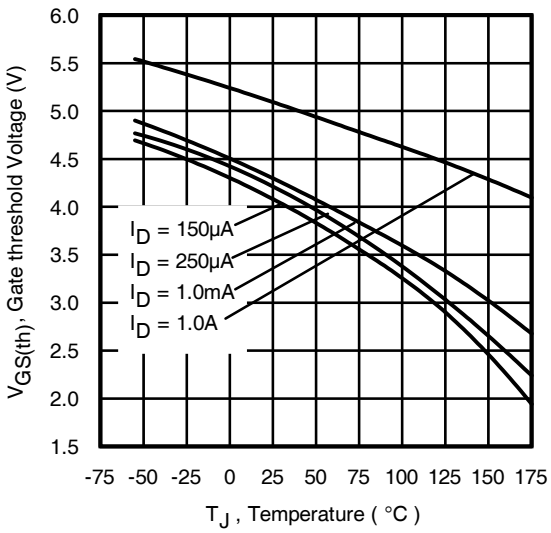



**Fig 14.** Threshold Voltage vs. Temperature

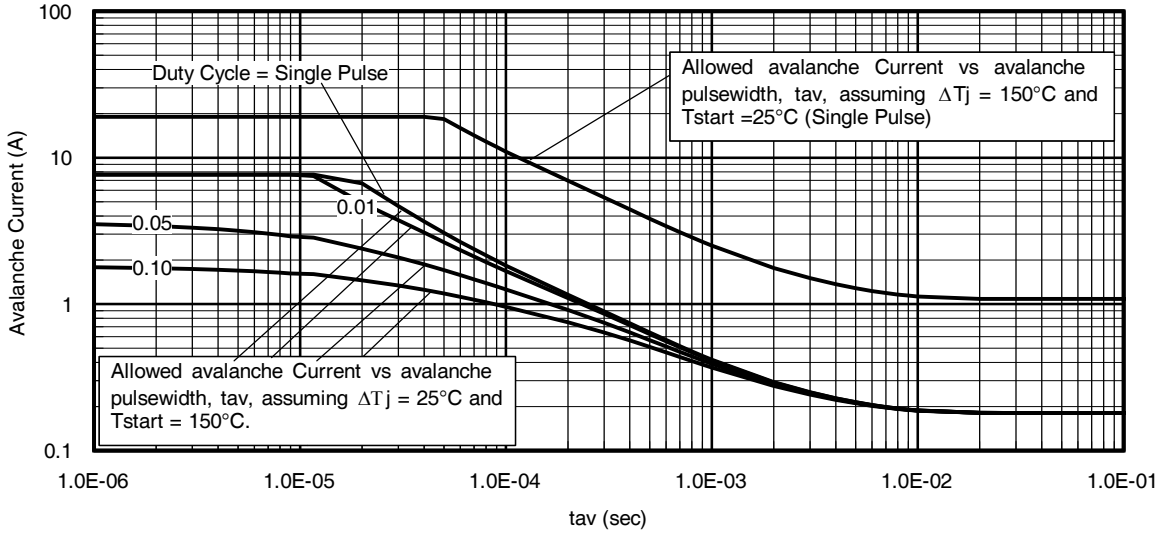



**Fig 15.** Typical Avalanche Current vs. Pulse width

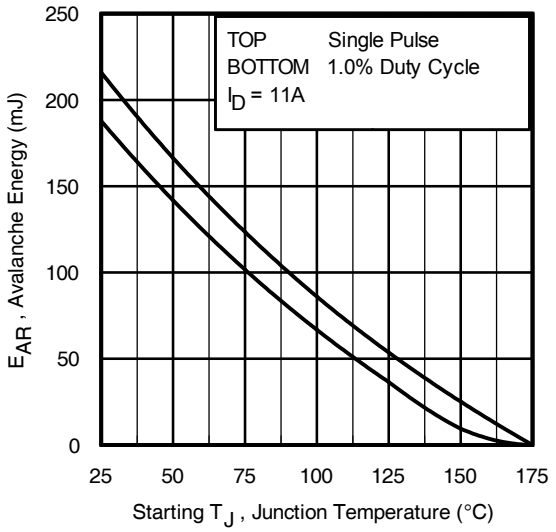



**Fig 16.** Maximum Avalanche Energy vs. Temperature

**Notes on Repetitive Avalanche Curves , Figures 15, 16:**
**(For further info, see AN-1005 at www.infineon.com)**

1. Avalanche failures assumption:
   Purely a thermal phenomenon and failure occurs at a temperature far in excess of $T_{jmax}$. This is validated for every part type.
2. Safe operation in Avalanche is allowed as long as $T_{jmax}$ is not exceeded.
3. Equation below based on circuit and waveforms shown in Figures 12a, 12b.
4. $P_{D\ (ave)}$ = Average power dissipation per single avalanche pulse.
5. BV = Rated breakdown voltage (1.3 factor accounts for voltage increase during avalanche).
6. $I_{av}$ = Allowable avalanche current.
7. $\Delta T$ = Allowable rise in junction temperature, not to exceed $T_{jmax}$ (assumed as 25°C in Figure 15, 16).
   $t_{av}$ = Average time in avalanche.
   D = Duty cycle in avalanche = $t_{av} \cdot f$
   $Z_{thJC}(D, t_{av})$ = Transient thermal resistance, see Figures 13)

$$P_{D\ (ave)} = 1/2\ (1.3 \cdot BV \cdot I_{av}) = \Delta T / Z_{thJC}$$
$$I_{av} = 2\Delta T / [1.3 \cdot BV \cdot Z_{th}]$$
$$E_{AS\ (AR)} = P_{D\ (ave)} \cdot t_{av}$$

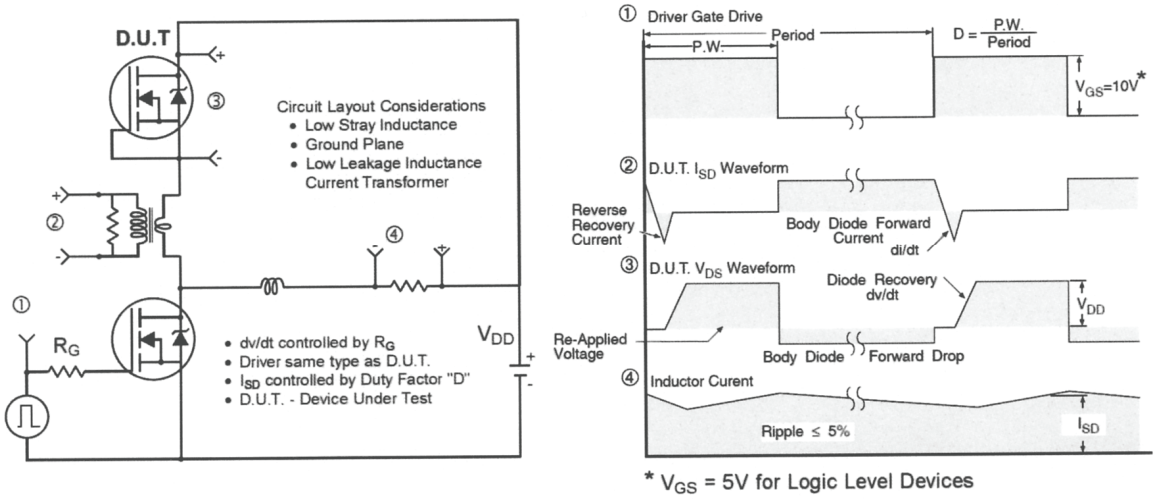



**Fig 17.** Peak Diode Recovery dv/dt Test Circuit for N-Channel HEXFET® Power MOSFETs

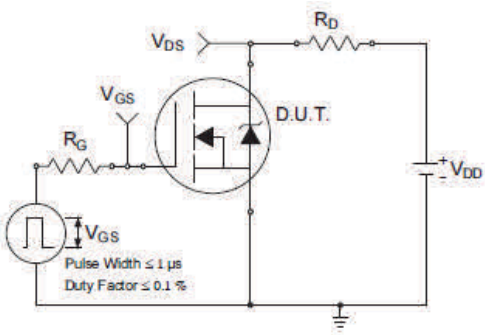



**Fig 18a.** Switching Time Test Circuit

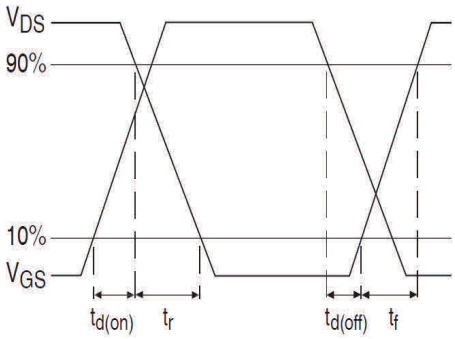
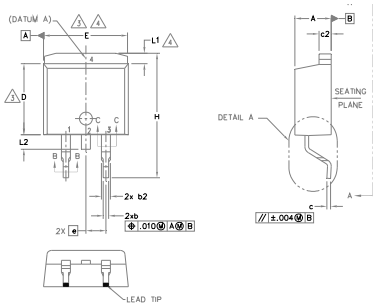


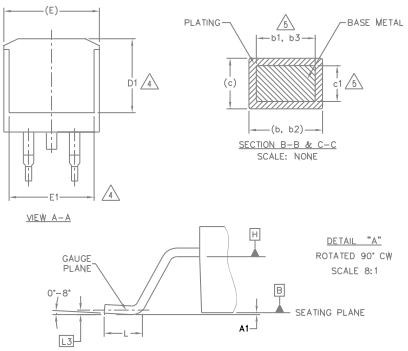

**Fig 18b.** Switching Time Waveforms

## D²Pak (TO-263AB) Package Outline (Dimensions are shown in millimeters (inches))




NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994
2. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
3. DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.127 [.005"] PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTMOST EXTREMES OF THE PLASTIC BODY AT DATUM H.
4. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSION E, L1, D1 & E1.
5. DIMENSION b1, b3 AND c1 APPLY TO BASE METAL ONLY.
6. DATUM A & B TO BE DETERMINED AT DATUM PLANE H.
7. CONTROLLING DIMENSION: INCH.
8. OUTLINE CONFORMS TO JEDEC OUTLINE TO-263AB.




| SYMBOL | DIMENSIONS | | | | NOTES |
|---|---|---|---|---|---|
| | MILLIMETERS | | INCHES | | |
| | MIN. | MAX. | MIN. | MAX. | |
| A | 4.06 | 4.83 | .160 | .190 | |
| A1 | 0.00 | 0.254 | .000 | .010 | |
| b | 0.51 | 0.99 | .020 | .039 | |
| b1 | 0.51 | 0.89 | .020 | .035 | 5 |
| b2 | 1.14 | 1.78 | .045 | .070 | |
| b3 | 1.14 | 1.73 | .045 | .068 | 5 |
| c | 0.38 | 0.74 | .015 | .029 | |
| c1 | 0.38 | 0.58 | .015 | .023 | 5 |
| c2 | 1.14 | 1.65 | .045 | .065 | |
| D | 8.38 | 9.65 | .330 | .380 | 3 |
| D1 | 6.86 | – | .270 | – | 4 |
| E | 9.65 | 10.67 | .380 | .420 | 3,4 |
| E1 | 6.22 | – | .245 | – | 4 |
| e | 2.54 BSC | | .100 BSC | | |
| H | 14.61 | 15.88 | .575 | .625 | |
| L | 1.78 | 2.79 | .070 | .110 | |
| L1 | – | 1.68 | – | .066 | 4 |
| L2 | – | 1.78 | – | .070 | |
| L3 | 0.25 BSC | | .010 BSC | | |

LEAD ASSIGNMENTS

DIODES

1.– ANODE (TWO DIE) / OPEN (ONE DIE)
2, 4.– CATHODE
3.– ANODE

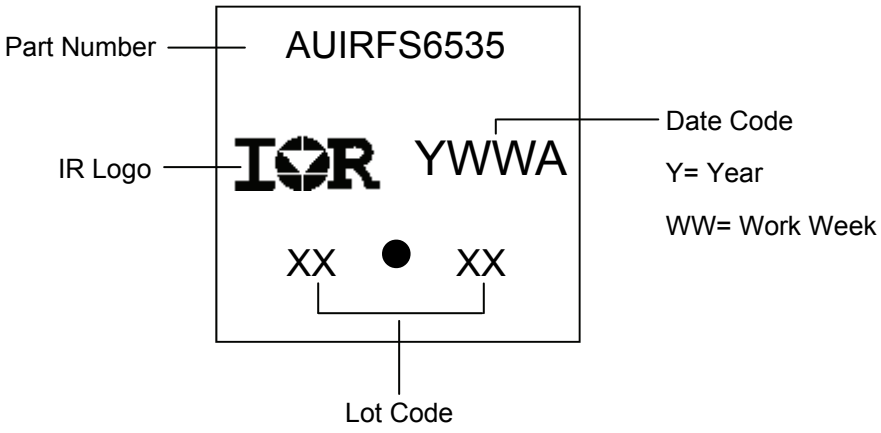
HEXFET

1.– GATE
2, 4.– DRAIN
3.– SOURCE

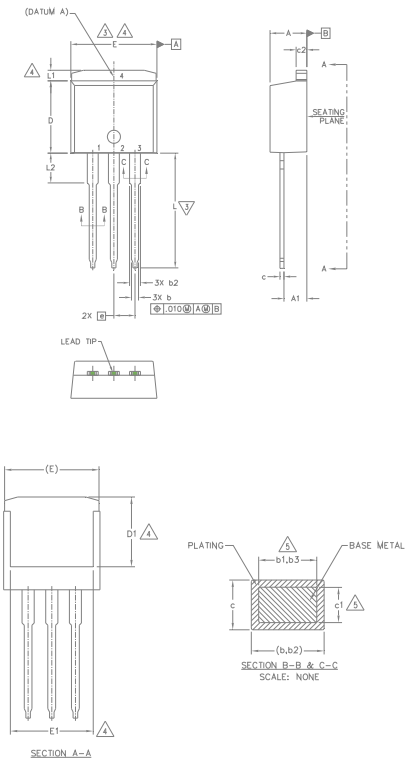
IGBTs, CoPACK

1.– GATE
2, 4.– COLLECTOR
3.– EMITTER

## D²Pak (TO-263AB) Part Marking Information



## TO-262 Package Outline (Dimensions are shown in millimeters (inches)




NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994
2. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
3. DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.127 [.005"] PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTMOST EXTREMES OF THE PLASTIC BODY.
4. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSION E, L1, D1 & E1.
5. DIMENSION b1 AND c1 APPLY TO BASE METAL ONLY.
6. CONTROLLING DIMENSION: INCH.
7. – OUTLINE CONFORM TO JEDEC TO-262 EXCEPT A1(max.), b(min.) AND D1(min.) WHERE DIMENSIONS DERIVED THE ACTUAL PACKAGE OUTLINE.

LEAD ASSIGNMENTS

IGBTs, CoPACK

1.– GATE
2.– COLLECTOR
3.– EMITTER
4.– COLLECTOR

HEXFET

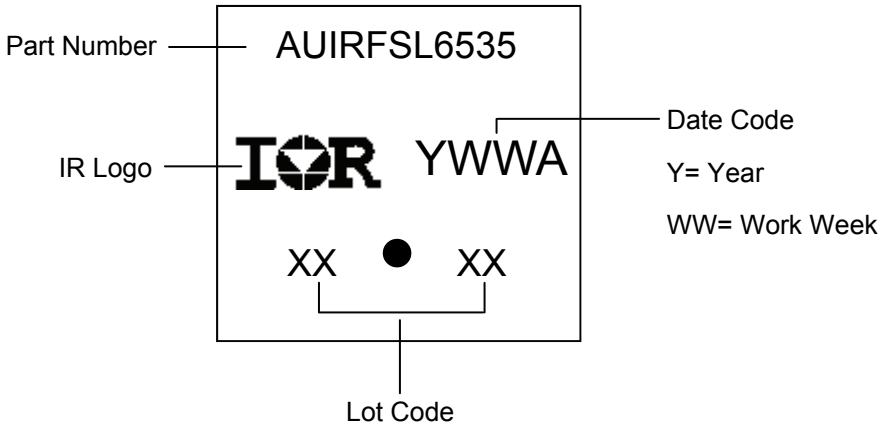
1.– GATE
2.– DRAIN
3.– SOURCE
4.– DRAIN

DIODES

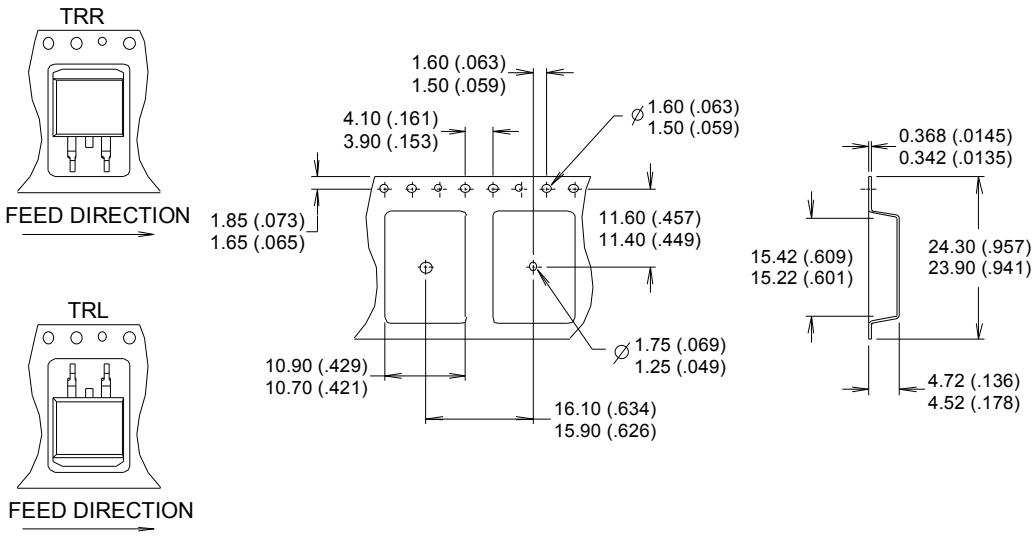
1.– ANODE (TWO DIE) / OPEN (ONE DIE)
2, 4.– CATHODE
3.– ANODE

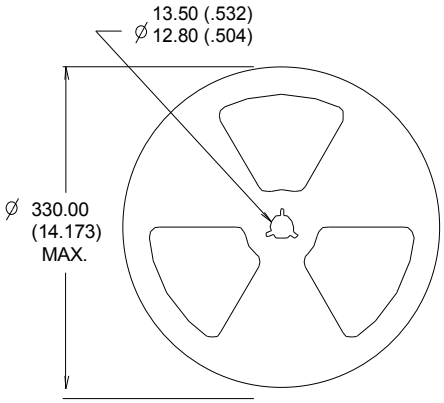
| SYMBOL | DIMENSIONS | | | | NOTES |
|---|---|---|---|---|---|
| | MILLIMETERS | | INCHES | | |
| | MIN. | MAX. | MIN. | MAX. | |
| A | 4.06 | 4.83 | .160 | .190 | |
| A1 | 2.03 | 3.02 | .080 | .119 | |
| b | 0.51 | 0.99 | .020 | .039 | |
| b1 | 0.51 | 0.89 | .020 | .035 | 5 |
| b2 | 1.14 | 1.78 | .045 | .070 | |
| b3 | 1.14 | 1.73 | .045 | .068 | 5 |
| c | 0.38 | 0.74 | .015 | .029 | |
| c1 | 0.38 | 0.58 | .015 | .023 | 5 |
| c2 | 1.14 | 1.65 | .045 | .065 | |
| D | 8.38 | 9.65 | .330 | .380 | 3 |
| D1 | 6.86 | – | .270 | – | 4 |
| E | 9.65 | 10.67 | .380 | .420 | 3,4 |
| E1 | 6.22 | – | .245 | | 4 |
| e | 2.54 BSC | | .100 BSC | | |
| L | 13.46 | 14.10 | .530 | .555 | |
| L1 | – | 1.65 | – | .065 | 4 |
| L2 | 3.56 | 3.71 | .140 | .146 | |

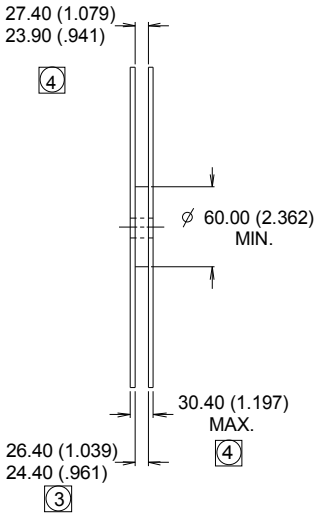
## TO-262 Part Marking Information



**D²Pak (TO-263AB) Tape & Reel Information** (Dimensions are shown in millimeters (inches))




NOTES :
1. COMFORMS TO EIA-418.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION MEASURED @ HUB.
4. INCLUDES FLANGE DISTORTION @ OUTER EDGE.

**Qualification Information**

| | | | |
|---|---|---|---|
| **Qualification Level** | | Automotive (per AEC-Q101) | |
| | | Comments: This part number(s) passed Automotive qualification. Infineon's Industrial and Consumer qualification level is granted by extension of the higher Automotive level. | |
| **Moisture Sensitivity Level** | | TO-262<br>$D^2$-Pak | MSL1 |
| **ESD** | Machine Model | Class M2 (+/-200)† AEC-Q101-002 | |
| | Human Body Model | Class H1B (+/-1000V)† AEC-Q101-001 | |
| | Charged Device Model | Class C5 (+/-2000V)† AEC-Q101-005 | |
| **RoHS Compliant** | | Yes | |

† Highest passing voltage.

**Revision History**

| Date | Comments |
|---|---|
| 12/4/2015 | • Updated datasheet with corporate template<br>• Corrected ordering table on page 1. |
| 8/23/2017 | • Corrected part marking on pages 9,10. |

**Published by**
**Infineon Technologies AG**
**81726 München, Germany**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