

Static Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

Symbol	Parameter	Min.	Тур.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	55			V	$V_{GS} = 0V, I_D = 250\mu A$
$\Delta V_{(BR)DSS}/\Delta T_{J}$	Breakdown Voltage Temp. Coefficient		0.05		V/°C	Reference to 25°C, I _D = 1.0mA
R _{DS(on)} SMD	Static Drain-to-Source On-Resistance		2.0	2.6	mΩ	V _{GS} = 10V, I _D = 140A ③
$V_{GS(th)}$	Gate Threshold Voltage	2.0		4.0	V	$V_{DS} = V_{GS}, I_{D} = 250 \mu A$
gfs	Forward Transconductance	110			S	$V_{DS} = 25V, I_{D} = 140A$
I _{DSS}	Drain-to-Source Leakage Current			20	μA	$V_{DS} = 55V$, $V_{GS} = 0V$
				250		$V_{DS} = 55V, V_{GS} = 0V, T_{J} = 125^{\circ}C$
	Gate-to-Source Forward Leakage Gate-to-Source Reverse Leakage			200	A	V _{GS} = 20V
				-200	nA	V _{GS} = -20V

Symbol	Parameter	Min.	Тур.	Max.	Units	Conditions	
Q_g	Total Gate Charge		130	200		I _D = 140A	
$\overline{Q_gs}$	Gate-to-Source Charge		53		nC	$V_{DS} = 44V$	
Q_{gd}	Gate-to-Drain ("Miller") Charge		49			V _{GS} = 10V ③	
$t_{d(on)}$	Turn-On Delay Time		23			$V_{DD} = 28V$	
t _r	Rise Time		130		no	I _D = 140A	
$t_{d(off)}$	Turn-Off Delay Time		80		ns	$R_G = 2.4\Omega$	
t _f	Fall Time		52			V _{GS} = 10V ③	
1 -	Internal Drain Inductance		4.5			Between lead,	
L _D	Internal Brain inductance		7.5		nH	6mm (0.25in.)	
	Internal Source Inductance		7.5	5	11111	from package	
L _S	Internal Source inductance		7.5			and center of die contact	
C _{iss}	Input Capacitance		7820			$V_{GS} = 0V$	
Coss	Output Capacitance		1260			V _{DS} = 25V	
C _{rss}	Reverse Transfer Capacitance		610		pF	f = 1.0 MHz, See Fig. 5	
Coss	Output Capacitance		4310			$V_{GS} = 0V, V_{DS} = 1.0V, f = 1.0MHz$	
Coss	Output Capacitance		980			$V_{GS} = 0V, V_{DS} = 44V, f = 1.0MHz$	
C _{oss} eff.	Effective Output Capacitance ④		1540			$V_{GS} = 0V$, $V_{DS} = 0V$ to 44V	

Diode Characteristics

Symbol	Parameter	Min.	Тур.	Max.	Units	Conditions	
	Continuous Source Current			240		MOSFET symbol	
Is	(Body Diode)			240	_	showing the	
	Pulsed Source Current	1000	Α	integral reverse			
I _{SM}	(Body Diode) ②			1000		p-n junction diode.	
V_{SD}	Diode Forward Voltage			1.3	V	$T_J = 25^{\circ}C$, $I_S = 140A$, $V_{GS} = 0V$ ③	
t _{rr}	Reverse Recovery Time		45	68	ns	$T_J = 25$ °C, $I_F = 140$ A, $V_{DD} = 28$ V	
Q_{rr}	Reverse Recovery Charge		35	53	nC	di/dt = 100A/µs ③	
t _{on}	Forward Turn-On Time	Intrir	Intrinsic turn-on time is negligible (turn-on is dominated by L _S +L _D)				

Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature. (See fig. 11).
- ② This value determined from sample failure population starting $T_J = 25$ °C, L=0.043mH, $R_G = 25\Omega$, $I_{AS} = 140A$, $V_{GS} = 10V$.
- Coss eff. is a fixed capacitance that gives the same charging time as Coss while V_{DS} is rising from $\,$ 0 to 80% V_{DSS}.
- ⑤ This is applied to D²Pak, when mounted on 1" square PCB (FR-4 or G-10 Material). For recommended footprint and soldering techniques refer to application note #AN-994.
- © R_{θ} is measured at T_{J} of approximately 90°C.
- Solder mounted on IMS substrate.
- Limited by T_{Jmax} starting $T_J = 25$ °C, L=0.043mH, R_G = 25 Ω , I_{AS} = 140A, V_{GS} =10V.Part not recommended for use above this value.

2017-10-09



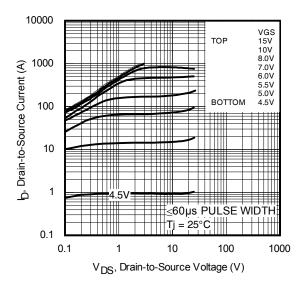


Fig. 1 Typical Output Characteristics

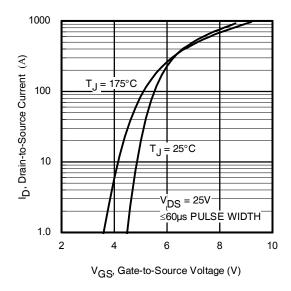


Fig. 3 Typical Transfer Characteristics

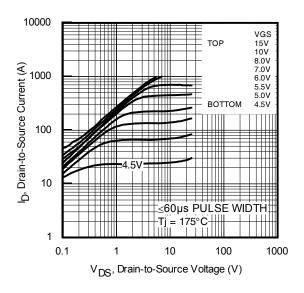


Fig. 2 Typical Output Characteristics

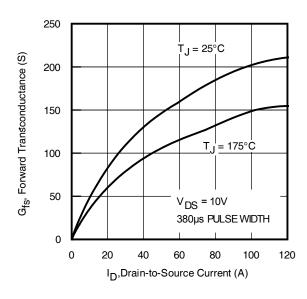


Fig. 4 Typical Forward Transconductance vs. Drain Current



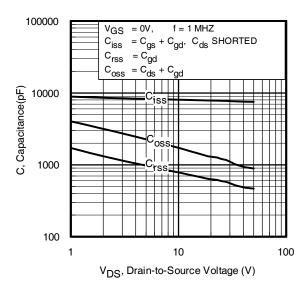


Fig 5. Typical Capacitance vs. Drain-to-Source Voltage

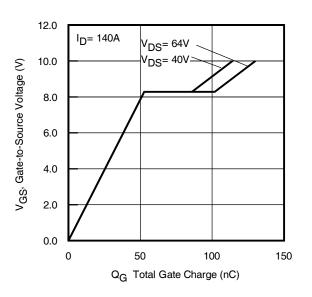


Fig 6. Typical Gate Charge vs. Gate-to-Source Voltage

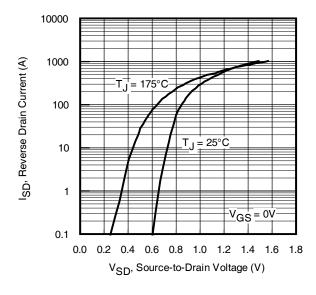


Fig. 7 Typical Source-to-Drain Diode Forward Voltage

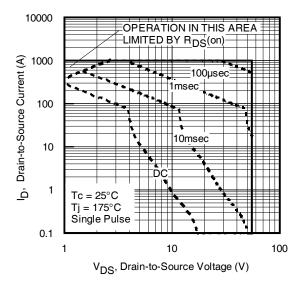


Fig 8. Maximum Safe Operating Area



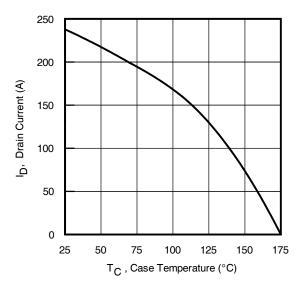


Fig 9. Maximum Drain Current vs. Case Temperature

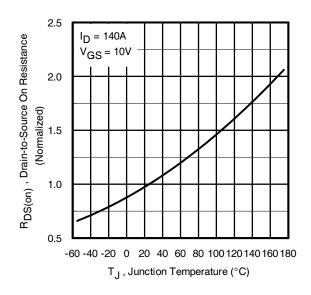


Fig 10. Normalized On-Resistance vs. Temperature

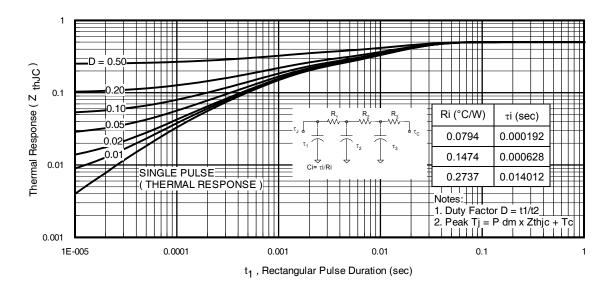


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case



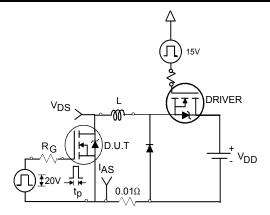


Fig 12a. Unclamped Inductive Test Circuit

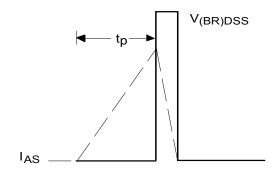


Fig 12b. Unclamped Inductive Waveforms

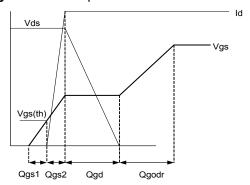


Fig 13a. Basic Gate Charge Waveform

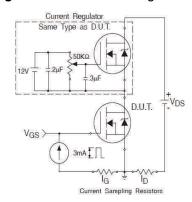


Fig 13b. Gate Charge Test Circuit

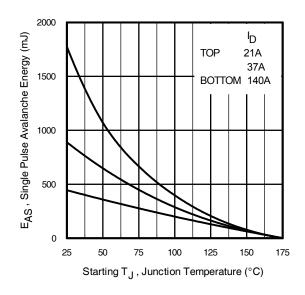


Fig 12c. Maximum Avalanche Energy

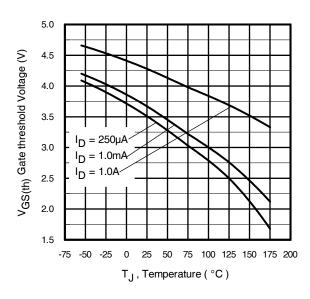


Fig 14. Threshold Voltage vs. Temperature



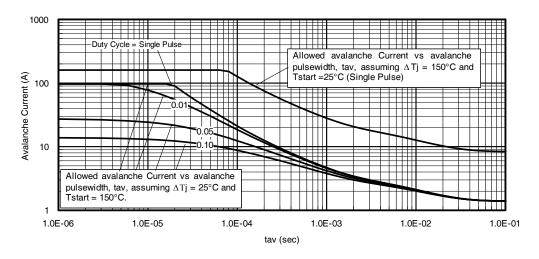


Fig 15. Typical Avalanche Current vs. Pulse width

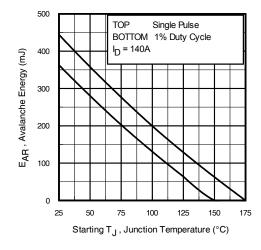


Fig 16. Maximum Avalanche Energy vs. Temperature

Notes on Repetitive Avalanche Curves, Figures 15, 16: (For further info, see AN-1005 at www.irf.com)

- Avalanche failures assumption:
- Purely a thermal phenomenon and failure occurs at a temperature far in excess of T_{jmax}. This is validated for every part type.
- Safe operation in Avalanche is allowed as long as T_{jmax} is not exceeded.
- Equation below based on circuit and waveforms shown in Figures 12a, 12b.
- PD (ave) = Average power dissipation per single avalanche pulse.
- BV = Rated breakdown voltage (1.3 factor accounts for voltage increase during avalanche).
- 6. lav = Allowable avalanche current.
- 7. ΔT = Allowable rise in junction temperature, not to exceed T_{jmax} (assumed as 25°C in Figure 15, 16).

tav = Average time in avalanche.

D = Duty cycle in avalanche = tav ·f

ZthJC(D, tav) = Transient thermal resistance, see Figures 11)

 $P_{D \text{ (ave)}} = 1/2 \text{ (} 1.3 \cdot \text{BV} \cdot \text{I}_{av} \text{)} = \Delta \text{T/ } Z_{\text{thJC}}$ $I_{av} = 2\Delta T / [1.3 \cdot BV \cdot Z_{th}]$ $E_{AS (AR)} = P_{D (ave)} \cdot t_{av}$

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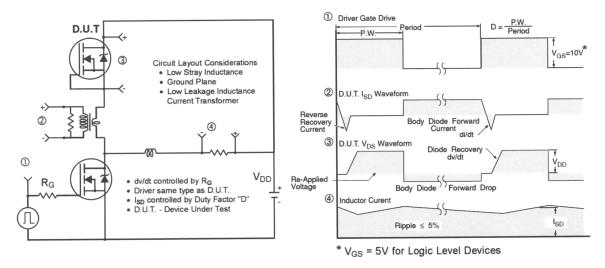


Fig 17. Peak Diode Recovery dv/dt Test Circuit for N-Channel HEXFET® Power MOSFETs

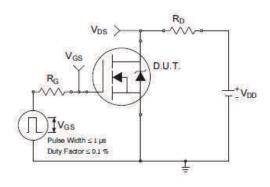


Fig 18a. Switching Time Test Circuit

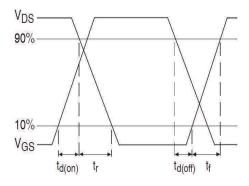
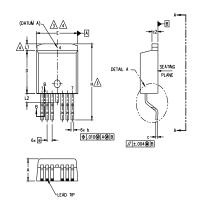


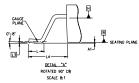
Fig 18b. Switching Time Waveforms

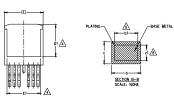


D²Pak - 7 Pin Package Outline

Dimensions are shown in millimeters (inches)





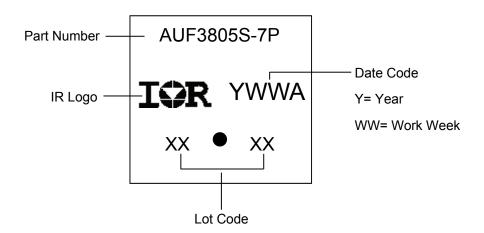


S Y M B O L	DIMENSIONS					
B	MILLIM	ETERS	INC	NOTES		
L	MIN.	MAX.	MIN.	MAX.	S	
Α	4.06	4.83	.160	.190		
A1	_	0.254	_	.010		
ь	0.51	0.99	.020	.036		
ь1	0.51	0.89	.020	.032	5	
С	0.38	0.74	.015	.029		
c1	0.38	0.58	.015	.023	5	
c2	1.14	1.65	.045	.065		
D	8.38	9.65	.330	.380	3	
D1	6.86	_	.270		4	
E	9.65	10.67	.380	.420	3,4	
E1	6.22	_	.245		4	
е	1.27	BSC	.050	BSC		
Н	14.61	15.88	.575	.625		
L	1.78	2.79	.070	.110		
∟1	_	1.68	_	.066	4	
L2	_	1.78	_	.070		
L3	0.25	BSC	.010	.010 BSC		
L4	4.78	5.28	.188	.208		

NOTES:

- 1. DIMENSIONING AND TOLERANCING AS PER ASME Y14.5M-1994
- 2. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
- 3. DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.127 [.005"] PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTMOST EXTREMES OF THE PLASTIC BODY AT DATUM H.
- THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSION E, L1, D1 & E1.
- 5. DIMENSION 61 AND c1 APPLY TO BASE METAL ONLY.
- 6. DATUM A & B TO BE DETERMINED AT DATUM PLANE H.
- 7. CONTROLLING DIMENSION: INCH.
- 8. OUTLINE CONFORMS TO JEDEC OUTLINE TO-263CB.

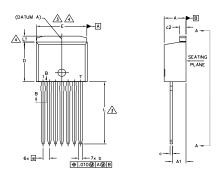
D²Pak - 7 Pin Part Marking Information





TO-263CA - 7 Pin Long Leads Package Outline

Dimensions are shown in millimeters (inches)





- 1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994
- 2. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].

3. DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.127 [.005"] PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTMOST EXTREMES OF THE PLASTIC BODY.

4. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSION E, L1, D1 & E1.

5. DIMENSION 61 AND c1 APPLY TO BASE METAL ONLY.

- 6. CONTROLLING DIMENSION: INCH.
- 7.- OUTLINE CONFORM TO JEDEC TO-263 CA

(E)	PLATING BASE METAL C C SECTION B-B SCALE: NONE
E1 A	

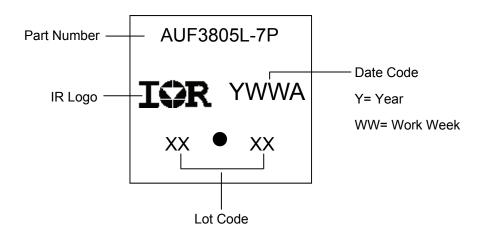
S Y M	DIMENSIONS				
В	MILLIM	ETERS	INC	N O T E S	
O L	MIN.	MAX.	MIN.	MAX.	S
Α	4.06	4.83	.160	.190	
A1	2.03	3.02	.080	.119	
Ь	0.51	0.91	.020	.036	
b1	0.51	0.81	.020	.032	5
С	0.38	0.74	.015	.029	
c1	0.38	0.58	.015	.023	5
c2	1.14	1.65	.045	.065	
D	8.51	9.65	.335	.380	3
D1	6.86	-	.270	_	4
E	9.65	10.67	.380	.420	3,4
E1	6.22	_	.245		4
е	1.27	BSC	.050	BSC	
L	13.46	14.10	.530	.555	
L1	_	1.65	_	.065	4
L2	_	6.35	_	.250	

LEAD ASSIGNMENTS

HEXFET

- 1.- GATE
- 2.- SOURCE
- 3.- SOURCE 4.- DRAIN
- 4. DRAIN 5. - SOURCE
- 6.- SOURCE
- 7.- SOURCE

TO-263CA - 7 Pin Part Marking Information

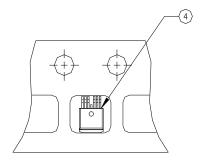




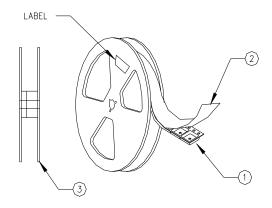
D2Pak - 7 Pin Tape and Reel

NOTES, TAPE & REEL, LABELLING:

- 1. TAPE AND REEL.
 - 1.1 REEL SIZE 13 INCH DIAMETER.
 - 1.2 EACH REEL CONTAINING 800 DEVICES.
 - 1.3 THERE SHALL BE A MINIMUM OF 42 SEALED POCKETS CONTAINED IN THE LEADER AND A MINIMUM OF 15 SEALED POCKETS IN THE TRAILER.
 - 1.4 PEEL STRENGTH MUST CONFORM TO THE SPEC. NO. 71-9667.
 - 1.5 PART ORIENTATION SHALL BE AS SHOWN BELOW.
 - 1.6 REEL MAY CONTAIN A MAXIMUM OF TWO UNIQUE LOT CODE/DATE CODE COMBINATIONS.
 REWORKED REELS MAY CONTAIN A MAXIMUM OF THREE UNIQUE LOT CODE/DATE CODE COMBINATIONS.
 HOWEVER, THE LOT CODES AND DATE CODES WITH THEIR RESPECTIVE QUANTITIES SHALL APPEAR ON THE BAR CODE LABEL FOR THE AFFECTED REEL.



- 2. LABELLING (REEL AND SHIPPING BAG).
 - 2.1 CUST. PART NUMBER (BAR CODE): IRFXXXXSTRL-7P
 - 2.2 CUST. PART NUMBER (TEXT CODE): IRFXXXXSTRL-7P
 - 2.3 I.R. PART NUMBER: IRFXXXXSTRL-7P
 - 2.4 QUANTITY:
 - 2.5 VENDOR CODE: IR
 - 2.6 LOT CODE:
 - 2.7 DATE CODE:





Qualification Information

		Automotive				
		(per AEC-Q101)				
		Comments: This part number(s) passed Automotive qualification. IR's Industrial and Consumer qualification level is granted by extension of the higher Automotive level.				
		D ² PAK 7 Pin	MSL1, 260°C			
	Machine Model	Class M4(+/-425V) [†]				
		(Per AEC-Q101-002)				
FOD	Human Body Model	Class H3A(+/-4000V) [†]				
ESD		(per AEC-Q101-001)				
	Charged Device Model	Class C5 (+/-1000V) [†]				
		(per AEC-Q101-005)				
RoHS Compliant			Yes			

† Highest passing voltage.

Revision History

Date	Comments		
09/02/2015	Updated data sheet with corporate template.Corrected ordering table on page1.		
09/30/2015	Updated "Infineon" logo all pages.Updated disclaimer on last page		
10/09/2017	Corrected typo error on part marking on page 9,10.		

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