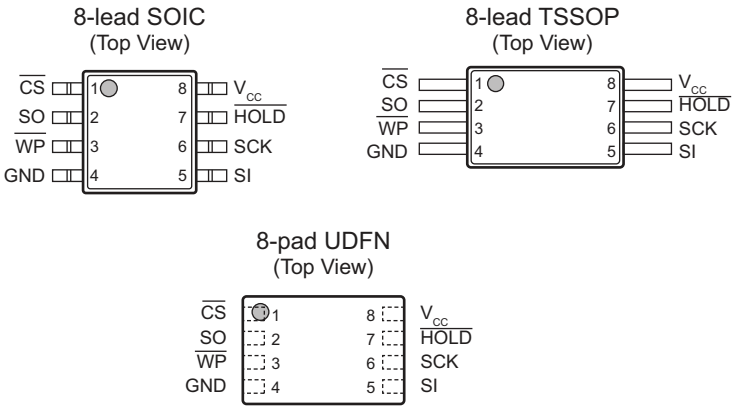
# Table of Contents

# 1. Pin Descriptions and Pinouts

**Figure 1. Pin Configurations**

| Pin Name | Function |
|---|---|
| $\overline{CS}$ | Chip Select |
| SCK | Serial Data Clock |
| SI | Serial Data Input |
| SO | Serial Data Output |
| GND | Ground |
| $V_{CC}$ | Power Supply |
| $\overline{WP}$ | Write Protect |
| $\overline{HOLD}$ | Suspends Serial Input |




Note: Drawings are not to scale.

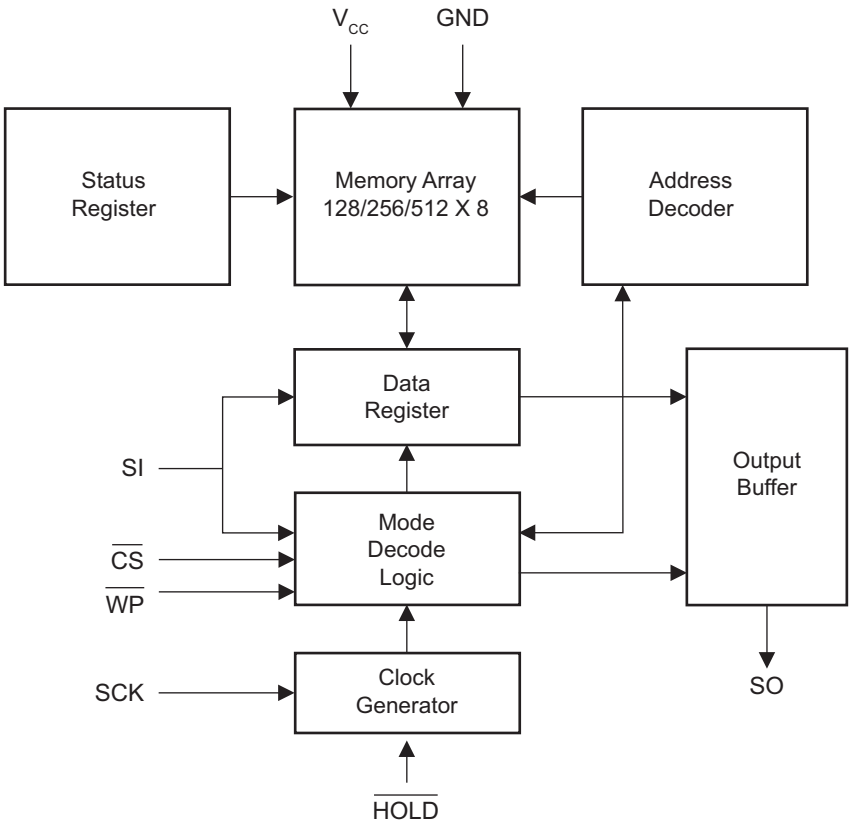
# 2. Absolute Maximum Ratings*

| | |
|---|---|
| Operating Temperature | -40°C to +125°C |
| Storage Temperature | -65°C to +150°C |
| Voltage on any pin with respect to ground | -1.0V to +7.0V |
| Maximum Operating Voltage | 6.25V |
| DC Output Current | 5.0mA |

*Notice: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

# 3. Block Diagram

**Figure 3-1. Block Diagram**



# 4. Serial Interface Description

**Master:** The device that generates the serial clock.

**Slave:** Because the Serial Clock pin (SCK) is always an input, AT25010B/020B/040B always operates as a slave.

**Transmitter/Receiver:** AT25010B/020B/040B has separate pins designated for data transmission (SO) and reception (SI).

**MSB:** The Most Significant Bit (MSB) is the first bit transmitted and received.

**Serial Opcode:** After the device is selected with $\overline{CS}$ going low, the first byte will be received. This byte contains the opcode that defines the operations to be performed. The opcode also contains address bit A8 in both the Read and the Write instructions for AT25040B only.

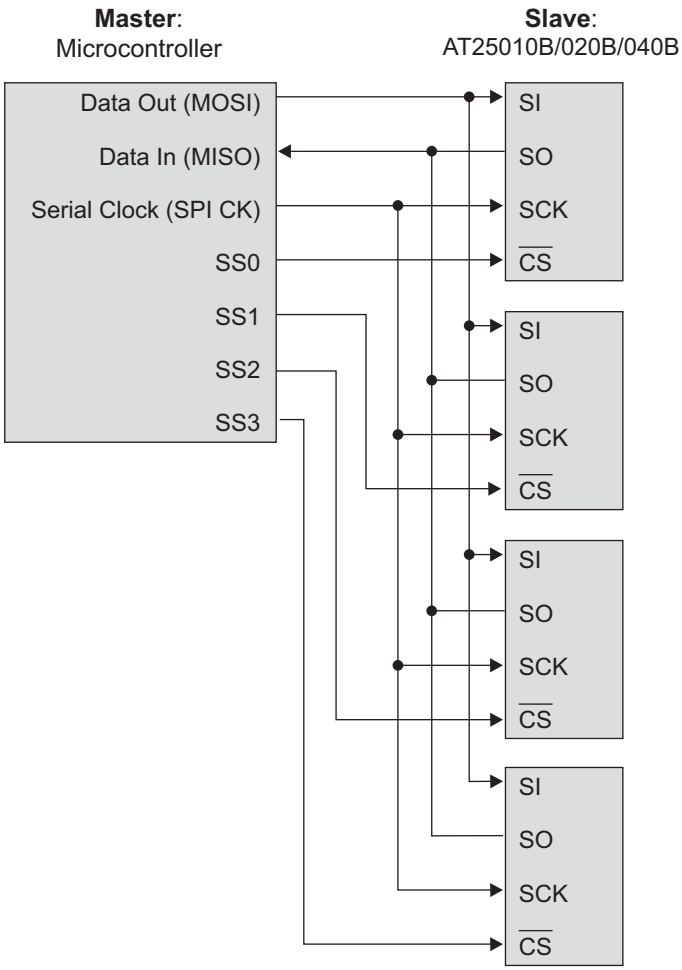
**Invalid Opcode:** If an invalid opcode is received, no data will be shifted into AT25010B/020B/040B, and the Serial Output pin (SO) will remain in a high impedance state until the falling edge of $\overline{CS}$ is detected again. This will reinitialize the serial communication.

**Chip Select:** AT25010B/020B/040B is selected when the $\overline{CS}$ pin is low. When the device is not selected, data will not be accepted via the SI pin, and the Serial Output pin (SO) will remain in a high impedance state.

**Hold:** The $\overline{HOLD}$ pin is used in conjunction with the $\overline{CS}$ pin to select AT25010B/020B/040B. When the device is selected and a serial sequence is underway, Hold can be used to pause the serial communication with the master device without resetting the serial sequence. To pause, the $\overline{HOLD}$ pin must be brought low while the SCK pin is low. To resume serial communication, the $\overline{HOLD}$ pin is brought high while the SCK pin is low (SCK may still toggle during Hold). Inputs to the SI pin will be ignored while the SO pin is in the high impedance state.

**Write Protect:** The Write Protect pin ($\overline{WP}$) will allow normal read/write operations when held high. When the $\overline{WP}$ pin is brought low, all write operations are inhibited. $\overline{WP}$ going low while $\overline{CS}$ is still low will interrupt a write to AT25010B/020B/040B. If the internal write cycle has already been initiated, $\overline{WP}$ going low will have no effect on any write operation.

**Figure 4-1. SPI Serial Interface**



# 5. Electrical Characteristics

## 5.1 Pin Capacitance

**Table 5-1. Pin Capacitance[1]**

Applicable at these conditions, unless otherwise noted. $T_A$ = 25°C, f = 1.0MHz, $V_{CC}$ = +5.0V.

| Symbol | Test Conditions | Max | Units | Conditions |
|---|---|---|---|---|
| $C_{OUT}$ | Output Capacitance (SO) | 8 | pF | $V_{OUT}$ = 0V |
| $C_{IN}$ | Input Capacitance ($\overline{CS}$, SCK, SI, $\overline{WP}$, $\overline{HOLD}$) | 6 | pF | $V_{IN}$ = 0V |

Note: 1. This parameter is characterized and is not 100% tested.

## 5.2 DC Characteristics

**Table 5-2. DC Characteristics**

Applicable over recommended operating range from: $T_{A1}$ = -40°C to +125°C, $V_{CC1}$ = 2.5V to 5.5V; $T_{A2}$ = -40°C to 105°C, $V_{CC2}$ = 1.7V to 5.5V.

| Symbol | Parameter | Test Condition | | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|---|
| $V_{CC1}$ | Supply Voltage | Grade 1 | | 2.5 | | 5.5 | V |
| $V_{CC2}$ | | Grade 2[2] and 3 | | 1.7 | | 5.5 | |
| $I_{CC1}$ | Supply Current | $V_{CC}$ = 5.0V at 5MHz, SO = Open, Read | | | | 6.0 | mA |
| $I_{CC2}$ | | $V_{CC}$ = 5.0V at 1MHz | | | | 3.0 | |
| $I_{CC3}$ | | $V_{CC}$ = 5.0V at 5MHz, SO = Open, Read, Write | | | | 6.0 | |
| $I_{SB1}$ | Standby Current | $V_{CC}$ = 1.7V, $\overline{CS}$ = $V_{CC}$ | | | 0.1 | 2.0 | µA |
| $I_{SB2}$ | | $V_{CC}$ = 2.5V, $\overline{CS}$ = $V_{CC}$ | | | 0.2 | 3.0 | |
| $I_{SB3}$ | | $V_{CC}$ = 5.0V, $\overline{CS}$ = $V_{CC}$ | | | 2.0 | 5.0 | |
| $I_{IL}$ | Input Leakage | $V_{IN}$ = 0V to $V_{CC}$ | | -3.0 | | | µA |
| $I_{OL}$ | Output Leakage | $V_{IN}$ = 0V to $V_{CC}$ | | -3.0 | | 3.0 | |
| $V_{IL}$[1] | Input Low-voltage | | | -0.6 | | $V_{CC}$ x 0.3 | V |
| $V_{IH}$[1] | Input High-voltage | | | $V_{CC}$ x 0.7 | | $V_{CC}$ + 0.5 | |
| $V_{OL1}$ | Output Low-voltage | 2.5V ≤ $V_{CC}$ ≤ 5.5V | $I_{OL}$ = 3.0mA | | | 0.4 | V |
| $V_{OH1}$ | Output High-voltage | | $I_{OH}$ = –1.6mA | $V_{CC}$ – 0.8 | | | |
| $V_{OL2}$ | Output Low-voltage | 1.7V ≤ $V_{CC}$ ≤ 5.5V | $I_{OL}$ = 0.15mA | | | 0.2 | V |
| $V_{OH2}$ | Output High-voltage | | $I_{OH}$ = -100µA | $V_{CC}$ – 0.2 | | | |

Notes: 1. $V_{IL}$ min and $V_{IH}$ max are reference only and are not tested.
2. Contact Sales for Grade 2 Availability

## 5.3 AC Characteristics

**Table 5-3. AC Characteristics**

Applicable over recommended operating range from $T_A$ = -40°C to +125°C, $V_{CC}$ = As Specified, CL = 1 TTL Gate and 100pF (unless otherwise noted).

| Symbol | Parameter | Voltage | Min | Max | Units |
|---|---|---|---|---|---|
| $f_{SCK}$ | SCK Clock Frequency | 1.7 to 5.5 | 0 | 5.0 | MHz |
| $t_{RI}$ | Input Rise Time | 1.7 to 5.5 | | 2 | µs |
| $t_{FI}$ | Input Fall Time | 1.7 to 5.5 | | 2 | µs |
| $t_{WH}$ | SCK High Time | 1.7 to 5.5 | 40 | | ns |
| $t_{WL}$ | SCK Low Time | 1.7 to 5.5 | 40 | | ns |
| $t_{CS}$ | $\overline{CS}$ High Time | 1.7 to 5.5 | 80 | | ns |
| $t_{CSS}$ | $\overline{CS}$ Setup Time | 1.7 to 5.5 | 80 | | ns |
| $t_{CSH}$ | $\overline{CS}$ Hold Time | 1.7 to 5.5 | 80 | | ns |
| $t_{SU}$ | Data In Setup Time | 1.7 to 5.5 | 5 | | ns |
| $t_H$ | Data In Hold Time | 1.7 to 5.5 | 20 | | ns |
| $t_{HD}$ | $\overline{Hold}$ Setup Time | 1.7 to 5.5 | 40 | | ns |
| $t_{CD}$ | $\overline{Hold}$ Time | 1.7 to 5.5 | 40 | | ns |
| $t_V$ | Output Valid | 1.7 to 5.5 | 0 | 40 | ns |
| $t_{HO}$ | Output Hold Time | 1.7 to 5.5 | 0 | | ns |
| $t_{LZ}$ | $\overline{Hold}$ to Output Low Z | 1.7 to 5.5 | 0 | 40 | ns |
| $t_{HZ}$ | $\overline{Hold}$ to Output High Z | 1.7 to 5.5 | | 80 | ns |
| $t_{DIS}$ | Output Disable Time | 1.7 to 5.5 | | 80 | ns |
| $t_{WC}$ | Write Cycle Time | 1.7 to 5.5 | | 5 | ms |
| Endurance(1) | 5.0V, 25°C, Page Mode | | 1,000,000 | | Write Cycles |

Note: 1. This parameter is characterized and is not 100% tested.

# 6. Functional Description

AT25010B/020B/040B is designed to interface directly with the synchronous Serial Peripheral Interface (SPI) of the 6805 and 68HC11 series of microcontrollers.

AT25010B/020B/040B utilizes an 8-bit instruction register. The list of instructions and their operation codes are contained in Table 6-1. All instructions, addresses, and data are transferred with the MSB first and start with a high-to-low CS transition.

**Table 6-1. Instruction Set for the Atmel AT25010B/020B/040B**

| Instruction Name | Instruction Format | Operation |
|---|---|---|
| WREN | 0000 X110 | Set Write Enable Latch |
| WRDI | 0000 X100 | Reset Write Enable Latch |
| RDSR | 0000 X101 | Read Status Register |
| WRSR | 0000 X001 | Write Status Register |
| READ | 0000 A011 | Read Data from Memory Array |
| WRITE | 0000 A010 | Write Data to Memory Array |

Note: "A" represents the ninth address bit (MSB bit A8) needed for AT25040B only.

**Write Enable (WREN):** The device will power up in the Write Disable state when $V_{CC}$ is applied. All programming instructions must therefore be preceded by a Write Enable instruction.

**Write Disable (WRDI):** To protect the device against inadvertent writes, the Write Disable instruction disables all programming modes. The WRDI instruction is independent of the status of the $\overline{WP}$ pin.

**Read Status Register (RDSR):** The Read Status Register instruction provides access to the status register. The Ready/Busy and Write Enable status of the device can be determined by the RDSR instruction. Similarly, the Block Write protection bits indicate the extent of protection employed. These bits are set by using the WRSR instruction.

**Table 6-2. Status Register Format**

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|
| X | X | X | X | BP1 | BP0 | WEN | $\overline{RDY}$ |

**Table 6-3. Read Status Register Bit Definition**

| Bit | Definition |
|---|---|
| Bit 0 ($\overline{RDY}$) | Bit 0 = 0 ($\overline{RDY}$) indicates the device is ready.<br>Bit 0 = 1 indicates the write cycle is in progress. |
| Bit 1 (WEN) | Bit 1 = 0 indicates the device is not write-enabled.<br>Bit 1 = 1 indicates the device is write-enabled. |
| Bit 2 (BP0) | See Table 6-4 on page 10. |
| Bit 3 (BP1) | See Table 6-4 on page 10. |
| Bits 4 -7 | Bits 4 – 7 = 0 when the device is not in an internal write cycle.<br>Bits 4 – 7 = 1 during an internal write cycle. |

**Write Status Register (WRSR):** The WRSR instruction allows the user to select one of four levels of protection. AT25010B/020B/040B is divided into four array segments. One-quarter, one-half, or all of the memory segments can be protected. Any of the data within any selected segment will therefore be read-only. The Block Write protection levels and corresponding status register control bits are shown in Table 6-4.

Bits BP0 and BP1 are nonvolatile cells that have the same properties and functions as the regular memory cells (e.g., WREN, $t_{WC}$, RDSR).

**Table 6-4. Block Write Protect Bits**

| Level | Status Register Bits | | Array Addresses Protected | | |
|---|---|---|---|---|---|
| | BP1 | BP0 | AT25010B | AT25020B | AT25040B |
| 0 | 0 | 0 | None | None | None |
| 1 (1/4) | 0 | 1 | 60 - 7F | C0 - FF | 180 - 1FF |
| 2 (1/2) | 1 | 0 | 40 - 7F | 80 - FF | 100 - 1FF |
| 3 (All) | 1 | 1 | 00 - 7F | 00 - FF | 000 - 1FF |

**Read Sequence (Read):** Reading AT25010B/020B/040B via the Serial Output (SO) pin requires the following sequence. After the $\overline{CS}$ line is pulled low to select a device, the Read opcode is transmitted via the SI line followed by the byte address to be read (A7–A0, see Table 6-5). Upon completion, any data on the SI line will be ignored. The data (D7–D0) at the specified address is then shifted out onto the SO line. If only one byte is to be read, the $\overline{CS}$ line should be driven high after the data comes out. The Read sequence can be continued since the byte address is automatically incremented and data will continue to be shifted out. When the highest address is reached, the address counter will roll over to the lowest address, allowing the entire memory to be read in one continuous Read cycle.

**Write Sequence (Write):** In order to program AT25010B/020B/040B, two separate instructions must be executed. First, the device ***must be Write Enabled*** via the WREN instruction. Then a Write instruction may be executed. Also, the address of the memory location(s) to be programmed must be outside the protected address field location selected by the Block Write protection level. During an internal write cycle, all commands will be ignored except the RDSR instruction.

A Write instruction requires the following sequence. After the $\overline{CS}$ line is pulled low to select the device, the Write opcode is transmitted via the SI line followed by the byte address (A7–A0) and the data (D7–D0) to be programmed (See Table 6-5). Programming will start after the $\overline{CS}$ pin is brought high. The low-to-high transition of the $\overline{CS}$ pin must occur during the SCK low-time immediately after clocking in the D0 (LSB) data bit.

The Ready/Busy status of the device can be determined by initiating a Read status register (RDSR) instruction. If Bit 0 = one, the Write cycle is still in progress. If Bit 0 = zero, the Write cycle has ended. Only the RDSR instruction is enabled during the Write programming cycle.

AT25010B/020B/040B is capable of a 8-byte Page Write operation. After each byte of data is received, the three low-order address bits are internally incremented by one; the high-order bits of the address will remain constant. If more than eight bytes of data are transmitted, the address counter will roll over and the previously written data will be overwritten. AT25010B/020B/040B is automatically returned to the Write Disable state at the completion of a Write cycle.

Note: If the device is not Write Enabled (WREN), the device will ignore the Write instruction and will return to the standby state, when $\overline{CS}$ is brought high. A new $\overline{CS}$ falling edge is required to reinitiate the serial communication.

**Table 6-5. Address Key**

| Address | AT25010B | AT25020B | AT25040B |
|---|---|---|---|
| $A_N$ | $A_6$–$A_0$ | $A_7$–$A_0$ | $A_8$–$A_0$ |
| Don't Care Bits | $A_7$ | None | None |

Note: The $A_8$ bit (AT25040B address MSB) must appear embedded in the opcode as illustrated in Table 6-1.

# 7. Timing Diagrams

**Figure 7-1. Synchronous Data Timing (for Mode 0)**

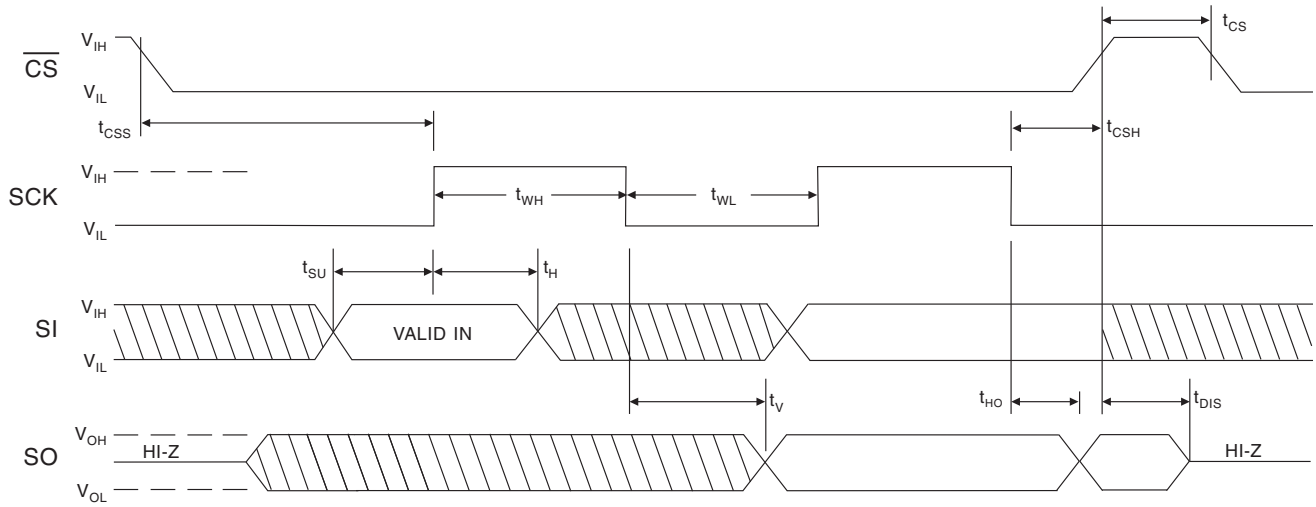



**Figure 7-2. WREN Timing**

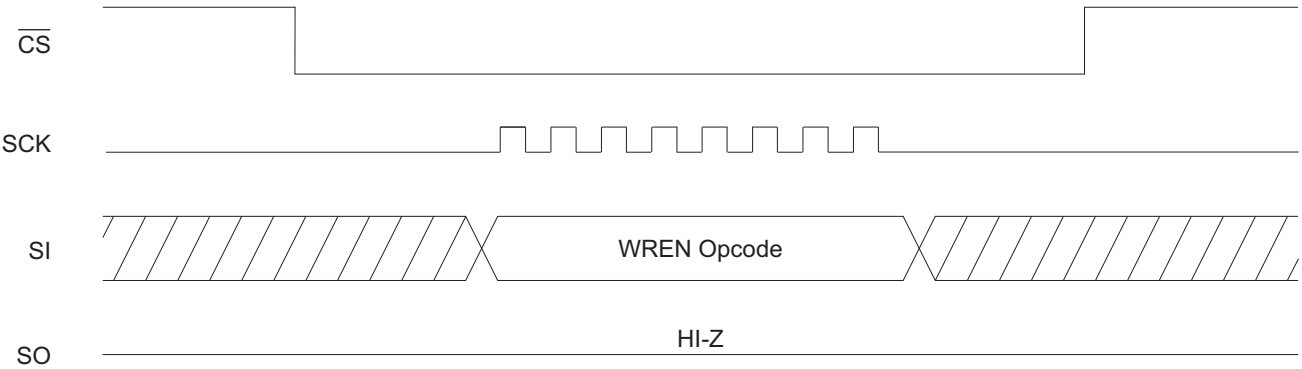



**Figure 7-3. WRDI Timing**

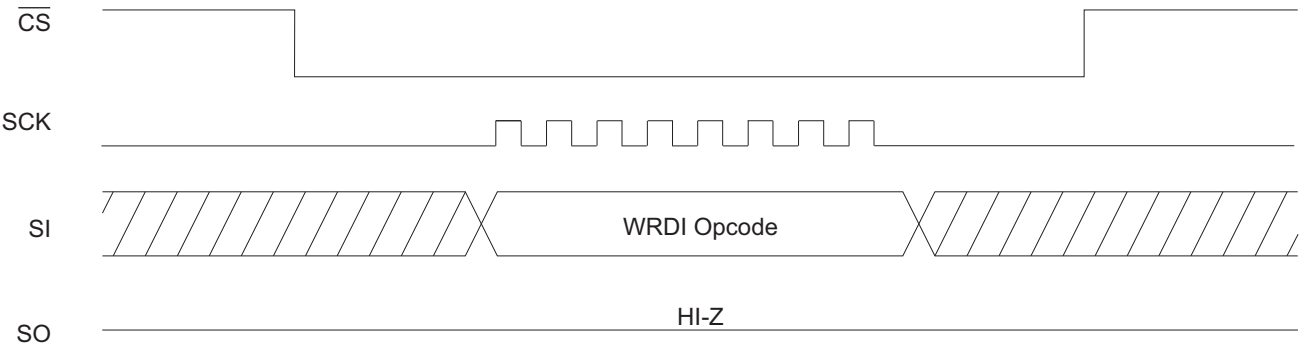


**Figure 7-4. RDSR Timing**

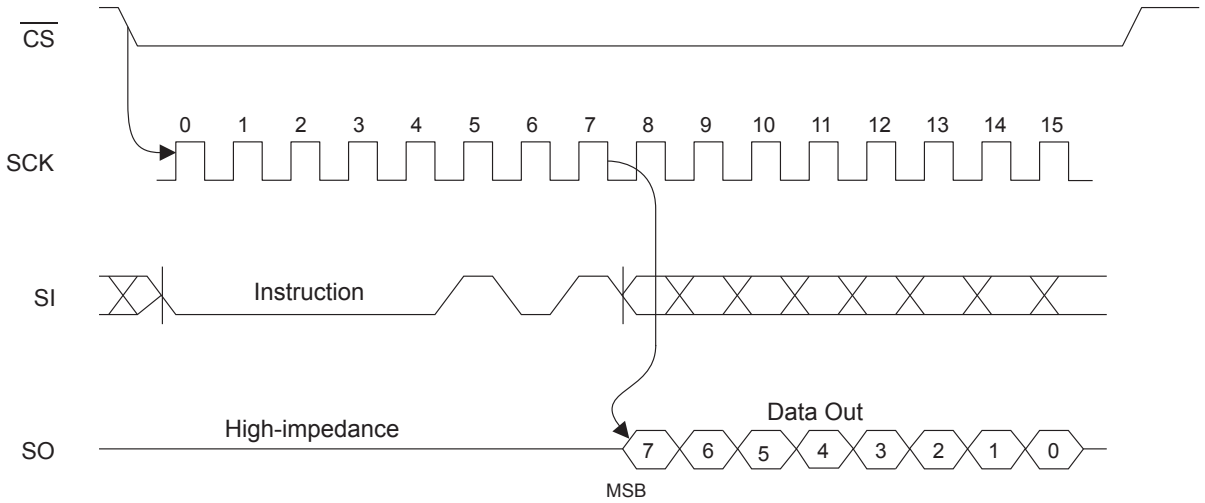



**Figure 7-5. WRSR Timing**

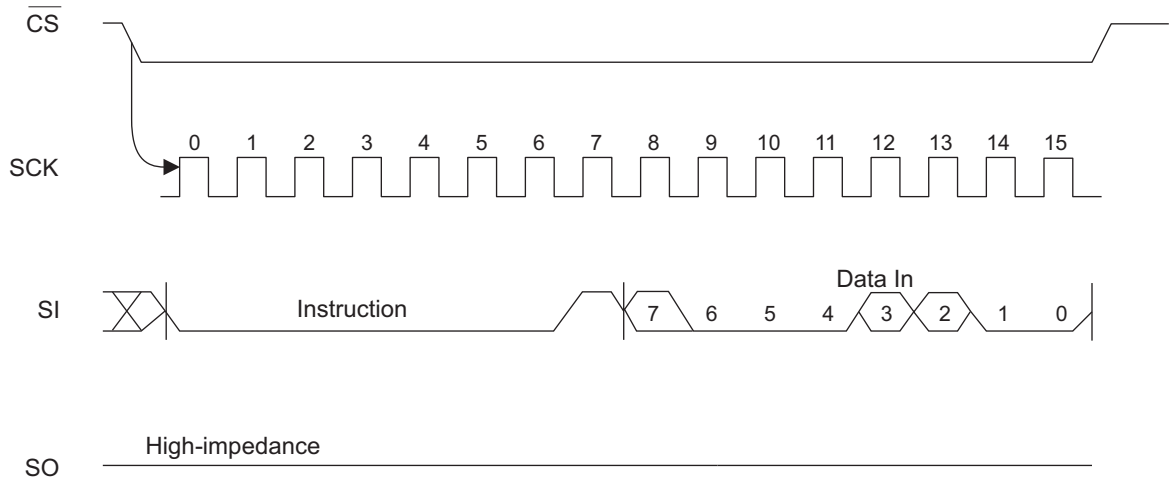


**Figure 7-6. Read Timing**

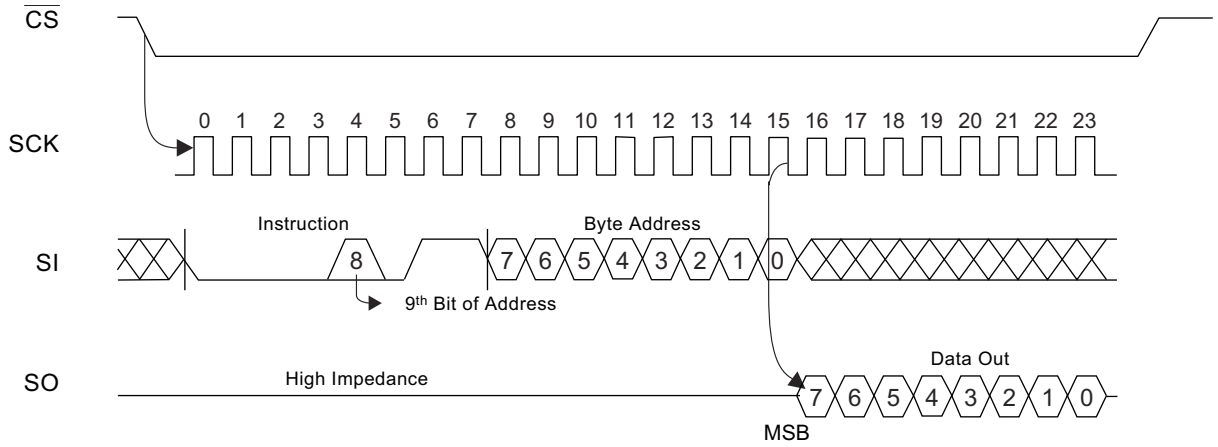



**Figure 7-7. Write Timing**

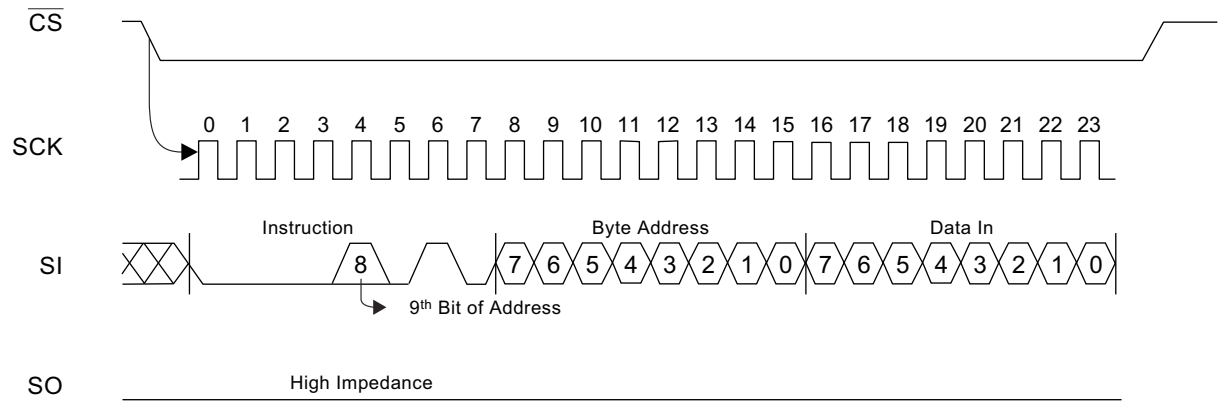
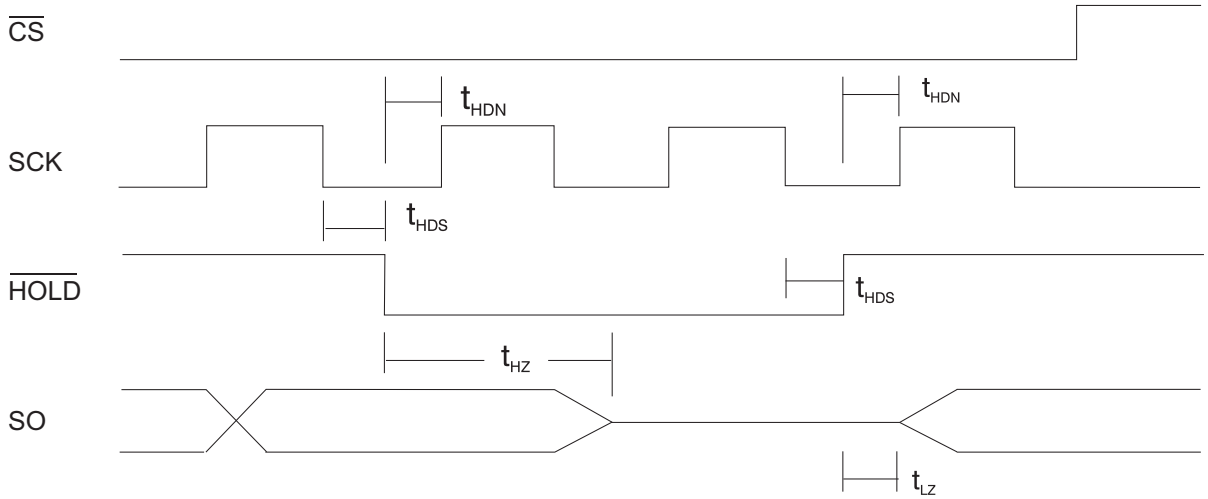


**Figure 7-8. $\overline{\text{HOLD}}$ Timing**

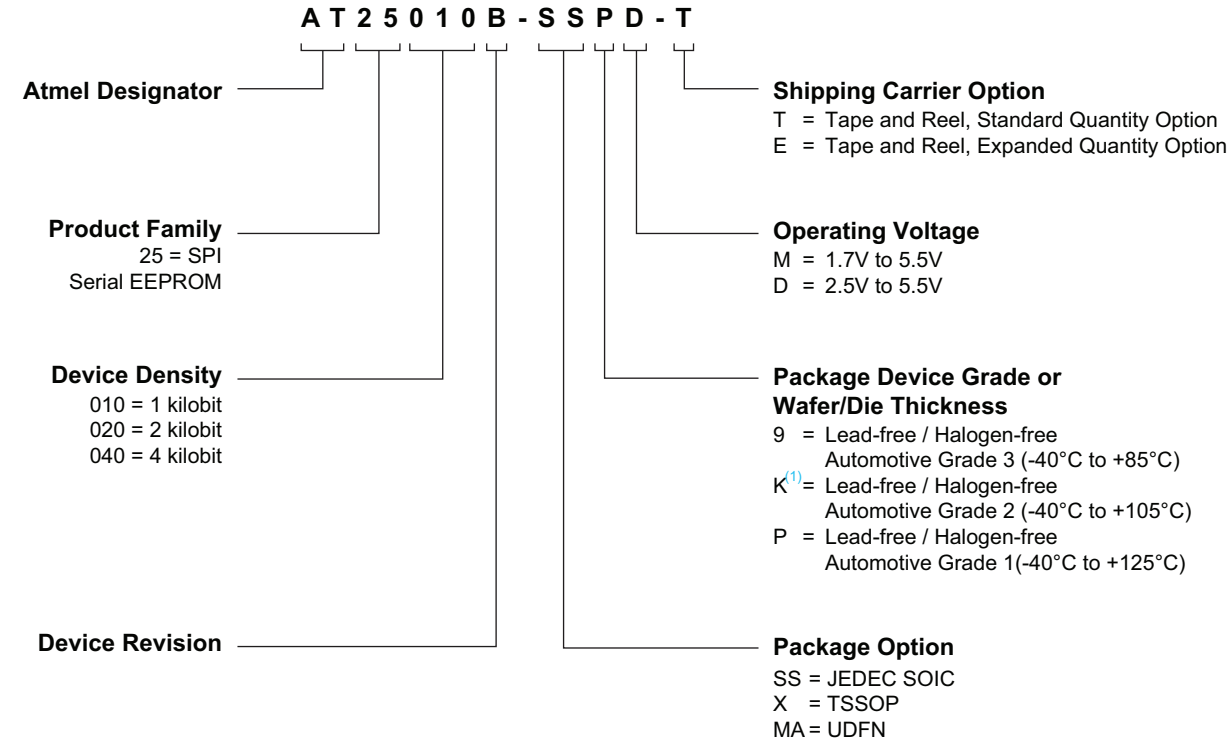



## 7.1 Power Recommendation

The device internal POR (Power-On Reset) threshold is just below the minimum device operating voltage. Power shall rise monotonically from 0.0Vdc to full $V_{CC}$ in less than 1ms. Hold at full $V_{CC}$ for at least 100µs before the first operation. Power shall drop from full $V_{CC}$ to 0.0Vdc in less than 1ms. Power dropping to a non-zero level and then slowly going to zero is *not* recommended. Power shall remain off (0.0Vdc) for 0.5s minimum. Please consult Atmel if your power conditions do not meet the above recommendations.

# 8. Ordering Information

## 8.1 Ordering Code Detail




Note: 1. Contact Sales for Grade 2 Availability

## 8.2 Ordering Code Information

### 8.2.1 Automotive Grade 1, $V_{CC}$ = 2.5V to 5.5V

| Atmel Ordering Code | Lead Finish | Package | Delivery Information | | Operation Range |
|---|---|---|---|---|---|
| | | | Form | Quantity | |
| AT25010B-SSPD-T | NiPdAu (Lead-free/Halogen-free) | 8S1 | Tape and Reel | 4,000 per Reel | Automotive Temperature (-40°C to 125°C) |
| AT25010B-XPD-T | | 8X | | 5,000 per Reel | |
| AT25010B-MAPD-T | | 8MA2 | | 5,000 per Reel | |
| AT25010B-MAPD-E | | | | 15,000 per Reel | |
| AT25020B-SSPD-T | NiPdAu (Lead-free/Halogen-free) | 8S1 | Tape and Reel | 4,000 per Reel | Automotive Temperature (-40°C to 125°C) |
| AT25020B-XPD-T | | 8X | | 5,000 per Reel | |
| AT25020B-MAPD-T | | 8MA2 | | 5,000 per Reel | |
| AT25020B-MAPD-E | | | | 15,000 per Reel | |
| AT25040B-SSPD-T | NiPdAu (Lead-free/Halogen-free) | 8S1 | Tape and Reel | 4,000 per Reel | Automotive Temperature (-40°C to 125°C) |
| AT25040B-XPD-T | | 8X | | 5,000 per Reel | |
| AT25040B-MAPD-T | | 8MA2 | | 5,000 per Reel | |
| AT25040B-MAPD-E | | | | 15,000 per Reel | |

| Package Type | |
|---|---|
| 8S1 | 8-lead, 0.150" wide, Plastic Gull Wing Small Outline (JEDEC SOIC) |
| 8X | 8-lead 4.4mm body, Plastic Thin Shrink Small Outline (TSSOP) |
| 8MA2 | 8-pad, 2.00mm x 3.00mm body, 0.50mm pitch, Ultra Thin, Dual No Lead (UDFN) |

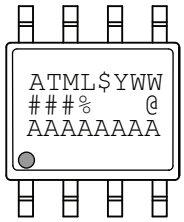
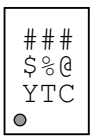
### 8.2.2 Automotive Grade 3, $V_{CC}$ = 1.7V to 5.5V

| Atmel Ordering Code | Lead Finish | Package | Delivery Information | | Operation Range |
|---|---|---|---|---|---|
| | | | Form | Quantity | |
| AT25010B-SS9M-T | NiPdAu (Lead-free/Halogen-free) | 8S1 | Tape and Reel | 4,000 per Reel | Automotive Temperature (-40°C to 85°C) |
| AT25010B-X9M-T | | 8X | | 5,000 per Reel | |
| AT25010B-MA9M-T | | 8MA2 | | 5,000 per Reel | |
| AT25010B-MA9M-E | | | | 15,000 per Reel | |
| | | | | | |
| AT25020B-SS9M-T | NiPdAu (Lead-free/Halogen-free) | 8S1 | Tape and Reel | 4,000 per Reel | Automotive Temperature (-40°C to 85°C) |
| AT25020B-X9M-T | | 8X | | 5,000 per Reel | |
| AT25020B-MA9M-T | | 8MA2 | | 5,000 per Reel | |
| AT25020B-MA9M-E | | | | 15,000 per Reel | |
| | | | | | |
| AT25040B-SS9M-T | NiPdAu (Lead-free/Halogen-free) | 8S1 | Tape and Reel | 4,000 per Reel | Automotive Temperature (-40°C to 85°C) |
| AT25040B-X9M-T | | 8X | | 5,000 per Reel | |
| AT25040B-MA9M-T | | 8MA2 | | 5,000 per Reel | |
| AT25040B-MA9M-E | | | | 15,000 per Reel | |

| Package Type | |
|---|---|
| 8S1 | 8-lead, 0.150" wide, Plastic Gull Wing Small Outline (JEDEC SOIC) |
| 8X | 8-lead 4.4mm body, Plastic Thin Shrink Small Outline (TSSOP) |
| 8MA2 | 8-pad, 2.00mm x 3.00mm body, 0.50mm pitch, Ultra Thin, Dual No Lead (UDFN) |

## 8.3 Product Markings

### AT25010B, AT25020B, and AT25040B: Package Marking Information

| 8-lead SOIC | 8-lead TSSOP | 8-pad UDFN |
|---|---|---|
|  |  | 2.0 x 3.0 mm Body  |







Note 1: ● designates pin 1

Note 2: Package drawings are not to scale

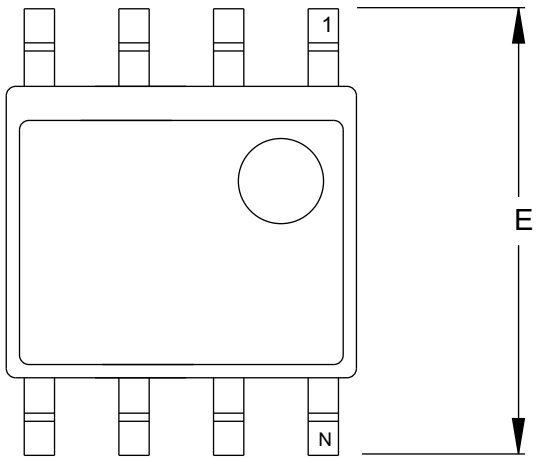
| **Catalog Number Truncation** | | | |
|---|---|---|---|
| AT25010B | | Truncation Code ###: 51B | |
| AT25020B | | Truncation Code ###: 52B | |
| AT25040B | | Truncation Code ###: 54B | |
| **Date Codes** | | | **% = Voltages** |
| Y = Year | M = Month | WW = Work Week of Assembly | M: 1.7V min |
| 6: 2016 0: 2020 | A: January | 02: Week 2 | D: 2.5V min |
| 7: 2017 1: 2021 | B: February | 04: Week 4 | |
| 8: 2018 2: 2022 | ... | ... | |
| 9: 2019 3: 2023 | L: December | 52: Week 52 | |
| **Country of Assembly** | **Lot Number** | | **$ = Grade/Lead Finish Material** |
| @ = Country of Assembly | AAA...A = Atmel Wafer Lot Number | | P: Automotive Grade 1/NiPdAu<br>K: Automotive Grade 2/NiPdAu<br>9: Automotive Grade 3/NiPdAu |
| **Trace Code** | | | **Atmel Truncation** |
| XX = Trace Code (Atmel Lot Numbers Correspond to Code)<br>Example: AA, AB.... YZ, ZZ | | | AT: Atmel<br>ATM: Atmel<br>ATML: Atmel |

4/20/2016

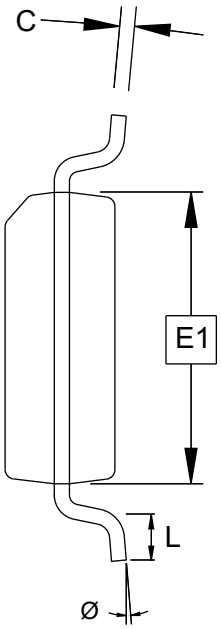
| Atmel<br>Package Mark Contact:<br>DL-CSO-Assy_eng@atmel.com | TITLE | DRAWING NO. | REV. |
|---|---|---|---|
| | 25010-20-40BAM, AT25010B, AT25020B and AT25040B<br>Automotive Package Marking Information | 25010-20-40BAM | E |

# 9. Packaging Information

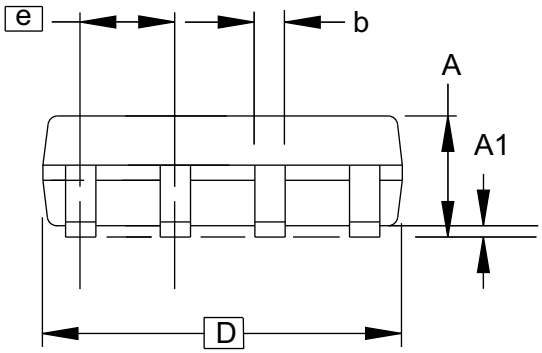
## 9.1 8S1 — 8-lead JEDEC SOIC




TOP VIEW




END VIEW




SIDE VIEW

Notes: This drawing is for general information only.
Refer to JEDEC Drawing MS-012, Variation AA
for proper dimensions, tolerances, datums, etc.

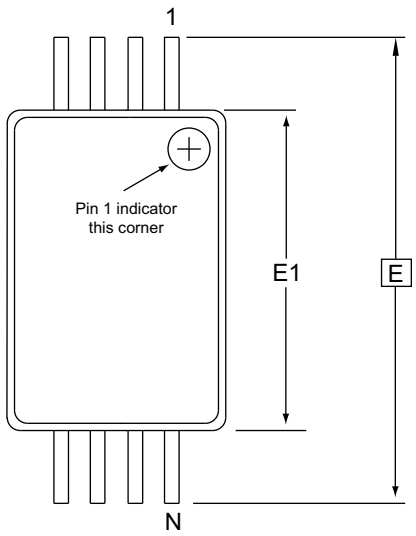
COMMON DIMENSIONS
(Unit of Measure = mm)

| SYMBOL | MIN | NOM | MAX | NOTE |
|---|---|---|---|---|
| A | – | – | 1.75 | |
| A1 | 0.10 | – | 0.25 | |
| b | 0.31 | – | 0.51 | |
| C | 0.17 | – | 0.25 | |
| D | | 4.90 BSC | | |
| E | | 6.00 BSC | | |
| E1 | | 3.90 BSC | | |
| e | | 1.27 BSC | | |
| L | 0.40 | – | 1.27 | |
| ø | 0° | – | 8° | |

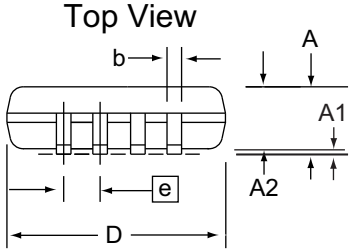
3/6/2015

| Atmel<br>Package Drawing Contact:<br>packagedrawings@atmel.com | **TITLE**<br>8S1, 8-lead (0.150” Wide Body), Plastic Gull Wing Small Outline (JEDEC SOIC) | **GPC**<br>SWB | **DRAWING NO.**<br>8S1 | **REV.**<br>H |
|---|---|---|---|---|

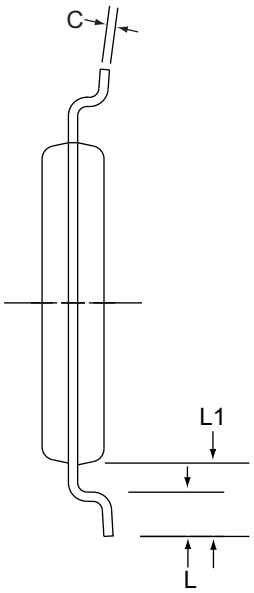
## 9.2 8X — 8-lead TSSOP




Top View




Side View




End View

Notes:
1. This drawing is for general information only. Refer to JEDEC Drawing MO-153, Variation AA, for proper dimensions, tolerances, datums, etc.
2. Dimension D does not include mold Flash, protrusions or gate burrs. Mold Flash, protrusions and gate burrs shall not exceed 0.15mm (0.006in) per side.
3. Dimension E1 does not include inter-lead Flash or protrusions. Inter-lead Flash and protrusions shall not exceed 0.25mm (0.010in) per side.
4. Dimension b does not include Dambar protrusion. Allowable Dambar protrusion shall be 0.08mm total in excess of the b dimension at maximum material condition. Dambar cannot be located on the lower radius of the foot. Minimum space between protrusion and adjacent lead is 0.07mm.
5. Dimension D and E1 to be determined at Datum Plane H.

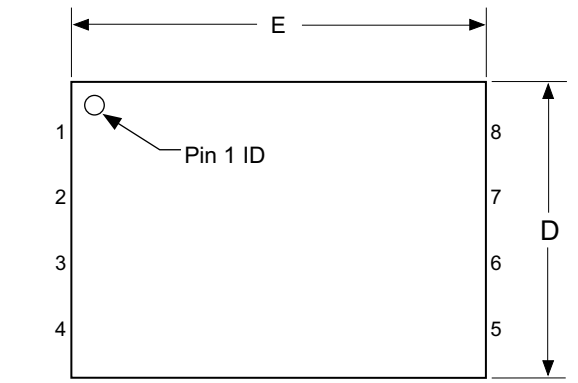
COMMON DIMENSIONS
(Unit of Measure = mm)

| SYMBOL | MIN | NOM | MAX | NOTE |
|---|---|---|---|---|
| A | - | - | 1.20 | |
| A1 | 0.05 | - | 0.15 | |
| A2 | 0.80 | 1.00 | 1.05 | |
| D | 2.90 | 3.00 | 3.10 | 2, 5 |
| E | | 6.40 BSC | | |
| E1 | 4.30 | 4.40 | 4.50 | 3, 5 |
| b | 0.19 | 0.25 | 0.30 | 4 |
| e | | 0.65 BSC | | |
| L | 0.45 | 0.60 | 0.75 | |
| L1 | | 1.00 REF | | |
| C | 0.09 | - | 0.20 | |

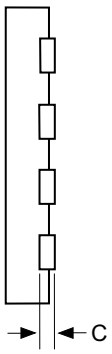
2/27/14

| Atmel<br>Package Drawing Contact:<br>packagedrawings@atmel.com | TITLE<br>8X, 8-lead 4.4mm Body, Plastic Thin Shrink Small Outline Package (TSSOP) | GPC<br>TNR | DRAWING NO.<br>8X | REV.<br>E |
|---|---|---|---|---|

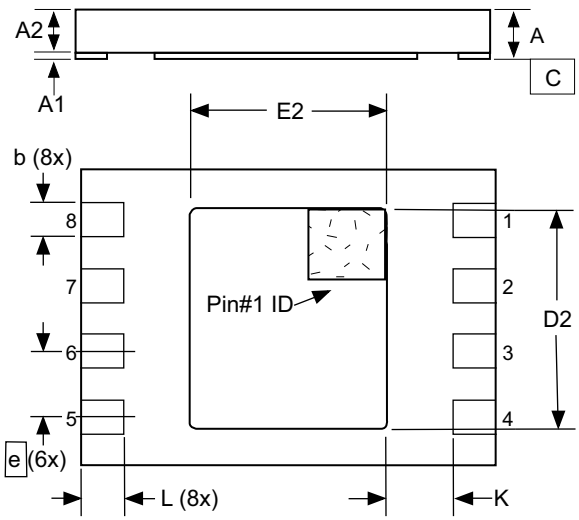
## 9.3 8MA2 — 8-pad UDFN




TOP VIEW




SIDE VIEW




BOTTOM VIEW

Notes:
1. This drawing is for general information only. Refer to Drawing MO-229, for proper dimensions, tolerances, datums, etc.
2. The Pin #1 ID is a laser-marked feature on Top View.
3. Dimensions b applies to metallized terminal and is measured between 0.15 mm and 0.30 mm from the terminal tip. If the terminal has the optional radius on the other end of the terminal, the dimension should not be measured in that radius area.
4. The Pin #1 ID on the Bottom View is an orientation feature on the thermal pad.

COMMON DIMENSIONS
(Unit of Measure = mm)

| SYMBOL | MIN | NOM | MAX | NOTE |
|---|---|---|---|---|
| A | 0.50 | 0.55 | 0.60 | |
| A1 | 0.0 | 0.02 | 0.05 | |
| A2 | - | - | 0.55 | |
| D | 1.90 | 2.00 | 2.10 | |
| D2 | 1.40 | 1.50 | 1.60 | |
| E | 2.90 | 3.00 | 3.10 | |
| E2 | 1.20 | 1.30 | 1.40 | |
| b | 0.18 | 0.25 | 0.30 | 3 |
| C | 0.152 REF | | | |
| L | 0.35 | 0.40 | 0.45 | |
| e | 0.50 BSC | | | |
| K | 0.20 | - | - | |

11/2/15

| Atmel<br>Package Drawing Contact:<br>packagedrawings@atmel.com | TITLE<br>8MA2, 8-pad 2 x 3 x 0.6mm Body, Thermally Enhanced Plastic Ultra Thin Dual Flat No-Lead Package (UDFN) | GPC<br>YNZ | DRAWING NO.<br>8MA2 | REV.<br>H |
|---|---|---|---|---|

# 10. Revision History

| Doc. Rev. | Date | Comments |
|---|---|---|
| 8802E | 12/2016 | Decreased $I_{SB1}$ maximum from 9µA to 2µA |
| 8802D | 09/2016 | Added the Automotive Grade 2 and 3 options and UDFN options.<br>Updated 8S1 and 8X package drawings, template / reorganization, and disclaimer page. |
| 8802C | 11/2012 | Updated ordering code tables.<br>Updated 8X package drawing. |
| 8802B | 10/2012 | Removed preliminary status.<br>Updated Atmel logos and disclaimer/copy page. |
| 8802A | 03/2012 | Initial document release. |

**Atmel Corporation** 1600 Technology Drive, San Jose, CA 95110 USA **T:** (+1)(408) 441.0311 **F:** (+1)(408) 436.4200 | **www.atmel.com**