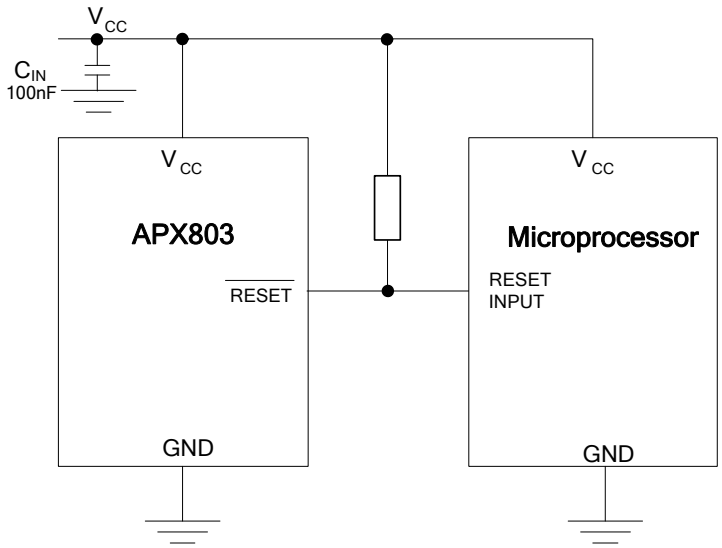
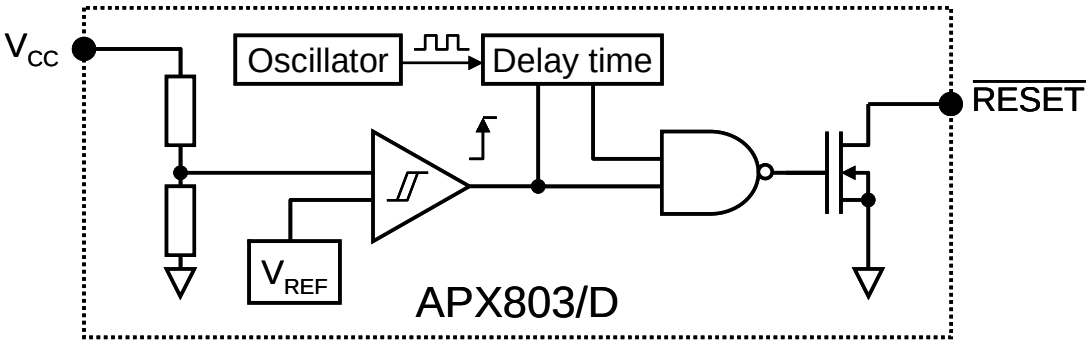
Typical Application Circuit



Pin Descriptions

Pin Name	Description
GND	Ground
$\overline{\text{RESET}}$	Reset Output Pin Active Low Open Drain
V_{CC}	Operating Voltage Input

Functional Block Diagram



Absolute Maximum Ratings

Symbol	Parameter	Rating	Unit
ESD HBM	Human Body Model ESD Protection	2	kV
ESD MM	Machine Model ESD Protection	200	V
V_{CC}	Supply Voltage	-0.3 to +6.0	V
V_{RESET}	$\overline{RESET}$ (open drain)	-0.3 to 6	V
I_{CC}	Input Current, V_{CC}	20	mA
I_O	Output Current, $\overline{RESET}$	20	mA
P_D	Continuous Power Dissipation (T_A = +70°C), de-rate 4mW/°C above +70°C	400	mW
T_{OP}	Operating Junction Temperature Range	-40 to +105	°C
T_{ST}	Storage Temperature Range	-65 to +150	°C

Recommended Operating Conditions

Symbol	Parameter	Min	Max	Unit
V_{CC}	Supply Voltage	1.1	5.5	V
V_{IN}	Input Voltage	0	(V_{CC}+0.3)	V
V_{RESET}	$\overline{RESET}$ output voltage	0	5.5	V
T_A	Operating Ambient Temperature Range	-40	85	°C
dV_{CC}/dt	V_{CC} Rate of rise (V_{CC} = 0~V_T)		100	V/µs

Electrical Characteristics (T_A = 25°C)

T_A= -40 to 85°C unless otherwise note. Typical values are at T_A=+25 °C.

Symbol	Parameter		Test Conditions	Min	Typ.	Max	Unit
I_{CC}	Supply Current		V_{TH} + 0.2V		30	40	µA
V_{TH}	Reset Threshold	APX803-23	T_A = 25°C	2.21	2.25	2.30	V
		APX803-26		2.59	2.63	2.66	
		APX803-29		2.89	2.93	2.96	
		APX803D-29		2.89	2.93	2.96	
		APX803-31		3.04	3.08	3.13	
		APX803-40		3.94	4.00	4.06	
		APX803-44		4.31	4.38	4.45	
		APX803-46		4.56	4.63	4.70	
	Reset Threshold hysteresis		V_{TH-H} – V_{TH-L}		40		mV
	Reset Threshold Tempco				30		ppm/°C
t_S	V_{CC} to RESET delay		V_{CC} = V_{TH} to (V_{TH} – 100mV)		20		µs
t_{DELAY}	Reset Active Timeout Period	APX803-XX	T_A = 0°C to +85°C	140	200	280	ms
		APX803D-29		1		3.3	
V_{OL}	$\overline{RESET}$ Output Voltage Low		V_{CC} = V_{TH} -0.2, I_{SINK} = 1.2mA			0.3	V
			V_{CC} = V_{TH} -0.2, I_{SINK} = 3.5mA			0.4	
			V_{CC} > 1.0V, I_{SINK} = 50uA			0.3	
I_{OH}	$\overline{RESET}$ Output High leakage current		V_{CC} > V_{TH} +0.2			1	µA
θ_{JA}	Thermal Resistance Junction-to-Ambient		SOT23/SOT23R (Note 2)		201		°C/W
θ_{JC}	Thermal Resistance Junction-to-Case		SOT23/SOT23R (Note 2)		56		°C/W

Notes: 2. Test condition for SOT23 and SOT23R: Devices mounted on FR-4 substrate PC board, 2oz copper, with minimum recommended pad layout.
3. Final datasheet limits to be determined by characterization and correlation.

Typical Performance Characteristics

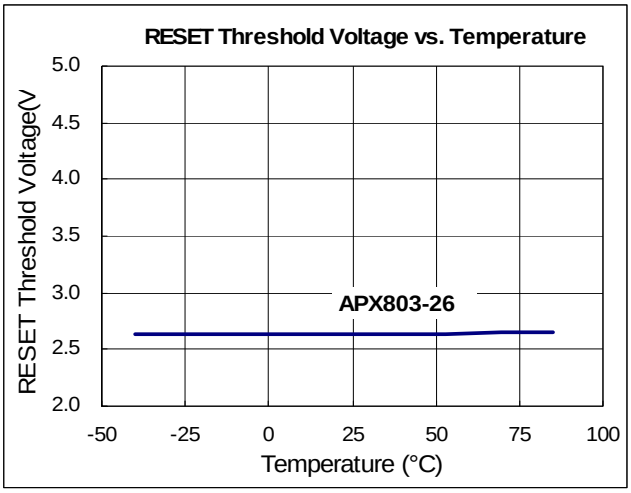


Figure 1

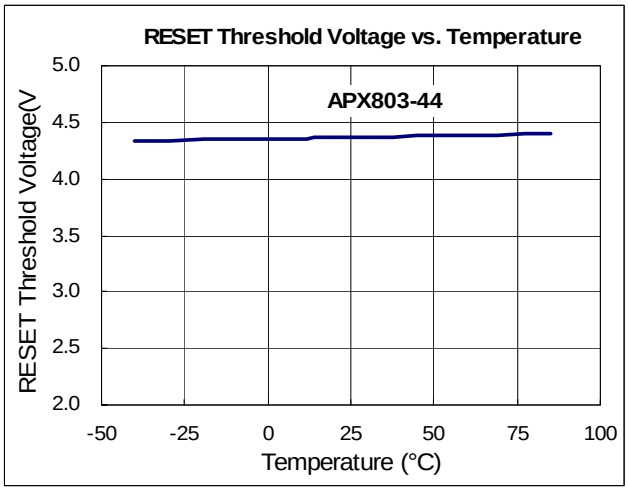


Figure 2

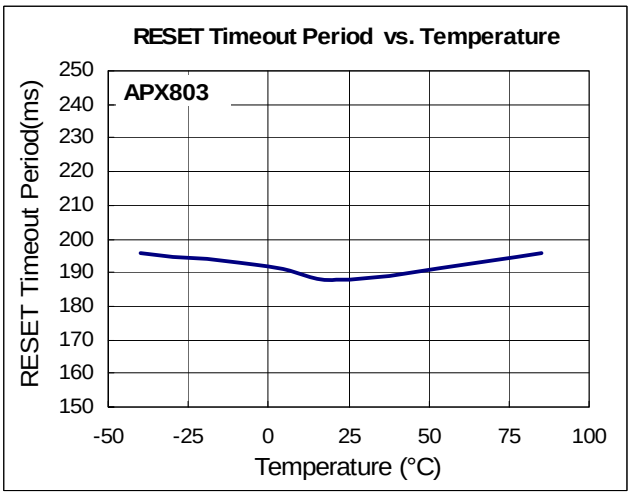


Figure 3

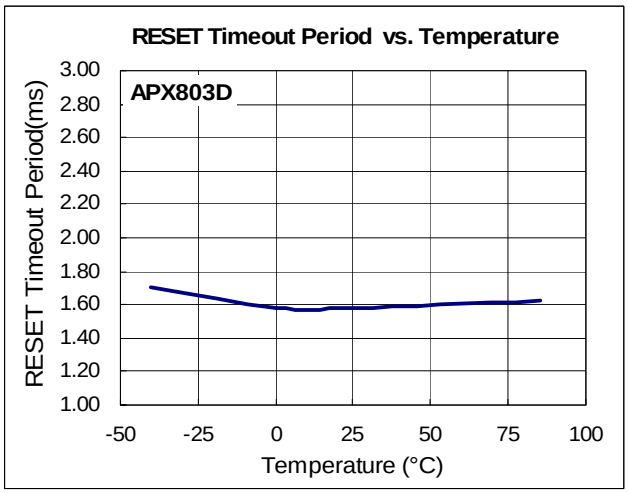


Figure 4

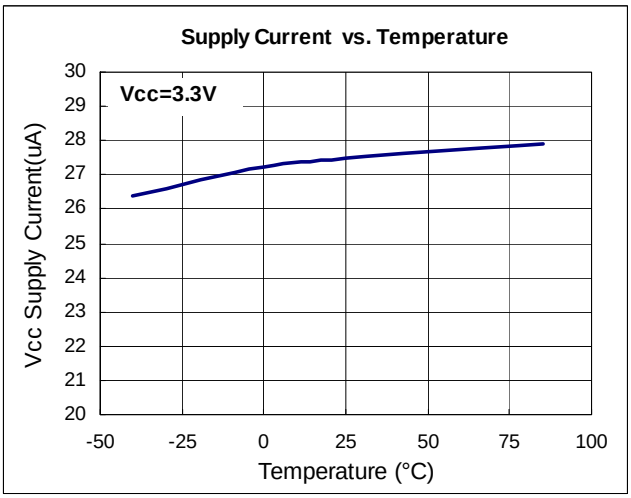


Figure 5

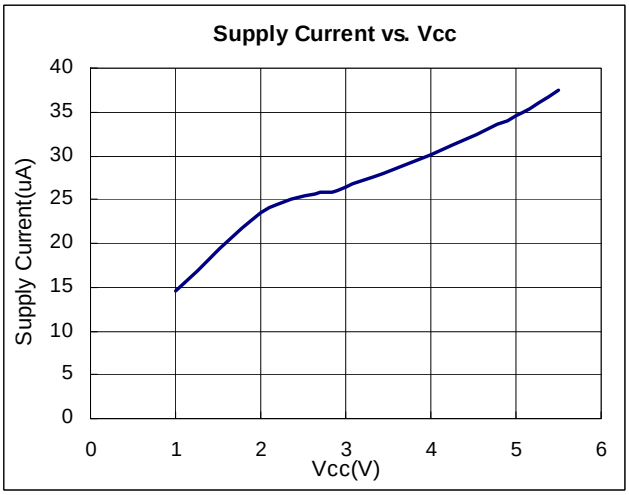


Figure 6

Typical Performance Characteristics (Continued)

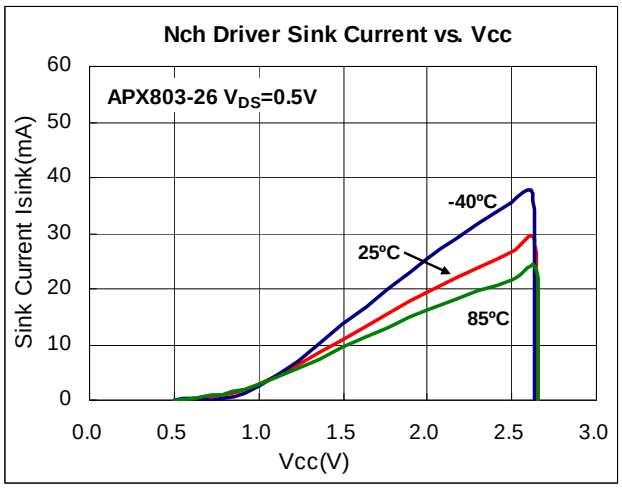


Figure 7

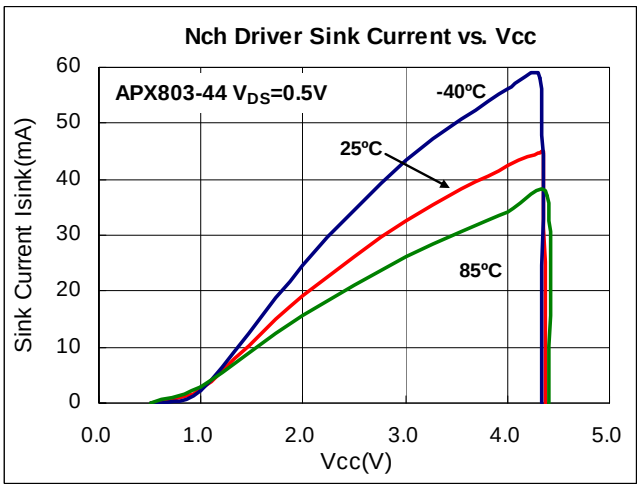


Figure 8

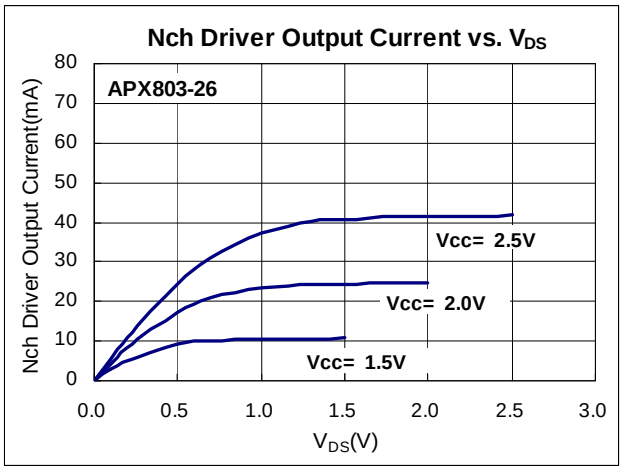


Figure 9

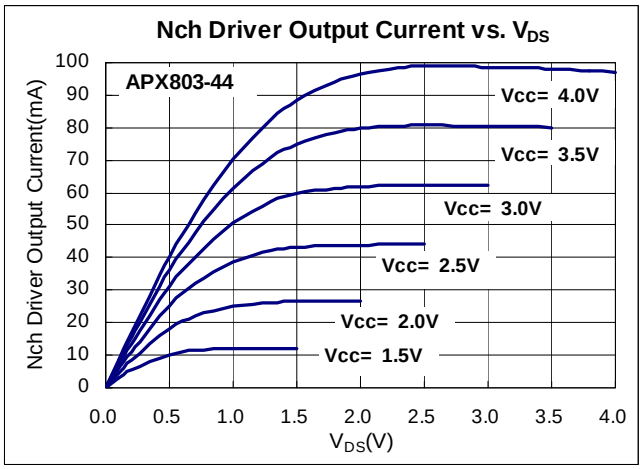
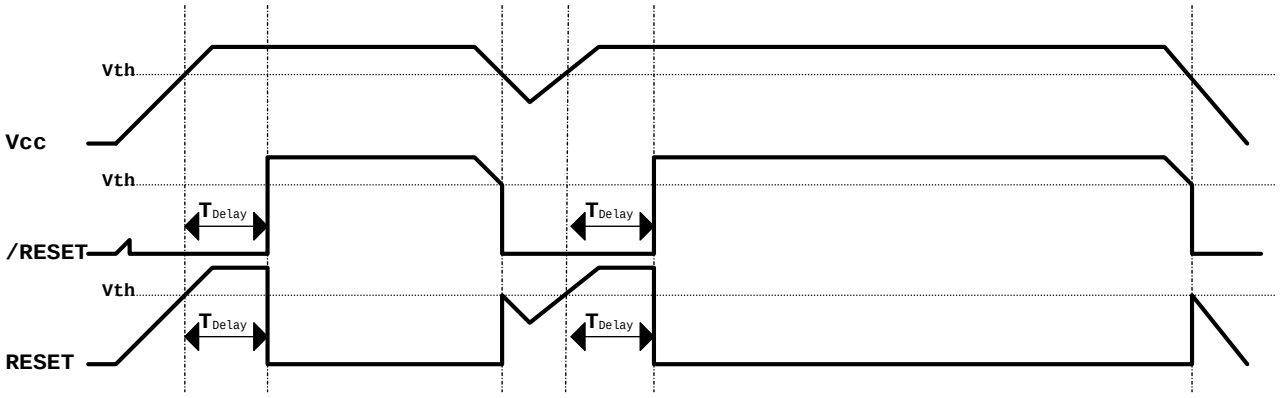


Figure 10

Timing Diagram



Functional Description

Microprocessors (µPs) and microcontrollers (µC) have a reset input to ensure that it starts up in a known state. The APX803/D drive the µP's reset input to prevent code-execution errors during power-up, power-down, or brownout conditions. They assert a reset signal whenever the V_{CC} supply voltage declines below a preset threshold and keep it asserted for a fixed period of time after V_{CC} has risen above the reset threshold. For the APX803D this period is a minimum of 1ms while for other APX803 variants it is at least 140ms. The APX803/D have an open-drain output stage.

Ensuring a Valid Reset Output Down to V_{CC} = 0

$\overline{\text{RESET}}$ is guaranteed to be a logic low for V_{CC} > 1V. Once V_{CC} exceeds the reset threshold, an internal timer keeps $\overline{\text{RESET}}$ low for the reset timeout period; after this interval, $\overline{\text{RESET}}$ goes high. If a brownout condition occurs (V_{CC} dips below the $\overline{\text{RESET}}$ reset threshold), $\overline{\text{RESET}}$ goes low. Any time V_{CC} goes below the reset threshold, the internal timer resets to zero, and $\overline{\text{RESET}}$ goes low. The internal timer starts after V_{CC} returns above the reset threshold, and $\overline{\text{RESET}}$ remains low for the reset timeout period.

When V_{CC} falls below 1V, the APX803/D $\overline{\text{RESET}}$ output no longer sinks current — it becomes an open circuit. Therefore, high-impedance CMOS logic inputs connected to $\overline{\text{RESET}}$ can drift to undetermined voltages. This presents no problem in most applications since most µP and other circuitry is inoperative with V_{CC} below 1V.

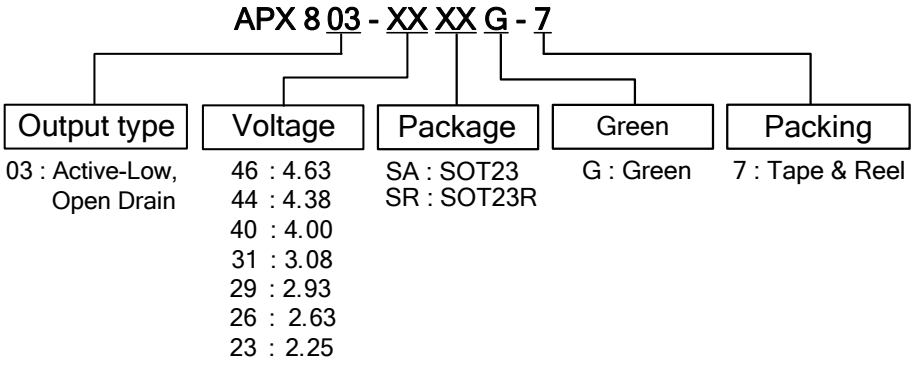
Interfacing to µP with Bidirectional Reset Pins

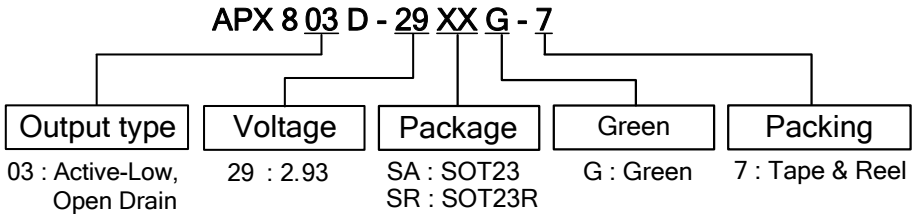
Since the RESET output on the APX803/D is open drain, this device interfaces easily with µP/µC that have bidirectional reset pins, such as the Motorola 68HC11. Connecting the µP supervisor's RESET output directly to the microcontroller's (µC's) RESET pin with a single pull-up resistor allows either device to assert reset.

Supervising and monitoring Multiple Supplies

Generally, the pull-up resistor connected to the APX803/D will connect to the supply voltage that is being monitored at the IC's V_{CC} pin. However, some systems may use the APX803/D open-drain output to level-shift from the monitored supply to reset the µP powered by a different supply voltage or monitor multiple supplies that will be fed into 1 µC/µP reset input.

Ordering Information





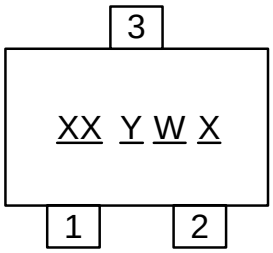
Device	Package Code	Packaging (Note 4)	7" Tape and Reel	
			Quantity	Part Number Suffix
APX803-XXSAG-7	SA	SOT23	3000/Tape & Reel	-7
APX803-XXSRG-7	SR	SOT23R	3000/Tape & Reel	-7
APX803D-29SAG-7	SA	SOT23	3000/Tape & Reel	-7
APX803D-29SRG-7	SR	SOT23R	3000/Tape & Reel	-7

Notes: 4. Pad layout as shown on Diodes Inc. suggested pad layout document AP02001, which can be found on our website at http://www.diodes.com/datasheets/ap02001.pdf.

Marking Information

(1) SOT23 and SOT23R

(Top View)

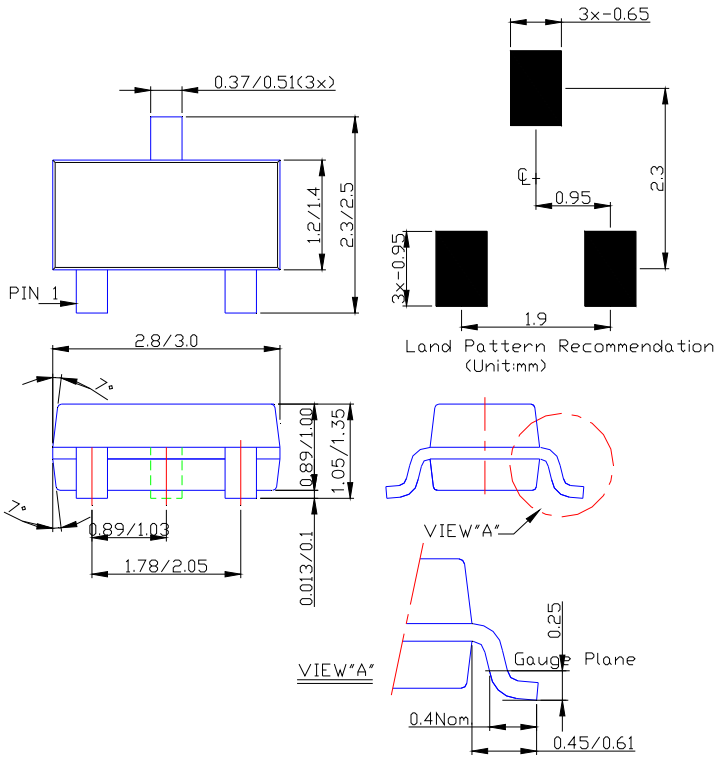


XX : Identification code
Y : Year 0~9
W : Week : A~Z : 1~26 week;
a~z : 27~52 week; z represents
52 and 53 week
X : A~Z : Green

Device	Package	Identification Code
APX803-46SA	SOT23	V3
APX803-44SA	SOT23	V4
APX803-40SA	SOT23	V5
APX803-31SA	SOT23	V6
APX803-29SA	SOT23	V7
APX803-26SA	SOT23	V8
APX803-23SA	SOT23	V9
APX803-46SR	SOT23R	S3
APX803-44SR	SOT23R	S4
APX803-40SR	SOT23R	S5
APX803-31SR	SOT23R	S6
APX803-29SR	SOT23R	S7
APX803-26SR	SOT23R	S8
APX803-23SR	SOT23R	S9
APX803D-29SA	SOT23	VN
APX803D-29SR	SOT23R	SN

Package Outline Dimensions (All Dimensions in mm)

(1) Package Type: SOT23 and SOT23R



Notes: 5. Package outline dimensions as shown on Diodes Inc. package outline dimensions document AP02002, which can be found on our website at http://www.diodes.com/datasheets/ap02002.pdf

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