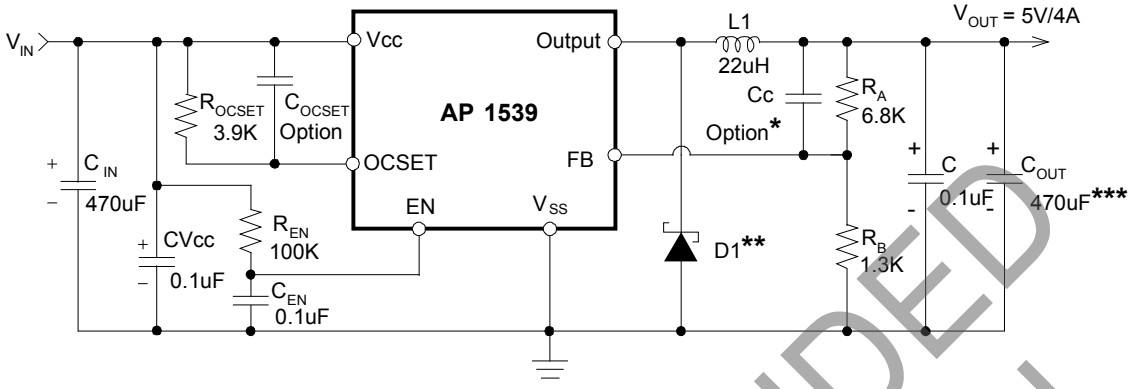
Typical Application Circuit



$V_{OUT}=V_{FB}$ x $(1+R_A/R_B)$

R_B= 0.7K~5K ohm

Notes: * Typical feedback compensation (Cc): 5600pF.
** Suggested Diodes Incorporated Power Schottky P/N: B540 series or PDS540.
*** Suggested C_{OUT} for V_{OUT} < 1V; 680uF.

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Pin Descriptions

Pin Name	Pin No.	Description
FB	1	Feedback pin
EN	2	Power-off pin H: Normal operation (Step-down operation) L: Step-down operation stopped (All circuits deactivated)
OCSET	3	Add an external resistor to set max output current
V_{CC}	4	IC power supply pin
Output	5, 6	Switch Pin. Connect external inductor/diode here. Minimize trace area at this pin to reduce EMI
V_{SS}	7, 8	GND Pin

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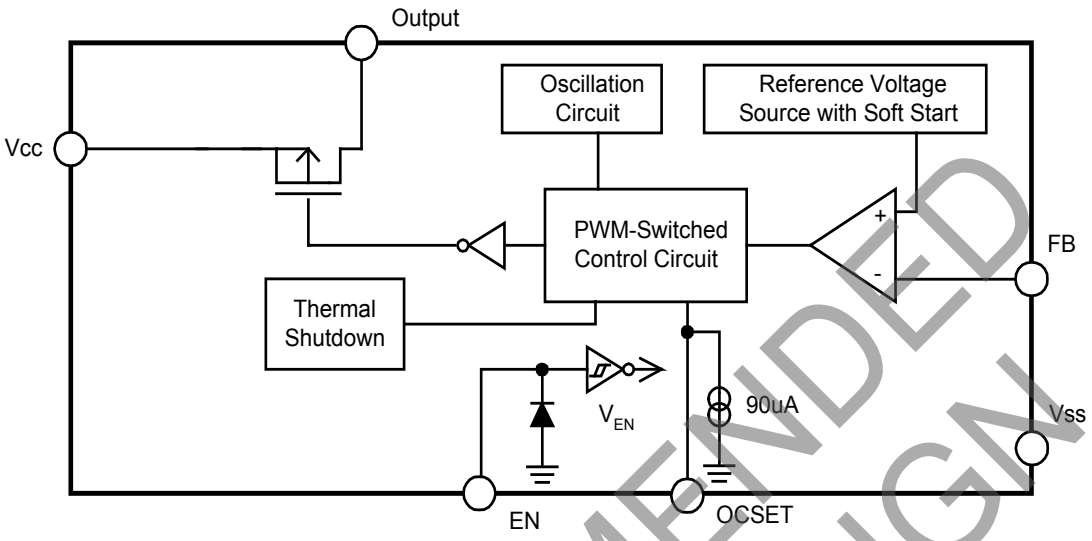
Block Diagram



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Absolute Maximum Ratings

Symbol	Parameter	Rating	Unit
ESD HBM	Human Body Model ESD Protection	5.5	KV
ESD MM	Machine Model ESD Protection	200	V
V_{CC}	V_{CC} Pin Voltage	V_{SS} - 0.3 to V_{SS} + 20	V
V_{FB}	Feedback Pin Voltage	V_{SS} - 0.3 to V_{CC}	V
V_{EN}	EN Pin Voltage	V_{SS} - 0.3 to V_{CC}	V
V_{OUT}	Switch Pin Voltage	V_{SS} - 0.3 to V_{CC}	V
P_D	Power Dissipation	Internally limited	mW
T_J	Operating Junction Temperature Range	-40 to +125	°C
T_{ST}	Storage Temperature Range	-65 to +150	°C

Caution: The absolute maximum ratings are rated values exceeding which the product could suffer physical damage. These values must therefore not be exceeded under any conditions.

Recommended Operating Conditions

Symbol	Parameter	Min	Max	Unit
V_{IN}	Input Voltage (Note 5)	3.6	18	V
I_{OUT}	Output Current	0	4	A
T_A	Operating Ambient Temperature	-20	+85	°C

Note: 5. For the operations in low input voltage, AP1539 can tolerate down to 3.6V but max output current loading will be less than 4A. For nominal applications in such low input voltage range, especially lower than 4V, a higher ROCSET with larger heat sink is recommended.

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Electrical Characteristics

(V_{IN} = 12V, T_A = +25°C, unless otherwise specified)

Symbol	Parameter	Conditions	Min	Typ.	Max	Unit
V_{FB}	Feedback Voltage	I_{OUT} = 0.1A	0.784	0.8	0.816	V
I_{FB}	Feedback Bias Current	I_{OUT} = 0.1A	—	0.1	0.5	μA
I_{SHDN}	Current Consumption During Power Off	V_{EN} = 0V	—	10	—	μA
ΔV_{OUT} / V_{IN}	Line Regulation	V_{IN} = 5V~18V	—	1	2	%
ΔV_{OUT} / V_{OUT}	Load Regulation	I_{OUT} = 0.1 to 4A	—	0.2	0.5	%
f_{OSC}	Oscillation Frequency	Measure waveform at SW pin	240	300	400	KHz
f_{OSC1}	Frequency of Current Limit or Short Circuit Protection	Measure waveform at SW pin	—	50	—	KHz
V_{IH}	EN Pin Input Voltage	Evaluate oscillation at SW pin	2.0	—	—	V
V_{IL}		Evaluate oscillation stop at SW pin	—	—	0.8	
I_{SH}	EN Pin Input Leakage Current	EN Pin High	—	20	—	μA
I_{SL}		EN Pin Low	—	-10	—	μA
I_{OCSET}	OCSET Pin Bias Current	—	75	90	105	μA
$R_{DS(ON)}$	Internal MOSFET $R_{DS(ON)}$	V_{IN} = 5V, V_{FB} = 0V	—	90	—	mΩ
		V_{IN} = 12V, V_{FB} = 0V	—	50	—	
EFFI	Efficiency	V_{IN} = 12V, V_{OUT} = 5V I_{OUT} = 4A	—	92	—	%
T_{SHDN}	Thermal shutdown threshold	—	—	+150	—	°C
T_{HYS}	Thermal shutdown hysteresis	—	—	+55	—	°C
θ_{JC}	Thermal Resistance Junction-to-Case	SOP-8L-DEP (Note 6)	—	26	—	°C/W

Note: 6. Test condition for SOP-8L-DEP: Devices mounted on 2oz copper, minimum recommended pad layout on top & bottom layer with thermal vias, double sided FR-4 PCB.

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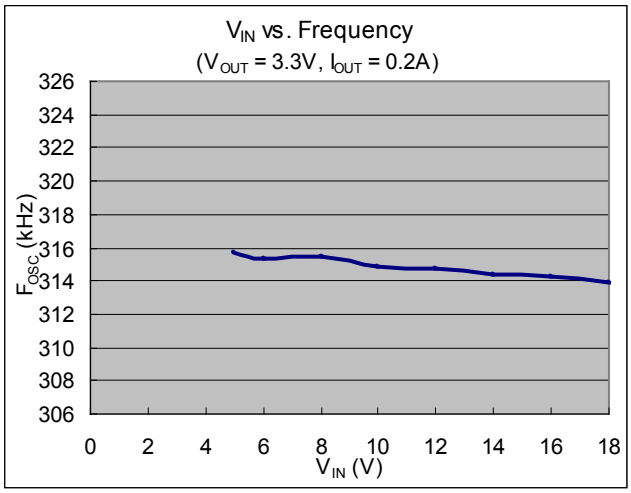
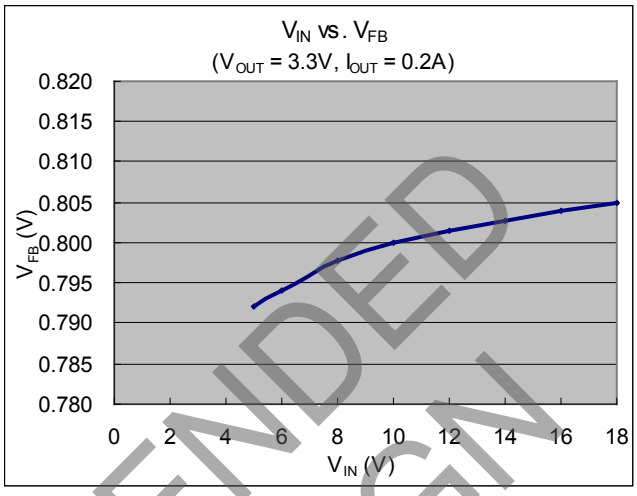
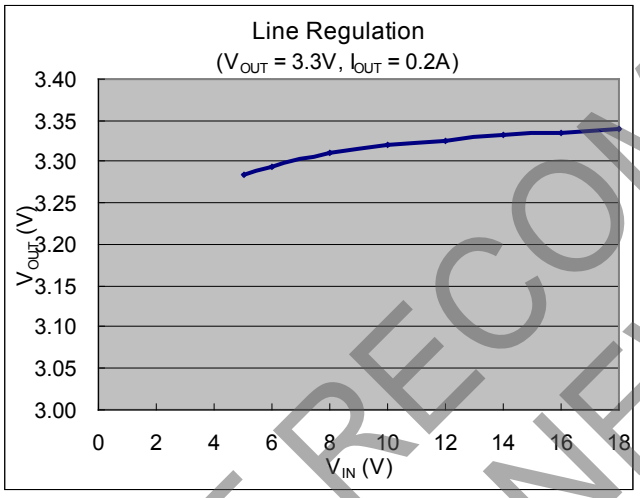
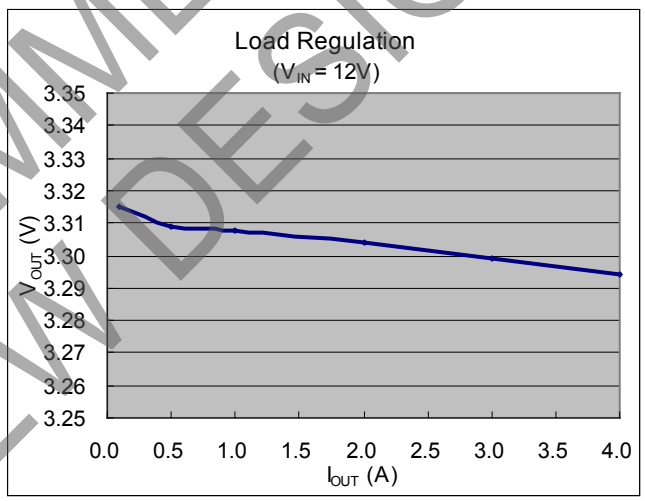
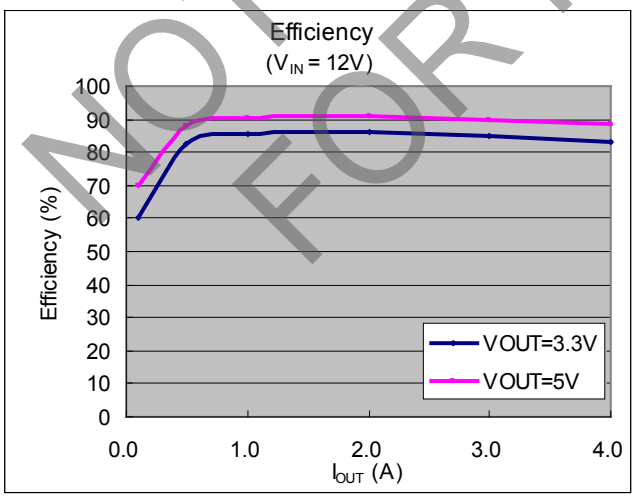
Typical Performance Characteristics

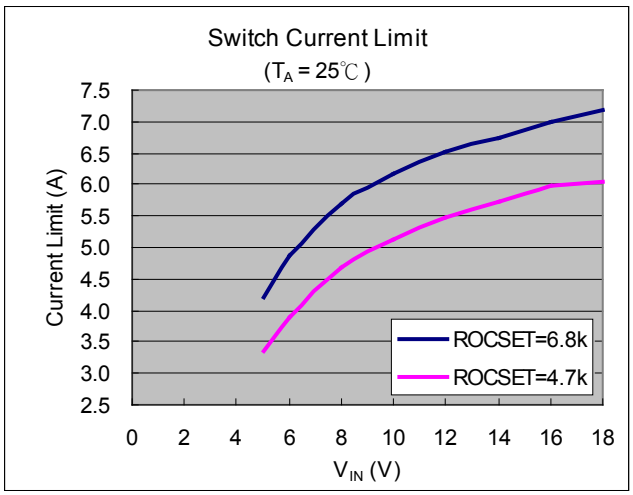












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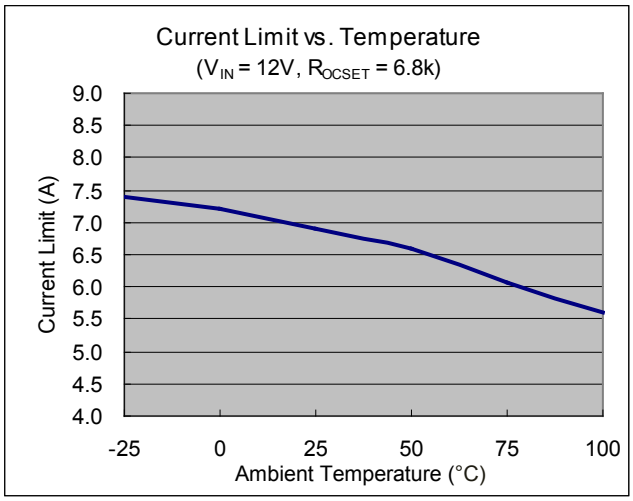
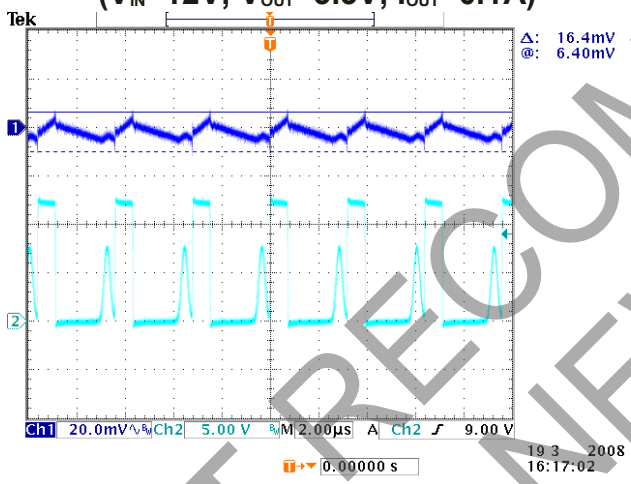
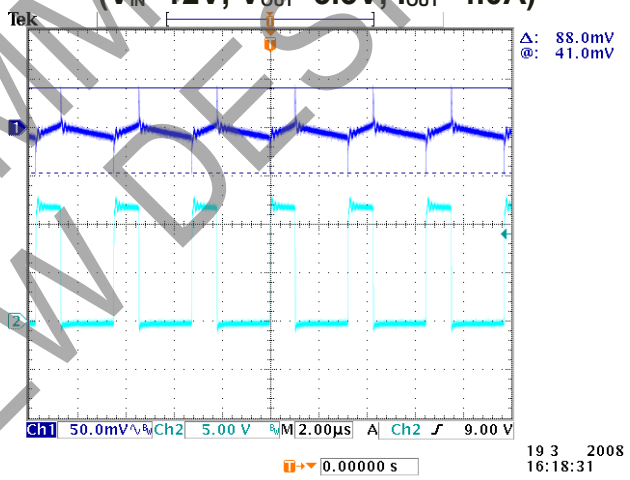
Typical Performance Characteristics (continued)



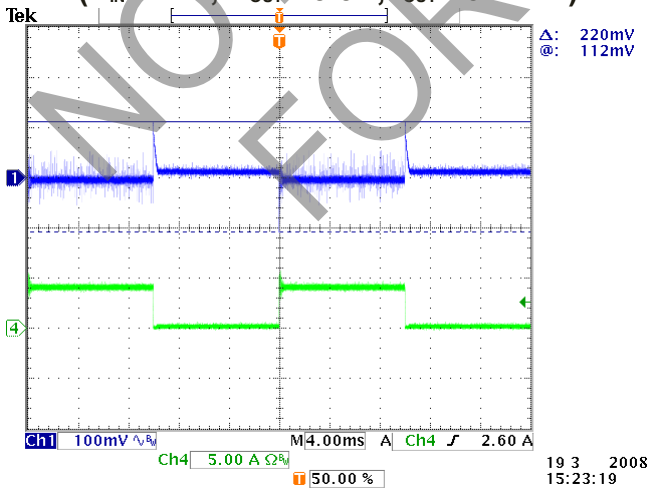
V_{OUT} Ripple
(V_{IN}=12V, V_{OUT}=3.3V, I_{OUT}=0.1A)



V_{OUT} Ripple
(V_{IN}=12V, V_{OUT}=3.3V, I_{OUT}=4.0A)



Load Transient Response
(V_{IN} =12V, V_{OUT} =3.3V, I_{OUT} =0.1~4A)



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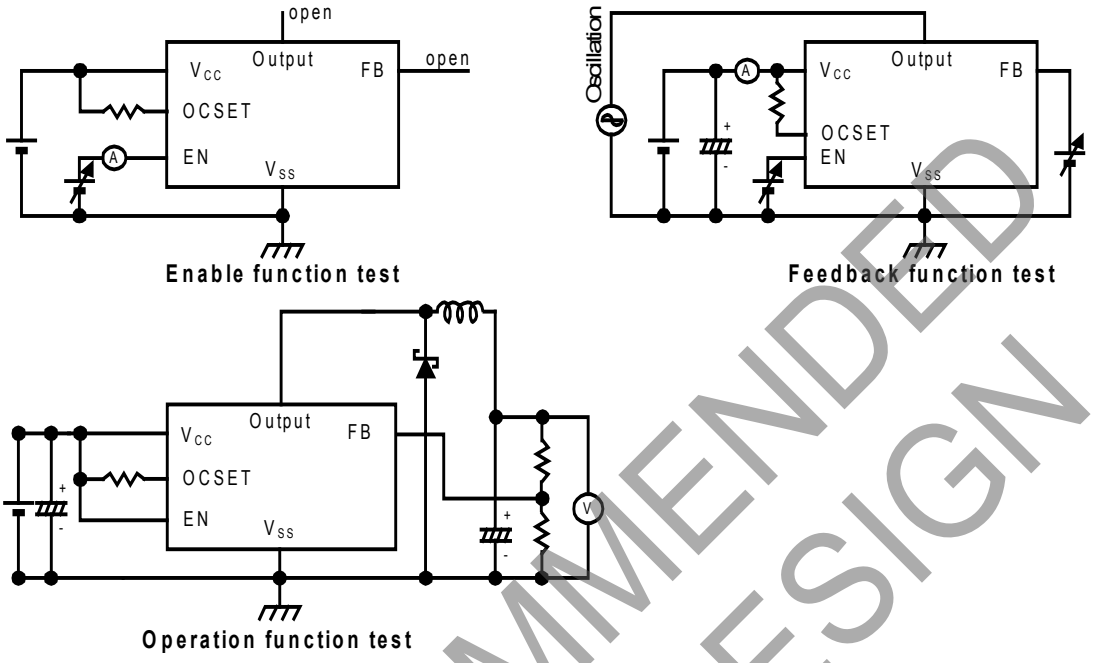
Test Circuit



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Functional Description

PWM Control
The AP1539 is a DC/DC converter that employs pulse width modulation (PWM) scheme. Its pulse width varies in the range of 0% to 99%, based on the output current loading. The output ripple voltage caused by the PWM high frequency switching can easily be reduced through an output filter. Therefore, this converter provides a low ripple output supply over a broad range of input voltage & output current loading.

Under Voltage Lockout
The under voltage lockout circuit of the AP1539 assures that the high-side MOSFET driver remains in the off state whenever the supply voltage drops below 3.3V. Normal operation resumes once V_{CC} rises above 3.5V.

Current Limit Protection
The current limit threshold is set by external resistor R_{OCSET} connected from V_{CC} supply to OCSET pin. The internal sink current I_{OCSET} (90uA typical) across this resistor sets the voltage at OCSET pin. When the PWM voltage is less than the voltage at OCSET, an over-current condition is triggered.

The current limit threshold is given by the following equation:

$$I_{PEAK} \times R_{DS(ON)} = I_{OCSET} \times R_{OCSET}$$

$$I_{PEAK} > I_{OUT(MAX)} + \frac{(\Delta I)}{2}$$

where,

$$\Delta I = \frac{V_{IN} - V_{OUT}}{fs \times L} \times \frac{V_{OUT}}{V_{IN}}$$

I_{PEAK} is the output peak current; $R_{DS\ (ON)}$ is the MOSFET ON resistance; F_S is the PWM frequency (300KHz typical). Also, the inductor value will affect the ripple current ΔI.

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Functional Description (continued)

The above equation is recommended for input voltage range of 5V to 18V. For input voltage lower than 5V, higher than 18V or ambient temperature over +100°C, higher R_{OCSET} is recommended.

The recommended minimum R_{OCSET} value is summarized below:

V_{OUT} (V)	V_{IN} (V)		
	5V	12V	18V
0.8	6.8K	3.9K	4.7K
1.0	6.8K	3.9K	4.7K
1.2	6.8K	3.9K	4.7K
1.8	6.8K	3.9K	4.7K
2.5	6.8K	3.9K	4.7K
3.3	6.8K	3.9K	4.7K
5.0	N/A	3.9K	5.6K

Inductor Selection
For most designs, the operates with inductors of 22μH to 33μH. The inductor value can be derived from the following equation:

$$L = \frac{V_{IN} - V_{OUT}}{fs \times \Delta I} \times \frac{V_{OUT}}{V_{IN}}$$

Where ΔI_L is inductor Ripple Current. Large value inductors lower ripple current and small value inductors result in high ripple current. Choose inductor ripple current approximately 15% of the maximum load current 4A, ΔI_L=0.6A. The DC current rating of the inductor should be at least equal to the maximum load current plus half the ripple current to prevent core saturation (4A+0.3A).

Input Capacitor Selection
This capacitor should be located close to the IC using short leads and the voltage rating should be approximately 1.5 times the maximum input voltage. The RMS current rating requirement for the input capacitor of a buck regulator is approximately 1⁄2 the DC load current. A low ESR input capacitor sized for maximum RMS current must be used. A 470μF low ESR capacitor for most applications is sufficient.

Output Capacitor Selection
The output capacitor is required to filter the output voltage and provides regulator loop stability. The important capacitor parameters are the 100KHz Equivalent Series Resistance (ESR), the RMS ripples current rating, voltage rating and capacitance value. For the output capacitor, the ESR value is the most important parameter. The output ripple can be calculated from the following formula.

$$V_{RIPPLE} = \Delta I_L \times ESR$$

The bulk capacitor's ESR will determine the output ripple voltage and the initial voltage drop after a high slew-rate transient.

An aluminum electrolytic capacitor's ESR value is related to the capacitance and its voltage rating. In most case, higher voltage electrolytic capacitors have lower ESR values. Most of the time, capacitors with much higher voltage ratings may be needed to provide the low ESR values required for low output ripple voltage.

PCB Layout Guide
If you need low T_C & T_J or large PD (Power Dissipation), The dual SW pins(5& 6) and V_{SS} pins(7& 8)on the SOP-8L package are internally connected to die pad, The evaluation board should be allowed for maximum copper area at output (SW) pins.
1. Connect FB circuits (R_1, R_2, C_1) as closely as possible and keep away from inductor flux for pure V_{FB}.
2. Connect C3 to V_{CC} and V_{SS} pin as closely as possible to get good power filter effect.
3. Connect R4 to V_{CC} and OCSET pin as closely as possible.
4. Connect ground side of the C2 & D1 & C4 as closely as possible and use ground plane for best performance.

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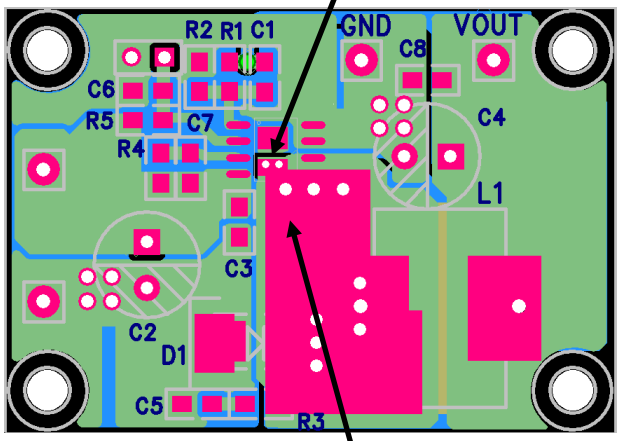
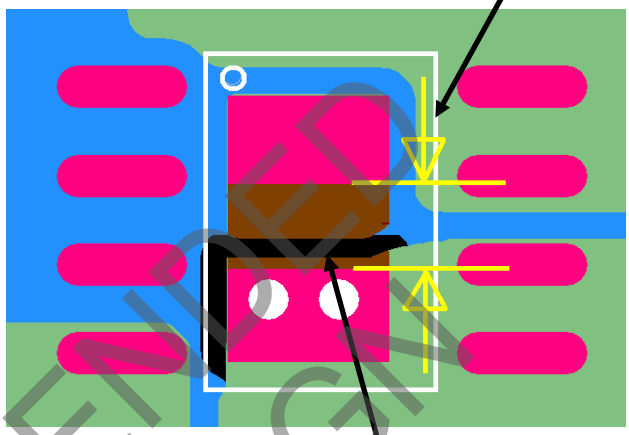
Functional Description (continued)

Keep the gap of exposed pads from short circuit.

Recommended exposed-pads gap: 30~40mil (0.75~1mm)

Top Side Layout Guide

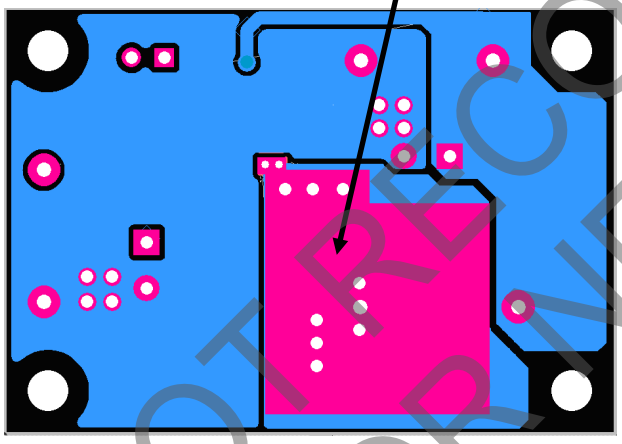




Use vias to conduct the heat into the backside of PCB layer. The heat sink at output (SW) pins should be allowed for maximum solder-painted area.

Brown: IC exposed pads.
Red: recommended layout.
Reference pads layout dimension:
Output: 90 x 50 mil
Vss: 90 x 60 mil

Bottom Side Layout Guide



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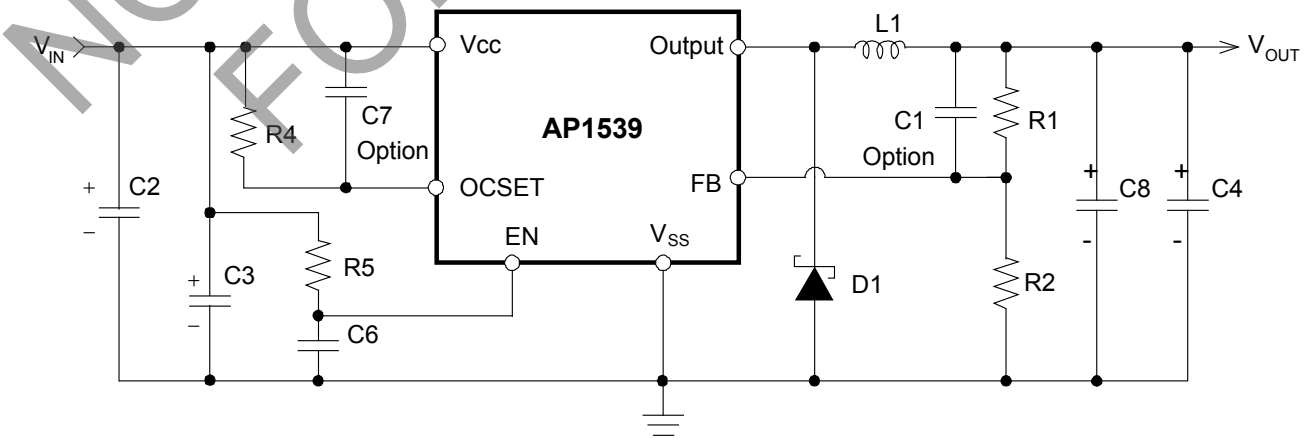

Layout numbering comparison

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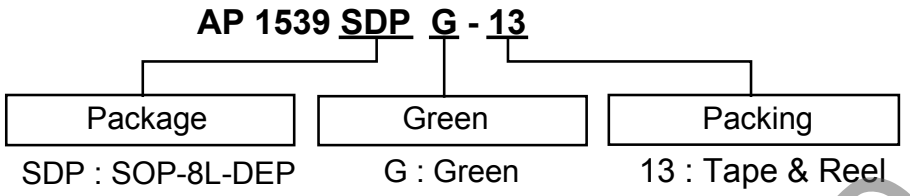
Ordering Information

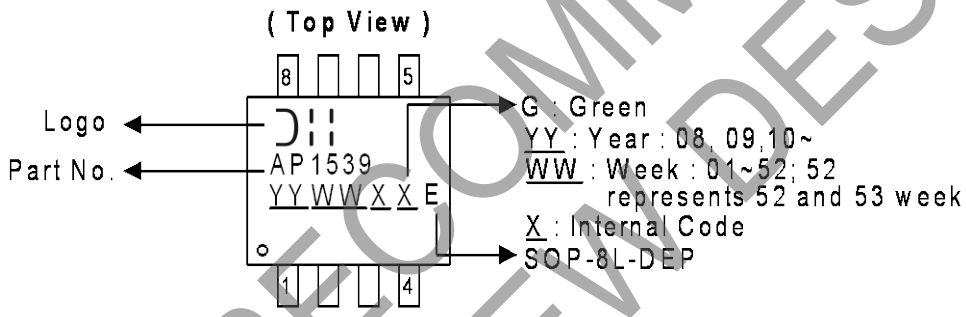


Device	Package Code	Packaging (Note 7)	13" Tape and Reel	
			Quantity	Part Number Suffix
AP1539SDPG-13	SDP	SOP-8L-DEP	2500/Tape & Reel	-13

Note: 7. Pad layout as shown as shown in Diodes Incorporated's package outline PDFs, which can be found on our website at http://www.diodes.com/package-outlines.html.

Marking Information

(1) SOP-8L-DEP



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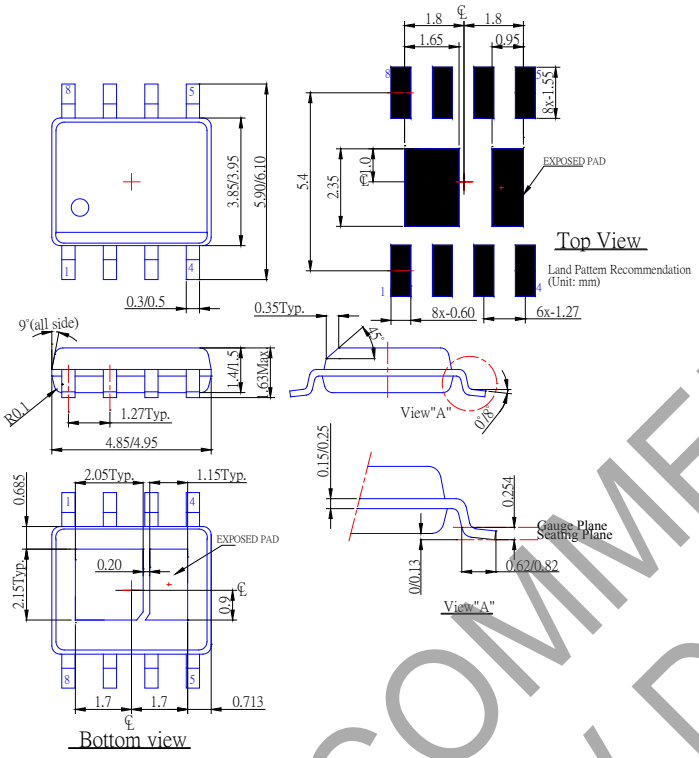
Package Outline Dimensions (All Dimensions in mm)

Please see http://www.diodes.com/package-outlines.html for the latest version.

(1) Package type: SOP-8L-DEP



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