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SPECIFICATIONS

ELECTRICAL SPECIFICATIONS—5 V OPERATION

All voltages are relative to their respective ground. $4.5\text{ V} \leq V_{DD1} \leq 5.5\text{ V}$, $4.5\text{ V} \leq V_{DD2} \leq 5.5\text{ V}$. All minimum/maximum specifications apply over the entire recommended operation range, unless otherwise noted. All typical specifications are at $T_A = 25^\circ\text{C}$, $V_{DD1} = V_{DD2} = 5\text{ V}$.

Table 1.

| Parameter | Symbol | Min | Typ | Max | Unit | Test Conditions |
|--|--|------------------------|-------|------|---------|---|
| DC SPECIFICATIONS | | | | | | |
| Input Supply Current | I _{DD1 (Q)} | | 0.3 | 0.8 | mA | V _I = 0 V or V _{DD1} |
| Output Supply Current | I _{DD2 (Q)} | | 0.01 | 0.06 | mA | V _I = 0 V or V _{DD1} |
| Input Supply Current (25 Mbps) (See Figure 5) | I _{DD1 (25)} | | 2.2 | 3.5 | mA | 12.5 MHz logic signal frequency |
| Output Supply Current ¹ (25 Mbps) (See Figure 6) | I _{DD2 (25)} | | 0.5 | 1.0 | mA | 12.5 MHz logic signal frequency |
| Input Supply Current (100 Mbps) (See Figure 5) | I _{DD1 (100)} | | 9.0 | 14 | mA | 50 MHz logic signal frequency, ADuM1100BR/ADuM1100UR only |
| Output Supply Current ¹ (100 Mbps) (See Figure 6) | I _{DD2 (100)} | | 2.0 | 2.8 | mA | 50 MHz logic signal frequency, ADuM1100BR/ADuM1100UR only |
| Input Current | I _I | −10 | +0.01 | +10 | μA | 0 V ≤ V _{IN} ≤ V _{DD1} |
| Logic High Output Voltage | V _{OH} | V _{DD2} − 0.1 | 5.0 | | V | I _O = −20 μA, V _I = V _{IH} |
| | | V _{DD2} − 0.8 | 4.6 | | V | I _O = −4 mA, V _I = V _{IH} |
| Logic Low Output Voltage | V _{OL} | | 0.0 | 0.1 | V | I _O = 20 μA, V _I = V _{IL} |
| | | | 0.03 | 0.1 | V | I _O = 400 μA, V _I = V _{IL} |
| | | | 0.3 | 0.8 | V | I _O = 4 mA, V _I = V _{IL} |
| SWITCHING SPECIFICATIONS | | | | | | |
| For ADuM1100AR | | | | | | |
| Minimum Pulse Width ² | PW | | | 40 | ns | C _L = 15 pF, CMOS signal levels |
| Maximum Data Rate ³ | | 25 | | | Mbps | C _L = 15 pF, CMOS signal levels |
| For ADuM1100BR/ADuM1100UR | | | | | | |
| Minimum Pulse Width ² | PW | | 6.7 | 10 | ns | C _L = 15 pF, CMOS signal levels |
| Maximum Data Rate ³ | | 100 | 150 | | Mbps | C _L = 15 pF, CMOS signal levels |
| For All Grades | | | | | | |
| Propagation Delay Time to Logic Low Output ^{4,5} (See Figure 7) | t _{PHL} | | 10.5 | 18 | ns | C _L = 15 pF, CMOS signal levels |
| Propagation Delay Time to Logic High Output ^{4,5} (See Figure 7) | t _{PLH} | | 10.5 | 18 | ns | C _L = 15 pF, CMOS signal levels |
| Pulse Width Distortion t _{PLH} − t _{PHL} ⁵ | PWD | | 0.5 | 2 | ns | C _L = 15 pF, CMOS signal levels |
| Change vs. Temperature ⁶ | | | 3 | | ps/°C | C _L = 15 pF, CMOS signal levels |
| Propagation Delay Skew (Equal Temperature) ^{5,7} | t _{PSK1} | | | 8 | ns | C _L = 15 pF, CMOS signal levels |
| Propagation Delay Skew (Equal Temperature, Supplies) ^{5,7} | t _{PSK2} | | | 6 | ns | C _L = 15 pF, CMOS signal levels |
| Output Rise/Fall Time | t _R , t _F | | 3 | | ns | C _L = 15 pF, CMOS signal levels |
| Common-Mode Transient Immunity at Logic Low/High Output ⁸ | C _{ML} , C _{MH} | 25 | 35 | | kV/μs | V _I = 0 V or V _{DD1} , V _{CM} = 1000 V, transient magnitude = 800 V |
| Refresh Rate | f _r | | 1.2 | | Mbps | |
| Input Dynamic Supply Current ⁹ | I _{DDI (D)} | | 0.09 | | mA/Mbps | |
| Output Dynamic Supply Current ⁹ | I _{DDO (D)} | | 0.02 | | mA/Mbps | |

- ¹ Output supply current values are with no output load present. See Figure 5 and Figure 6 for information on supply current variation with logic signal frequency. See the Power Consumption section for guidance on calculating the input and output supply currents for a given data rate and output load.
- ² The minimum pulse width is the shortest pulse width at which the specified pulse width distortion is guaranteed.
- ³ The maximum data rate is the fastest data rate at which the specified pulse width distortion is guaranteed.
- ⁴ t_{PHL} is measured from the 50% level of the falling edge of the V_i signal to the 50% level of the falling edge of the V_o signal. t_{PLH} is measured from the 50% level of the rising edge of the V_i signal to the 50% level of the rising edge of the V_o signal.
- ⁵ Because the input thresholds of the ADuM1100 are at voltages other than the 50% level of typical input signals, the measured propagation delay and pulse width distortion can be affected by slow input rise/fall times. See the Propagation Delay-Related Parameters section and Figure 14 through Figure 18 for information on the impact of given input rise/fall times on these parameters.
- ⁶ Pulse width distortion change vs. temperature is the absolute value of the change in pulse width distortion for a 1°C change in operating temperature.
- ⁷ t_{PSK1} is the magnitude of the worst-case difference in t_{PHL} and/or t_{PLH} that is measured between units at the same operating temperature and output load within the recommended operating conditions. t_{PSK2} is the magnitude of the worst-case difference in t_{PHL} and/or t_{PLH} that is measured between units at the same operating temperature, supply voltages, and output load within the recommended operating conditions.
- ⁸ CM_H is the maximum common-mode voltage slew rate that can be sustained while maintaining $V_o > 0.8 V_{DD2}$. CM_L is the maximum common-mode voltage slew rate that can be sustained while maintaining $V_o < 0.8 V$. The common-mode voltage slew rates apply to both rising and falling edges. The transient magnitude is the range over which the common mode is slewed.
- ⁹ Dynamic supply current is the incremental amount of supply current required for a 1 Mbps increase in signal data rate. See Figure 5 and Figure 6 for information on supply current variation with logic signal frequency. See the Power Consumption section for guidance on calculating the input and output supply currents for a given data rate and output load.

ELECTRICAL SPECIFICATIONS—3.3 V OPERATION

All voltages are relative to their respective ground. $3.0\text{ V} \leq V_{DD1} \leq 3.6\text{ V}$, $3.0\text{ V} \leq V_{DD2} \leq 3.6\text{ V}$. All minimum/maximum specifications apply over the entire recommended operation range, unless otherwise noted. All typical specifications are at $T_A = 25^\circ\text{C}$, $V_{DD1} = V_{DD2} = 3.3\text{ V}$.

Table 2.

| Parameter | Symbol | Min | Typ | Max | Unit | Test Conditions |
|--|------------------------|-----------------|-------|------|-------------------|---|
| DC SPECIFICATIONS | | | | | | |
| Input Supply Current | $I_{DD1(Q)}$ | | 0.1 | 0.3 | mA | $V_I = 0\text{ V}$ or V_{DD1} |
| Output Supply Current | $I_{DD2(Q)}$ | | 0.005 | 0.04 | mA | $V_I = 0\text{ V}$ or V_{DD1} |
| Input Supply Current (25 Mbps) (See Figure 5) | $I_{DD1(25)}$ | | 2.0 | 2.8 | mA | 12.5 MHz logic signal frequency |
| Output Supply Current ¹ (25 Mbps) (See Figure 6) | $I_{DD2(25)}$ | | 0.3 | 0.7 | mA | 12.5 MHz logic signal frequency |
| Input Supply Current (50 Mbps) (See Figure 5) | $I_{DD1(50)}$ | | 4.0 | 6.0 | mA | 25 MHz logic signal frequency, ADuM1100BR/ADuM1100UR only |
| Output Supply Current ¹ (50 Mbps) (See Figure 6) | $I_{DD2(50)}$ | | 1.2 | 1.6 | mA | 25 MHz logic signal frequency, ADuM1100BR/ADuM1100UR only |
| Input Current | I_I | -10 | +0.01 | +10 | μA | $0\text{ V} \leq V_{IN} \leq V_{DD1}$ |
| Logic High Output Voltage | V_{OH} | $V_{DD2} - 0.1$ | 3.3 | | V | $I_O = -20\text{ }\mu\text{A}$, $V_I = V_{IH}$ |
| | | $V_{DD2} - 0.5$ | 3.0 | | V | $I_O = -2.5\text{ mA}$, $V_I = V_{IH}$ |
| Logic Low Output Voltage | V_{OL} | | 0.0 | 0.1 | V | $I_O = 20\text{ }\mu\text{A}$, $V_I = V_{IL}$ |
| | | | 0.04 | 0.1 | V | $I_O = 400\text{ }\mu\text{A}$, $V_I = V_{IL}$ |
| | | | 0.3 | 0.4 | V | $I_O = 2.5\text{ mA}$, $V_I = V_{IL}$ |
| | | | | | | |
| SWITCHING SPECIFICATIONS | | | | | | |
| For ADuM1100AR | | | | | | |
| Minimum Pulse Width ² | PW | 25 | | 40 | ns | $C_L = 15\text{ pF}$, CMOS signal levels |
| Maximum Data Rate ³ | | | | | Mbps | $C_L = 15\text{ pF}$, CMOS signal levels |
| For ADuM1100BR/ADuM1100UR | | | | | | |
| Minimum Pulse Width ² | PW | 50 | 10 | 20 | ns | $C_L = 15\text{ pF}$, CMOS signal levels |
| Maximum Data Rate ³ | | | 100 | | Mbps | $C_L = 15\text{ pF}$, CMOS signal levels |
| For All Grades | | | | | | |
| Propagation Delay Time to Logic Low Output ^{4,5} (See Figure 8) | t_{PHL} | | 14.5 | 28 | ns | $C_L = 15\text{ pF}$, CMOS signal levels |
| Propagation Delay Time to Logic High Output ^{4,5} (See Figure 8) | t_{PLH} | | 15.0 | 28 | ns | $C_L = 15\text{ pF}$, CMOS signal levels |
| Pulse Width Distortion $ t_{PLH} - t_{PHL} $ ⁵ | PWD | | 0.5 | 3 | ns | $C_L = 15\text{ pF}$, CMOS signal levels |
| Change vs. Temperature ⁶ | | | 10 | | ps/°C | $C_L = 15\text{ pF}$, CMOS signal levels |
| Propagation Delay Skew (Equal Temperature) ^{5,7} | t_{PSK1} | | | 15 | ns | $C_L = 15\text{ pF}$, CMOS signal levels |
| Propagation Delay Skew (Equal Temperature, Supplies) ^{5,7} | t_{PSK2} | | | 12 | ns | $C_L = 15\text{ pF}$, CMOS signal levels |
| Output Rise/Fall Time | t_R, t_F | | 3 | | ns | $C_L = 15\text{ pF}$, CMOS signal levels |
| Common-Mode Transient Immunity at Logic Low/High Output ⁸ | $ CM_L $, $ CM_H $ | 25 | 35 | | kV/ μs | $V_I = 0\text{ V}$ or V_{DD1} , $V_{CM} = 1000\text{ V}$, transient magnitude = 800 V |
| Refresh Rate | f_r | | 1.1 | | Mbps | |
| Input Dynamic Supply Current ⁹ | $I_{DDI(D)}$ | | 0.08 | | mA/Mbps | |
| Output Dynamic Supply Current ⁹ | $I_{DDO(D)}$ | | 0.04 | | mA/Mbps | |

- ¹ Output supply current values are with no output load present. See Figure 5 and Figure 6 for information on supply current variation with logic signal frequency. See the Power Consumption section for guidance on calculating the input and output supply currents for a given data rate and output load.
- ² The minimum pulse width is the shortest pulse width at which the specified pulse width distortion is guaranteed.
- ³ The maximum data rate is the fastest data rate at which the specified pulse width distortion is guaranteed.
- ⁴ t_{PHL} is measured from the 50% level of the falling edge of the V_i signal to the 50% level of the falling edge of the V_o signal. t_{PLH} is measured from the 50% level of the rising edge of the V_i signal to the 50% level of the rising edge of the V_o signal.
- ⁵ Because the input thresholds of the ADuM1100 are at voltages other than the 50% level of typical input signals, the measured propagation delay and pulse width distortion can be affected by slow input rise/fall times. See the Propagation Delay-Related Parameters section and Figure 14 through Figure 18 for information on the impact of given input rise/fall times on these parameters.
- ⁶ Pulse width distortion change vs. temperature is the absolute value of the change in pulse width distortion for a 1°C change in operating temperature.
- ⁷ t_{PSK1} is the magnitude of the worst-case difference in t_{PHL} and/or t_{PLH} that is measured between units at the same operating temperature and output load within the recommended operating conditions. t_{PSK2} is the magnitude of the worst-case difference in t_{PHL} and/or t_{PLH} that is measured between units at the same operating temperature, supply voltages, and output load within the recommended operating conditions.
- ⁸ CM_H is the maximum common-mode voltage slew rate that can be sustained while maintaining $V_o > 0.8 V_{DD2}$. CM_L is the maximum common-mode voltage slew rate that can be sustained while maintaining $V_o < 0.8 V$. The common-mode voltage slew rates apply to both rising and falling edges. The transient magnitude is the range over which the common mode is slewed.
- ⁹ Dynamic supply current is the incremental amount of supply current required for a 1 Mbps increase in signal data rate. See Figure 5 and Figure 6 for information on supply current variation with logic signal frequency. See the Power Consumption section for guidance on calculating the input and output supply currents for a given data rate and output load.

ELECTRICAL SPECIFICATIONS—MIXED 5 V/3 V OR 3 V/5 V OPERATION

All voltages are relative to their respective ground. 5 V/3 V operation: $4.5\text{ V} \leq V_{DD1} \leq 5.5\text{ V}$, $3.0\text{ V} \leq V_{DD2} \leq 3.6\text{ V}$. 3 V/5 V operation: $3.0\text{ V} \leq V_{DD1} \leq 3.6\text{ V}$, $4.5\text{ V} \leq V_{DD2} \leq 5.5\text{ V}$. All minimum/maximum specifications apply over the entire recommended operation range, unless otherwise noted. All typical specifications are at $T_A = 25^\circ\text{C}$, $V_{DD1} = 3.3\text{ V}$, $V_{DD2} = 5\text{ V}$ or $V_{DD1} = 5\text{ V}$, $V_{DD2} = 3.3\text{ V}$.

Table 3.

| Parameter | Symbol | Min | Typ | Max | Unit | Test Conditions |
|--|--------------------|-----------------|-------|------|---------------|---|
| DC SPECIFICATIONS | | | | | | |
| Input Supply Current, Quiescent | $I_{DD1(Q)}$ | | | | | |
| 5 V/3 V Operation | | | 0.3 | 0.8 | mA | |
| 3 V/5 V Operation | | | 0.1 | 0.3 | mA | |
| Output Supply Current, Quiescent | $I_{DDO(Q)}$ | | | | | |
| 5 V/3 V Operation | | | 0.005 | 0.04 | mA | |
| 3 V/5 V Operation | | | 0.01 | 0.06 | mA | |
| Input Supply Current, 25 Mbps | $I_{DD1(25)}$ | | | | | |
| 5 V/3 V Operation | | | 2.2 | 3.5 | mA | 12.5 MHz logic signal frequency |
| 3 V/5 V Operation | | | 2.0 | 2.8 | mA | 12.5 MHz logic signal frequency |
| Output Supply Current ¹ , 25 Mbps | $I_{DDO(25)}$ | | | | | |
| 5 V/3 V Operation | | | 0.3 | 0.7 | mA | 12.5 MHz logic signal frequency |
| 3 V/5 V Operation | | | 0.5 | 1.0 | mA | 12.5 MHz logic signal frequency |
| Input Supply Current, 50 Mbps | $I_{DD1(50)}$ | | | | | |
| 5 V/3 V Operation | | | 4.5 | 7.0 | mA | 25 MHz logic signal frequency |
| 3 V/5 V Operation | | | 4.0 | 6.0 | mA | 25 MHz logic signal frequency |
| Output Supply Current ¹ , 50 Mbps | $I_{DDO(50)}$ | | | | | |
| 5 V/3 V Operation | | | 1.2 | 1.6 | mA | 25 MHz logic signal frequency |
| 3 V/5 V Operation | | | 1.0 | 1.5 | mA | 25 MHz logic signal frequency |
| Input Currents | I_{IA} | -10 | +0.01 | +10 | μA | $0\text{ V} \leq V_{IA}, V_{IB}, V_{IC}, V_{ID} \leq V_{DD1} \text{ or } V_{DD2}$ |
| Logic High Output Voltage | V_{OH} | $V_{DD2} - 0.1$ | 3.3 | | V | $I_O = -20\text{ }\mu\text{A}$, $V_I = V_{IH}$ |
| 5 V/3 V Operation | | $V_{DD2} - 0.5$ | 3.0 | | V | $I_O = -2.5\text{ mA}$, $V_I = V_{IH}$ |
| Logic Low Output Voltage | V_{OL} | | 0.0 | 0.1 | V | $I_O = 20\text{ }\mu\text{A}$, $V_I = V_{IL}$ |
| 5 V/3 V Operation | | | 0.04 | 0.1 | V | $I_O = 400\text{ }\mu\text{A}$, $V_I = V_{IL}$ |
| | | | 0.3 | 0.4 | V | $I_O = 2.5\text{ mA}$, $V_I = V_{IL}$ |
| Logic High Output Voltage | V_{OH} | $V_{DD2} - 0.1$ | 5.0 | | V | $I_O = -20\text{ }\mu\text{A}$, $V_I = V_{IH}$ |
| 3 V/5 V Operation | | $V_{DD2} - 0.8$ | 4.6 | | V | $I_O = -4\text{ mA}$, $V_I = V_{IH}$ |
| Logic Low Output Voltage | V_{OL} | | 0.0 | 0.1 | V | $I_O = 20\text{ }\mu\text{A}$, $V_I = V_{IL}$ |
| 3 V/5 V Operation | | | 0.03 | 0.1 | V | $I_O = 400\text{ }\mu\text{A}$, $V_I = V_{IL}$ |
| | | | 0.3 | 0.8 | V | $I_O = 4\text{ mA}$, $V_I = V_{IL}$ |
| SWITCHING SPECIFICATIONS | | | | | | |
| For ADuM1100AR | | | | | | |
| Minimum Pulse Width ² | PW | | | 40 | ns | $C_L = 15\text{ pF}$, CMOS signal levels |
| Maximum Data Rate ³ | | 25 | | | Mbps | $C_L = 15\text{ pF}$, CMOS signal levels |
| For ADuM1100BR/ADuM1100UR | | | | | | |
| Minimum Pulse Width ² | PW | | | 20 | ns | $C_L = 15\text{ pF}$, CMOS signal levels |
| Maximum Data Rate ³ | | 50 | | | Mbps | $C_L = 15\text{ pF}$, CMOS signal levels |
| For All Grades | | | | | | |
| Propagation Delay Time to Logic Low/High Output ^{4,5} | t_{PHL}, t_{PLH} | | | | | |
| 5 V/3 V Operation (See Figure 9) | | | 13 | 21 | ns | $C_L = 15\text{ pF}$, CMOS signal levels |
| 3 V/5 V Operation (See Figure 10) | | | 16 | 26 | ns | $C_L = 15\text{ pF}$, CMOS signal levels |

| Parameter | Symbol | Min | Typ | Max | Unit | Test Conditions |
|--|-------------------------------------|-----|------|-----|---------|--|
| Pulse Width Distortion, $ t_{PLH} - t_{PHL} $ ⁵ | PWD | | | | | |
| 5 V/3 V Operation | | | 0.5 | 2 | ns | C _L = 15 pF, CMOS signal levels |
| 3 V/5 V Operation | | | 0.5 | 3 | ns | C _L = 15 pF, CMOS signal levels |
| Change in Pulse Width Distortion vs. Temperature ⁶ | | | | | | |
| 5 V/3 V Operation | | | 3 | | ps/°C | C _L = 15 pF, CMOS signal levels |
| 3 V/5 V Operation | | | 10 | | ps/°C | C _L = 15 pF, CMOS signal levels |
| Propagation Delay Skew (Equal Temperature) ^{5,7} | t _{PSK1} | | | | | |
| 5 V/3 V Operation | | | | 12 | ns | C _L = 15 pF, CMOS signal levels |
| 3 V/5 V Operation | | | | 15 | ns | C _L = 15 pF, CMOS signal levels |
| Propagation Delay Skew (Equal Temperature, Supplies) ^{5,7} | t _{PSK2} | | | | | |
| 5 V/3 V Operation | | | | 9 | ns | C _L = 15 pF, CMOS signal levels |
| 3 V/5 V Operation | | | | 12 | ns | C _L = 15 pF, CMOS signal levels |
| Output Rise/Fall Time (10% to 90%) | t _R , t _F | | 3 | | ns | C _L = 15 pF, CMOS signal levels |
| Common-Mode Transient Immunity at Logic Low/High Output ⁸ | CM _L , CM _H | 25 | 35 | | kV/μs | V _I = 0 V or V _{DD1} , V _{CM} = 1000 V, transient magnitude = 800 V |
| Refresh Rate | f _r | | | | | |
| 5 V/3 V Operation | | | 1.2 | | Mbps | |
| 3 V/5 V Operation | | | 1.1 | | Mbps | |
| Input Dynamic Supply Current ⁹ | C _{PD1} | | | | | |
| 5 V/3 V Operation | | | 0.09 | | mA/Mbps | |
| 3 V/5 V Operation | | | 0.08 | | mA/Mbps | |
| Output Dynamic Supply Current ⁹ | C _{PD2} | | | | | |
| 5 V/3 V Operation | | | 0.04 | | mA/Mbps | |
| 3 V/5 V Operation | | | 0.02 | | mA/Mbps | |

¹ Output supply current values are with no output load present. See Figure 5 and Figure 6 for information on supply current variation with logic signal frequency. See the Power Consumption section for guidance on calculating the input and output supply currents for a given data rate and output load.

² The minimum pulse width is the shortest pulse width at which the specified pulse width distortion is guaranteed.

³ The maximum data rate is the fastest data rate at which the specified pulse width distortion is guaranteed.

⁴ t_{PHL} is measured from the 50% level of the falling edge of the V_I signal to the 50% level of the falling edge of the V_O signal. t_{PLH} is measured from the 50% level of the rising edge of the V_I signal to the 50% level of the rising edge of the V_O signal.

⁵ Because the input thresholds of the ADuM1100 are at voltages other than the 50% level of typical input signals, the measured propagation delay and pulse width distortion can be affected by slow input rise/fall times. See the Propagation Delay-Related Parameters section and Figure 14 through Figure 18 for information on the impact of given input rise/fall times on these parameters.

⁶ Pulse width distortion change vs. temperature is the absolute value of the change in pulse width distortion for a 1°C change in operating temperature.

⁷ t_{PSK1} is the magnitude of the worst-case difference in t_{PHL} and/or t_{PLH} that is measured between units at the same operating temperature and output load within the recommended operating conditions. t_{PSK2} is the magnitude of the worst-case difference in t_{PHL} and/or t_{PLH} that is measured between units at the same operating temperature, supply voltages, and output load within the recommended operating conditions.

⁸ CM_H is the maximum common-mode voltage slew rate that can be sustained while maintaining V_O > 0.8 V_{DD2}. CM_L is the maximum common-mode voltage slew rate that can be sustained while maintaining V_O < 0.8 V. The common-mode voltage slew rates apply to both rising and falling edges. The transient magnitude is the range over which the common mode is slewed.

⁹ Dynamic supply current is the incremental amount of supply current required for a 1 Mbps increase in signal data rate. See Figure 5 and Figure 6 for information on supply current variation with logic signal frequency. See the Power Consumption section for guidance on calculating the input and output supply currents for a given data rate and output load.

PACKAGE CHARACTERISTICS

Table 4.

| Parameter | Symbol | Min | Typ | Max | Unit | Test Conditions |
|--|------------------|-----|------------------|-----|------|---|
| Resistance (Input-to-Output) ¹ | R _{I-O} | | 10 ¹² | | Ω | f = 1 MHz |
| Capacitance (Input-to-Output) ¹ | C _{I-O} | | 1.0 | | pF | |
| Input Capacitance ² | C _I | | 4.0 | | pF | |
| IC Junction-to-Case Thermal Resistance, Side 1 | θ _{JCI} | | 46 | | °C/W | Thermocouple located at center of package underside |
| IC Junction-to-Case Thermal Resistance, Side 2 | θ _{JCO} | | 41 | | °C/W | |
| Package Power Dissipation | P _{PD} | | | 240 | mW | |

¹ The device is considered a 2-terminal device; Pin 1, Pin 2, Pin 3, and Pin 4 are shorted together, and Pin 5, Pin 6, Pin 7, and Pin 8 are shorted together.

² Input capacitance is measured at Pin 2 (V_I).

REGULATORY INFORMATION

The ADuM1100 is approved by the following organizations.

Table 5.

| UL | CSA | CQC | VDE |
|--|---|---|---|
| Recognized Under 1577 Component Recognition Program ¹ | Approved under CSA Component Acceptance Notice 5A | Approved under CQC11-471543-2012 | Certified according to DIN V VDE V 0884-10 (VDE V 0884-10):2006-12 ² |
| Single/Basic Insulation, 2500 V rms Isolation Voltage | Basic insulation per CSA 60950-1-03 and IEC 60950-1, 400 V rms (565 V peak) maximum working voltage | Basic insulation per GB4943.1-2011 400 V rms (588 V peak) maximum working voltage, tropical climate, altitude ≤ 5000 meters | Reinforced insulation, 560 V peak |
| File E214100 | File 205078 | File CQC14001117247 | File 2471900-4880-0001 |

¹ In accordance with UL 1577, each ADuM1100 is proof tested by applying an insulation test voltage ≥3000 V rms for 1 sec (current leakage detection limit = 5 μA).

² In accordance with DIN V VDE V 0884-10, each ADuM1100 is proof tested by applying an insulation test voltage ≥1050 V peak for 1 sec (partial discharge detection limit = 5 pC). The * marking branded on the component designates DIN V VDE V 0884-10 approval.

INSULATION AND SAFETY-RELATED SPECIFICATIONS

Table 6.

| Parameter | Symbol | Value | Unit | Conditions |
|---|-------------------|-----------|--------|--|
| Minimum External Air Gap (Clearance) | L(I01) | 4.90 min | mm | Measured from input terminals to output terminals, shortest distance through air |
| Minimum External Tracking (Creepage) | L(I02) | 4.01 min | mm | Measured from input terminals to output terminals, shortest distance path along body |
| Minimum Internal Gap (Internal Clearance) | | 0.016 min | mm | Insulation distance through insulation |
| Tracking Resistance (Comparative Tracking Index) | CTI | >400 | V | DIN IEC 112/VDE 0303 Part 1 |
| Isolation Group | | II | | Material Group (DIN VDE 0110, 1/89, Table I) |
| Maximum Working Voltage Compatible with 50 Years Service Life | V _{IORM} | 565 | V peak | Continuous peak voltage across the isolation barrier |

DIN V VDE V 0884-10 (VDE V 0884-10):2006-12 INSULATION CHARACTERISTICS

This isolator is suitable for reinforced isolation only within the safety limit data. Maintenance of the safety data is ensured by means of protective circuits. The asterisk (*) marking on the package denotes DIN V VDE V 0884-10 approval for 560 V peak working voltage.

Table 7.

| Description | Conditions | Symbol | Characteristic | Unit |
|---|---|------------|--------------------------------|--------|
| Installation Classification per DIN VDE 0110 For Rated Mains Voltage ≤ 150 V rms For Rated Mains Voltage ≤ 300 V rms For Rated Mains Voltage ≤ 400 V rms | | | I to IV I to III I to II | |
| Climatic Classification | | | 40/105/21 | |
| Pollution Degree per DIN VDE 0110, Table 1 | | | 2 | |
| Maximum Working Insulation Voltage | $V_{IORM} \times 1.875 = V_{PR}$, 100% production test, $t_m = 1$ sec, partial discharge < 5 pC | V_{IORM} | 560 | V peak |
| Input-to-Output Test Voltage, Method B1 | | V_{PR} | 1050 | V peak |
| Input-to-Output Test Voltage, Method A | $V_{IORM} \times 1.6 = V_{PR}$, $t_m = 60$ sec, partial discharge < 5 pC | V_{PR} | | |
| After Environmental Tests Subgroup 1 | | | 896 | V peak |
| After Input and/or Safety Test Subgroup 2 and Subgroup 3 | $V_{IORM} \times 1.2 = V_{PR}$, $t_m = 60$ sec, partial discharge < 5 pC | | 672 | V peak |
| Highest Allowable Overvoltage | Transient overvoltage, $t_{TR} = 10$ seconds | V_{TR} | 4000 | V peak |
| Safety-Limiting Values | Maximum value allowed in the event of a failure (see Figure 2) | | | |
| Case Temperature | | T_s | 150 | °C |
| Side 1 Current | | I_{S1} | 160 | mA |
| Side 2 Current | | I_{S2} | 170 | mA |
| Insulation Resistance at T_s | $V_{IO} = 500$ V | R_s | >10 ⁹ | Ω |

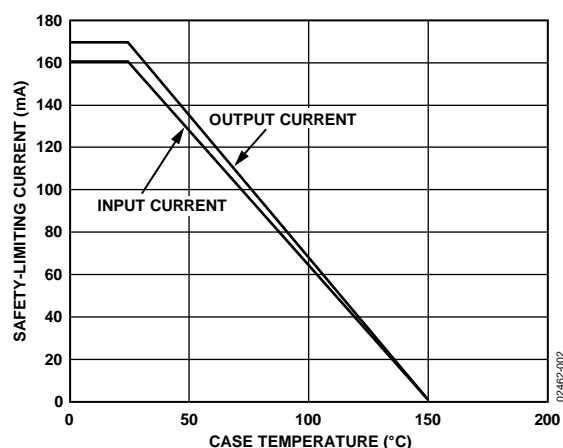


Figure 2. Thermal Derating Curve, Dependence of Safety-Limiting Values with Case Temperature per DIN V VDE V 0884-10

RECOMMENDED OPERATING CONDITIONS**Table 8.**

| Parameter | Symbol | Min | Max | Unit |
|--|--------------------------|-----|-----------|------|
| Operating Temperature | | | | |
| ADuM1100AR/ADuM1100BR | T_A | -40 | +105 | °C |
| ADuM1100UR | T_A | -40 | +125 | °C |
| Supply Voltages ¹ | V_{DD1} , V_{DD2} | 3.0 | 5.5 | V |
| Logic High Input Voltage, 5 V Operation ^{1,2} (See Figure 11 and Figure 12) | V_{IH} | 2.0 | V_{DD1} | V |
| Logic Low Input Voltage, 5 V Operation ^{1,2} (See Figure 11 and Figure 12) | V_{IL} | 0.0 | 0.8 | V |
| Logic High Input Voltage, 3.3 V Operation ^{1,2} (See Figure 11 and Figure 12) | V_{IH} | 1.5 | V_{DD1} | V |
| Logic Low Input Voltage, 3.3 V Operation ^{1,2} (See Figure 11 and Figure 12) | V_{IL} | 0.0 | 0.5 | V |
| Input Signal Rise and Fall Times | | | 1.0 | ms |

¹ All voltages are relative to their respective ground.

² Input switching thresholds have 300 mV of hysteresis. See the Method of Operation, DC Correctness, and Magnetic Field Immunity section, Figure 19, and Figure 20 for information on immunity to external magnetic fields.

ABSOLUTE MAXIMUM RATINGS

Table 9.

| Parameter | Symbol | Min | Max | Unit |
|---------------------------------------|-------------------------------------|------|------------------------|-------|
| Storage Temperature | T _{ST} | −55 | +150 | °C |
| Ambient Operating Temperature | T _A | −40 | +125 | °C |
| Supply Voltages ¹ | V _{DD1} , V _{DD2} | −0.5 | +6.5 | V |
| Input Voltage ¹ | V _I | −0.5 | V _{DD1} + 0.5 | V |
| Output Voltage ¹ | V _O | −0.5 | V _{DD2} + 0.5 | V |
| Average Current, per Pin ² | | | | |
| Temperature ≤ 105°C | | −25 | +25 | mA |
| Temperature ≤ 125°C | | | | |
| Input Current | | −7 | +7 | mA |
| Output Current | | −20 | +20 | mA |
| Common-Mode Transients ³ | | −100 | +100 | kV/μs |

¹ All voltages are relative to their respective ground.

² See Figure 2 for information on maximum allowable current for various temperatures.

³ Refers to common-mode transients across the insulation barrier. Common-mode transients exceeding the Absolute Maximum Rating may cause latch-up or permanent damage.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

Table 10. Truth Table (Positive Logic)

| V _I Input | V _{DD1} State | V _{DD2} State | V _O Output |
|----------------------|------------------------|------------------------|-----------------------|
| H | Powered | Powered | H |
| L | Powered | Powered | L |
| X | Unpowered | Powered | H ¹ |
| X | Powered | Unpowered | X ¹ |

¹ V_O returns to V_I state within 1 μs of power restoration.

Figure 3 shows the package branding. The asterisk (*) is the DIN EN 60747-5-2 mark, R is the package designator (R denotes SOIC_N), YYWW is the date code, and XXXXXX is the lot code.

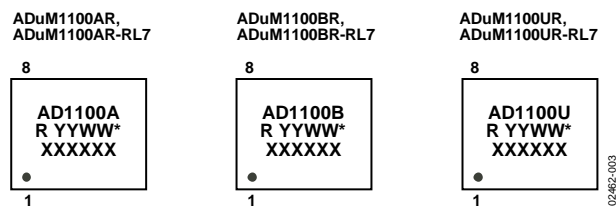


Figure 3. Package Branding

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

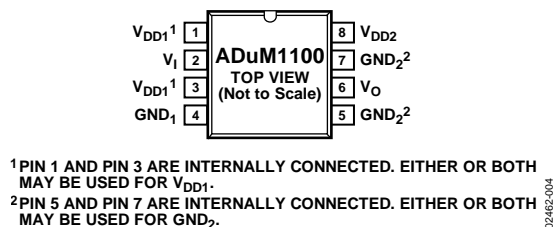


Figure 4. Pin Configuration

Table 11. Pin Function Descriptions

| Pin No. | Mnemonic | Description |
|---------|-----------|--|
| 1 | V_{DD1} | Input Supply Voltage, 3.0 V to 5.5 V. |
| 2 | V_I | Logic Input. |
| 3 | V_{DD1} | Input Supply Voltage, 3.0 V to 5.5 V. |
| 4 | GND_1 | Input Ground Reference. |
| 5 | GND_2 | Output Ground Reference. |
| 6 | V_O | Logic Output. |
| 7 | GND_2 | Output Ground Reference. |
| 8 | V_{DD2} | Output Supply Voltage, 3.0 V to 5.5 V. |

TYPICAL PERFORMANCE CHARACTERISTICS

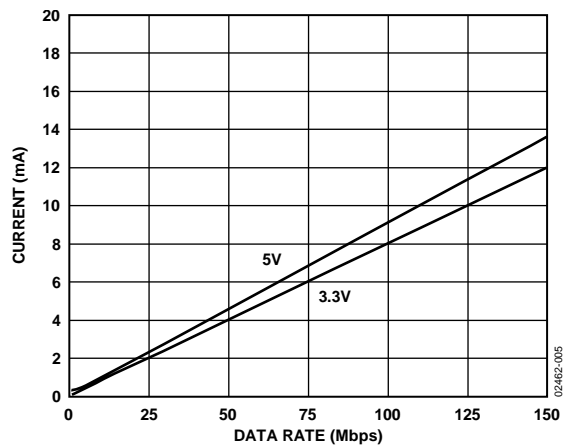


Figure 5. Typical Input Supply Current vs. Logic Signal Frequency for 5 V and 3.3 V Operation

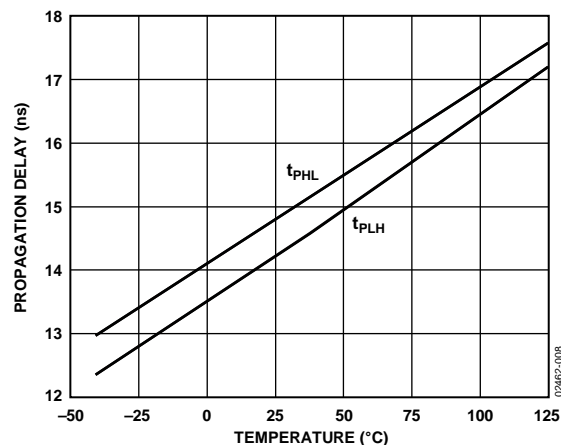


Figure 8. Typical Propagation Delays vs. Temperature, 3.3 V Operation

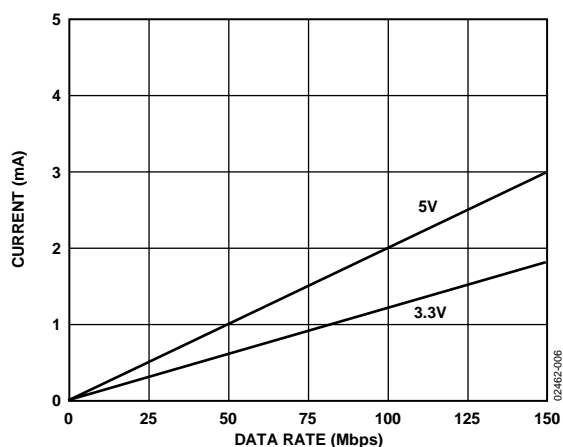


Figure 6. Typical Output Supply Current vs. Logic Signal Frequency for 5 V and 3.3 V Operation

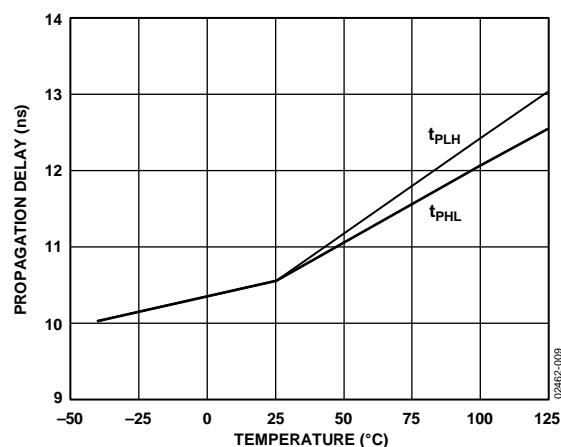


Figure 9. Typical Propagation Delays vs. Temperature, 5 V/3 V Operation

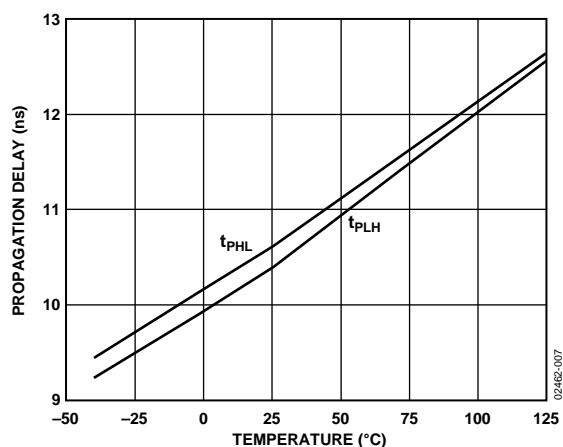


Figure 7. Typical Propagation Delays vs. Temperature, 5 V Operation

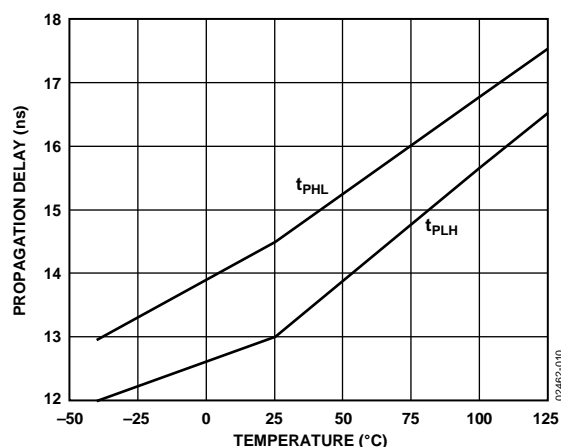


Figure 10. Typical Propagation Delays vs. Temperature, 3 V/5 V Operation

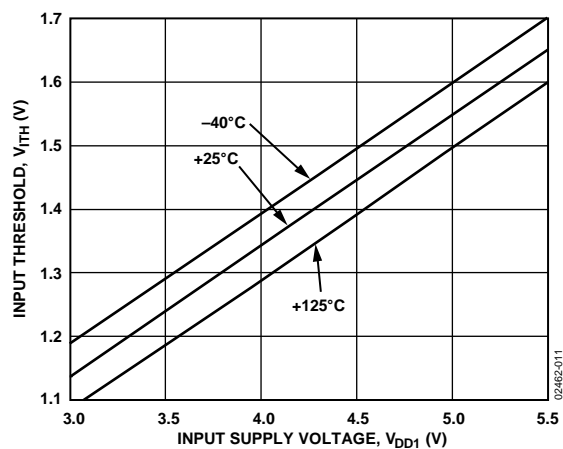


Figure 11. Typical Input Voltage Switching Threshold, Low-to-High Transition

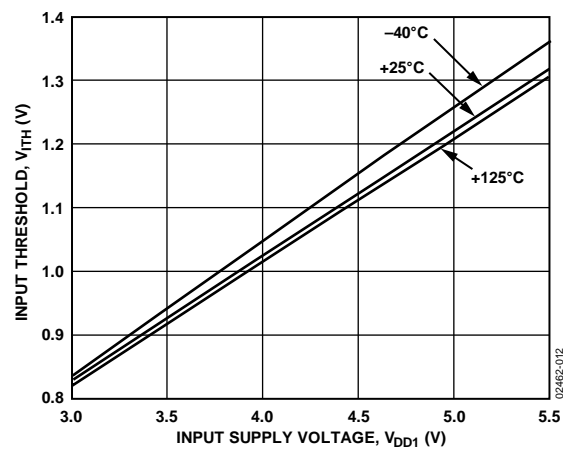


Figure 12. Typical Input Voltage Switching Threshold, High-to-Low Transition

APPLICATION INFORMATION

PC BOARD LAYOUT

The ADuM1100 digital isolator requires no external interface circuitry for the logic interfaces. A bypass capacitor is recommended at the input and output supply pins. The input bypass capacitor can conveniently be connected between Pin 3 and Pin 4 (see Figure 13). Alternatively, the bypass capacitor can be located between Pin 1 and Pin 4. The output bypass capacitor can be connected between Pin 7 and Pin 8 or Pin 5 and Pin 8. The capacitor value should be between 0.01 μF and 0.1 μF . The total lead length between both ends of the capacitor and the power supply pins should not exceed 20 mm.

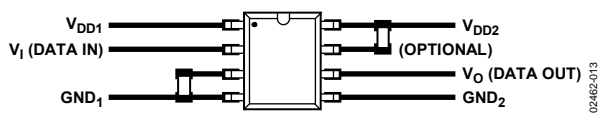


Figure 13. Recommended Printed Circuit Board Layout

See the [AN-1109 Application Note](#) for board layout guidelines.

PROPAGATION DELAY-RELATED PARAMETERS

Propagation delay time describes the length of time it takes for a logic signal to propagate through a component. Propagation delay time to logic low output and propagation delay time to logic high output refer to the duration between an input signal transition and the respective output signal transition (see Figure 14).

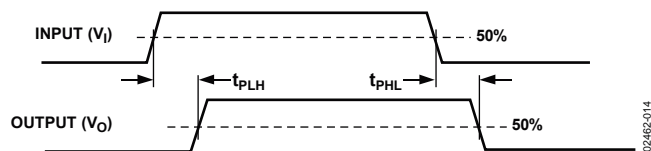


Figure 14. Propagation Delay Parameters

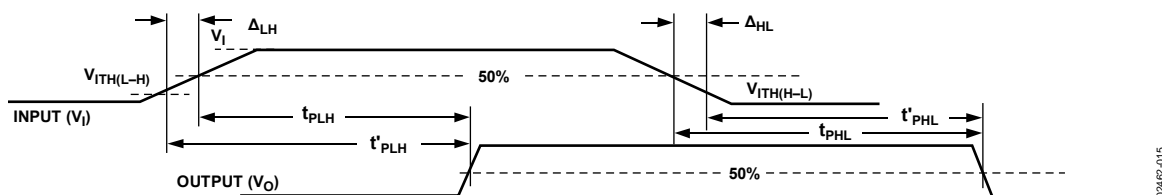


Figure 15. Impact of Input Rise/Fall Time on Propagation Delay

Pulse width distortion is the maximum difference between t_{PLH} and t_{PHL} and provides an indication of how accurately the input signal's timing is preserved in the component's output signal. Propagation delay skew is the difference between the minimum and maximum propagation delay values among multiple ADuM1100 components operated at the same operating temperature and having the same output load.

Depending on the input signal rise/fall time, the measured propagation delay based on the input 50% level can vary from the true propagation delay of the component (as measured from its input switching threshold). This is because the input threshold, as is the case with commonly used optocouplers, is at a different voltage level than the 50% point of typical input signals. This propagation delay difference is given by

$$\Delta_{LH} = t'_{PLH} - t_{PLH} = (t_R/0.8 V_I)(0.5 V_I - V_{ITH(L-H)})$$

$$\Delta_{HL} = t'_{PHL} - t_{PHL} = (t_F/0.8 V_I)(0.5 V_I - V_{ITH(H-L)})$$

where:

t_{PLH} and t_{PHL} are the propagation delays as measured from the input 50% level.

t'_{PLH} and t'_{PHL} are the propagation delays as measured from the input switching thresholds.

t_R and t_F are the input 10% to 90% rise/fall times.

V_I is the amplitude of the input signal (0 V to V_I levels assumed).

$V_{ITH(L-H)}$ and $V_{ITH(H-L)}$ are the input switching thresholds.

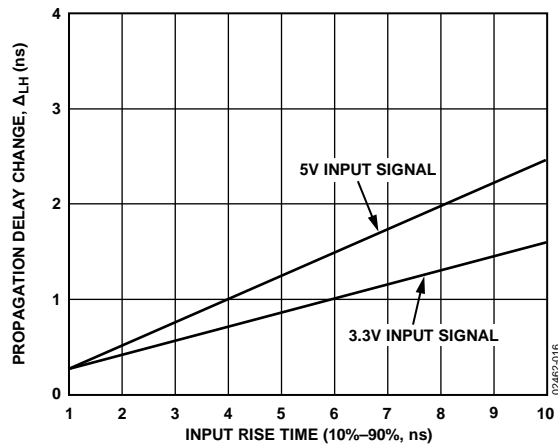


Figure 16. Typical Propagation Delay Change Due to Input Rise Time Variation (for $V_{DD1} = 3.3\text{ V}$ and 5 V)

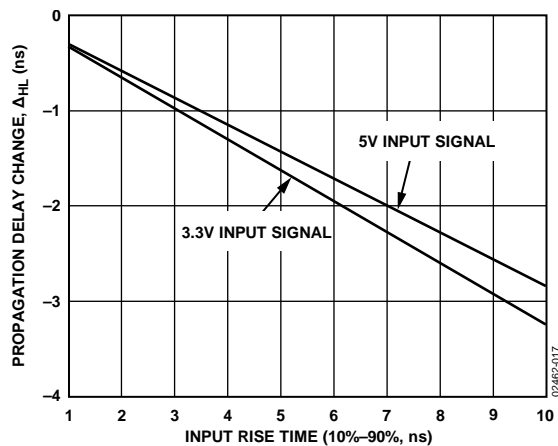


Figure 17. Typical Propagation Delay Change Due to Input Fall Time Variation (for $V_{DD1} = 3.3\text{ V}$ and 5 V)

The impact of the slower input edge rates can also affect the measured pulse width distortion as based on the input 50% level. This impact can either increase or decrease the apparent pulse width distortion depending on the relative magnitudes of t_{PHL} , t_{PLH} , and PWD . The case of interest here is the condition that leads to the largest increase in pulse width distortion. The change in this case is given by

$$\Delta PWD = PWD' - PWD = \Delta t_{LH} - \Delta t_{HL} = (t/0.8 V_I)(V - V_{ITH(L-H)} - V_{ITH(H-L)}), \text{ (for } t = t_R = t_F)$$

where:

$$PWD = |t_{PLH} - t_{PHL}|$$

$$PWD' = |t'_{PLH} - t'_{PHL}|$$

This adjustment in pulse width distortion is plotted as a function of input rise/fall time in Figure 18.

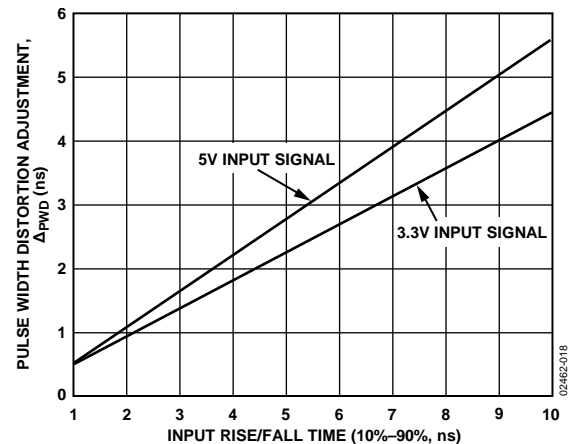


Figure 18. Typical Pulse Width Distortion Adjustment Due to Input Rise/Fall Time Variation (for $V_{DD1} = 3.3\text{ V}$ and 5 V)

METHOD OF OPERATION, DC CORRECTNESS, AND MAGNETIC FIELD IMMUNITY

The two coils in Figure 1 act as a pulse transformer. Positive and negative logic transitions at the isolator input cause narrow (2 ns) pulses to be sent via the transformer to the decoder. The decoder is bistable and therefore either set or reset by the pulses indicating input logic transitions. In the absence of logic transitions at the input for more than $\sim 1\text{ }\mu\text{s}$, a periodic update pulse of the appropriate polarity is sent to ensure dc correctness at the output. If the decoder receives none of these update pulses for more than about $5\text{ }\mu\text{s}$, the input side is assumed to be unpowered or nonfunctional, in which case the isolator output is forced to a logic high state by the watchdog timer circuit.

The limitation on the magnetic field immunity of the [ADuM1100](#) is set by the condition in which induced voltage in the transformer's receiving coil is sufficiently large to either falsely set or reset the decoder. The analysis that follows defines the conditions under which this can occur. The 3.3 V operating condition of the [ADuM1100](#) is examined because it represents the most susceptible mode of operation.

The pulses at the transformer output are greater than 1.0 V in amplitude. The decoder has sensing thresholds at about 0.5 V , therefore establishing a 0.5 V margin in which induced voltages can be tolerated. The voltage induced across the receiving coil is given by

$$V = (-d\beta/dt) \sum \pi r_n^2, n = 1, 2, \dots, N$$

where:

β is the magnetic flux density (gauss).

N is the number of turns in the receiving coil.

r_n is the radius of the n th turn in the receiving coil (cm).

Given the geometry of the receiving coil in the ADuM1100 and an imposed requirement that the induced voltage be at most 50% of the 0.5 V margin at the decoder, a maximum allowable magnetic field is calculated, as shown in Figure 19.

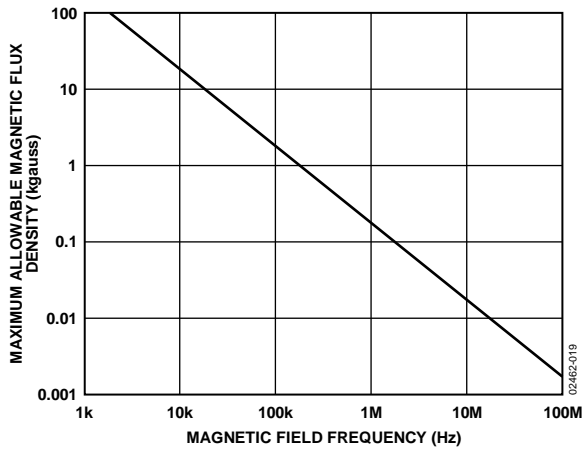


Figure 19. Maximum Allowable External Magnetic Field

For example, at a magnetic field frequency of 1 MHz, the maximum allowable magnetic field of 0.2 kgauss induces a voltage of 0.25 V at the receiving coil. This is about 50% of the sensing threshold and does not cause a faulty output transition. Similarly, if such an event were to occur during a transmitted pulse (and was of the worst-case polarity), it would reduce the received pulse from >1.0 V to 0.75 V, still well above the 0.5 V sensing threshold of the decoder.

The preceding magnetic flux density values correspond to specific current magnitudes at given distances away from the ADuM1100 transformers. Figure 20 expresses these allowable current magnitudes as a function of frequency for selected distances. As can be seen, the ADuM1100 is extremely immune and can be affected only by extremely large currents operated at high frequency and very close to the component. For the 1 MHz example noted, one would have to place a current of 0.5 kA 5 mm away from the ADuM1100 to affect the component's operation.

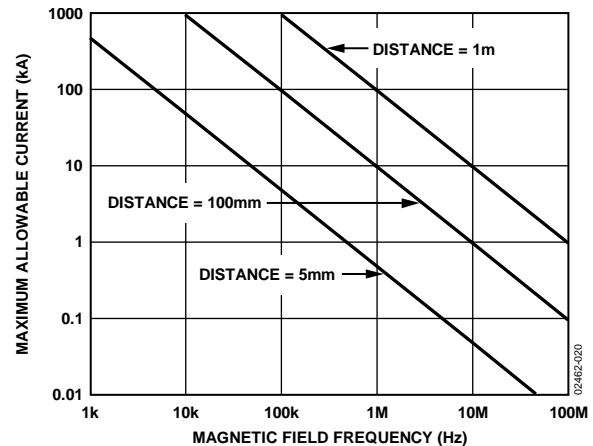


Figure 20. Maximum Allowable Current for Various Current-to-ADuM1100 Spacings

Note that at combinations of strong magnetic field and high frequency, any loops formed by printed circuit board traces could induce sufficiently large error voltages to trigger the thresholds of succeeding circuitry. Care should be taken in the layout of such traces to avoid this possibility.

POWER CONSUMPTION

The supply current of the ADuM1100 isolator is a function of the supply voltage, the input data rate, and the output load.

The input supply current is given by

$$I_{DDI} = I_{DDI(Q)} \quad f \leq 0.5f_r$$

$$I_{DDI} = I_{DDI(D)} \times (2f - f_r) + I_{DDI(Q)} \quad f > 0.5f_r$$

The output supply current is given by

$$I_{DDO} = I_{DDO(Q)} \quad f \leq 0.5f_r$$

$$I_{DDO} = (I_{DDO(D)} + (0.5 \times 10^{-3}) \times C_L V_{DDO}) \times (2f - f_r) + I_{DDO(Q)} \quad f > 0.5f_r$$

where:

$I_{DDI(D)}$, $I_{DDO(D)}$ are the input and output dynamic supply currents per channel (mA/Mbps).

C_L is the output load capacitance (pF).

V_{DDO} is the output supply voltage (V).

f is the input logic signal frequency (MHz, half the input data rate, NRZ signaling).

f_r is the input stage refresh rate (Mbps).

$I_{DDI(Q)}$, $I_{DDO(Q)}$ are the specified input and output quiescent supply currents (mA).

Figure 1: Dimensions of the test structure. The figure shows two views of a test structure. The top view is a plan view of a rectangular chip with dimensions: width 5.00 (0.1968) and 4.80 (0.1890); height 6.20 (0.2441) and 5.80 (0.2284); and internal features 4.00 (0.1574), 3.80 (0.1497), 1.27 (0.0500), and 1.75 (0.0688). The bottom view is a side view showing the chip's profile with dimensions: width 0.25 (0.0098) and 0.10 (0.0040); height 1.75 (0.0688) and 1.35 (0.0532); and internal features 0.51 (0.0201) and 0.31 (0.0122). The bottom view also includes a 'COPLANARITY 0.10' label and a 'SEATING PLANE' label. The right view is a perspective view of the chip with dimensions: width 0.50 (0.0196) and 0.25 (0.0099); height 1.27 (0.0500) and 0.40 (0.0157); and a 45° angle. The right view also includes a '8° 0°' label and a '0.17 (0.0067)' label.

COMPLIANT TO JEDEC STANDARDS MS-012-AA
CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS
(IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR
REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

Figure 21. 8-Lead Standard Small Outline Package [SOIC_N]
Narrow Body (R-8)
Dimensions shown in millimeters and (inches)

| Model ¹ | Temperature Range | Maximum Data Rate (Mbps) | Minimum Pulse Width (ns) | Package Description | Package Option |
|--------------------|-------------------|--------------------------|--------------------------|---------------------------------|----------------|
| ADuM1100AR | −40°C to +105°C | 25 | 40 | 8-Lead SOIC_N | R-8 |
| ADuM1100AR-RL7 | −40°C to +105°C | 25 | 40 | 8-Lead SOIC_N, 1,000 Piece Reel | R-8 |
| ADuM1100ARZ | −40°C to +105°C | 25 | 40 | 8-Lead SOIC_N | R-8 |
| ADuM1100ARZ-RL7 | −40°C to +105°C | 25 | 40 | 8-Lead SOIC_N, 1,000 Piece Reel | R-8 |
| ADuM1100BR | −40°C to +105°C | 100 | 10 | 8-Lead SOIC_N | R-8 |
| ADuM1100BR-RL7 | −40°C to +105°C | 100 | 10 | 8-Lead SOIC_N, 1,000 Piece Reel | R-8 |
| ADuM1100BRZ | −40°C to +105°C | 100 | 10 | 8-Lead SOIC_N | R-8 |
| ADuM1100BRZ-RL7 | −40°C to +105°C | 100 | 10 | 8-Lead SOIC_N, 1,000 Piece Reel | R-8 |
| ADuM1100UR | −40°C to +125°C | 100 | 10 | 8-Lead SOIC_N | R-8 |
| ADuM1100UR-RL7 | −40°C to +125°C | 100 | 10 | 8-Lead SOIC_N, 1,000 Piece Reel | R-8 |
| ADuM1100URZ | −40°C to +125°C | 100 | 10 | 8-Lead SOIC_N | R-8 |
| ADuM1100URZ-RL7 | −40°C to +125°C | 100 | 10 | 8-Lead SOIC_N, 1,000 Piece Reel | R-8 |

¹ Z = RoHS Compliant Part.

NOTES