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REVISION HISTORY

5/2017—Rev. 0 to Rev. A

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Changed CP-24-10 to CP-24-14 ... Throughout
Updated Outline Dimensions ... 28
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7/2016—Revision 0: Initial Version

DETAILED FUNCTIONAL BLOCK DIAGRAM

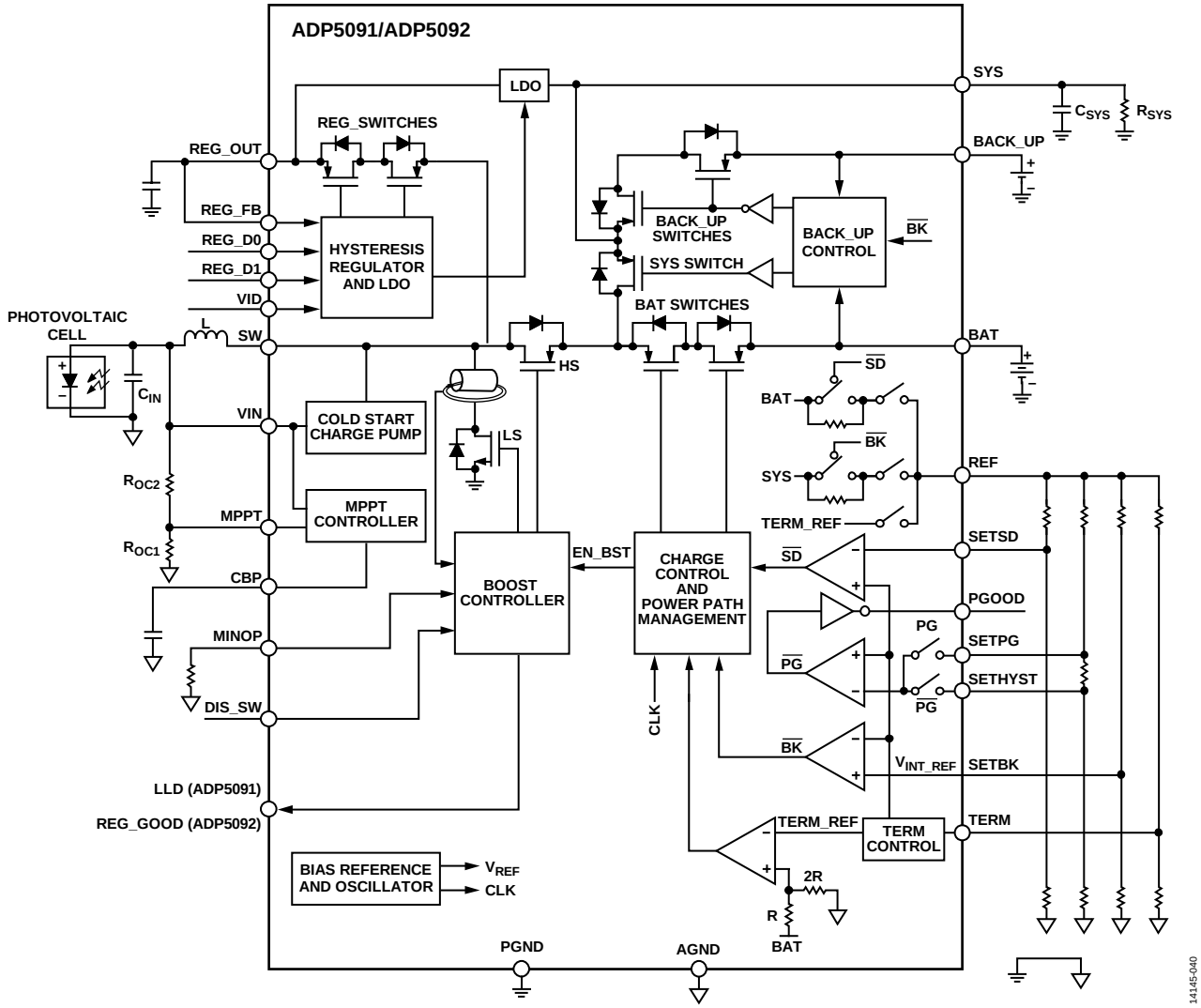

Figure 2. Detailed Functional Block Diagram

SPECIFICATIONS

Voltage input (V_{IN}) = 1.2 V, V_{SYS} = V_{BAT} = 3 V, T_J = −40°C to +125°C for minimum/maximum specifications, and T_A = 25°C for typical specifications, unless otherwise noted. External components include the following: inductance (L) = 22 µH, input capacitance (C_{IN}) = 4.7 µF, and C_{SYS} = 4.7 µF.

Table 1.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
QUIESCENT CURRENT						
Operating Quiescent Current of SYS Pin ($V_{IN} > V_{CBP} \geq V_{MINOP}$)	I_{Q_SYS}	REG_D0 = low, REG_D1 = low		510	1000	nA
		REG_D0 = high, REG_D1 = low		650	1150	nA
		REG_D0 = low, REG_D1 = high		750	1290	nA
		REG_D0 = high, REG_D1 = high		760	1300	nA
Sleeping Quiescent Current of SYS Pin ($V_{CBP} < V_{MINOP}$)	$I_{IQ\_SLEEP\_SYS}$	REG_D0 = low, REG_D1 = low		390	880	nA
COLD START CIRCUIT						
Minimum Input Voltage for Cold Start	V_{IN_COLD}	V_{SYS} = 0 V, 0°C < T_A < 85°C		380	500	mV
Minimum Input Power for Cold Start	P_{IN_COLD}			6		µW
End of Cold Start Operation						
Threshold	V_{SYS_TH}		1.73	1.87	2.00	V
Hysteresis	V_{SYS_HYS}			95		mV
BOOST REGULATOR						
Input Voltage Operating Range	V_{IN}	Cold start completed	0.08		3.3	V
Input Power Operating Range	P_{IN}	Cold start completed, V_{IN} = 3 V			600	mW
Start Charging BAT Threshold on SYS	V_{SYS_CHG}		2.00	2.19	2.35	V
Start Charging BAT Hysteresis on SYS	$V_{SYS\_CHG\_HYS}$			150		mV
Input Peak Current	I_{IN_PEAK}	Factory trim, 1 bit, Option 0		200	250	mA
		Option 1		300		mA
Low-Side Switch On Resistance	$R_{LS\_DS\_ON}$	Pin to pin measurement		0.44	0.6	Ω
High-Side Switch On Resistance	$R_{HS\_DS\_ON}$	Pin to pin measurement		0.85	1.2	Ω
SYS Switch On Resistance	$R_{SYS\_DS\_ON}$			0.32	0.70	Ω
DIS_SW Voltage						
High	$V_{DIS\_SW\_HIGH}$		1			V
Low	$V_{DIS\_SW\_LOW}$				0.5	V
DIS_SW Delay	$t_{DIS\_SW\_DELAY}$			1		µs
VIN CONTROL AND MINOP						
VIN Open Circuit Voltage						
Default Sampling Cycle	t_{OCV_CYCLE}	Factory trim, 2 bit (4 sec, 8 sec, 16 sec, 32 sec)		16		sec
Sampling Time	t_{OCV_SAMPL}			256		ms
MINOP Bias Current	I_{MINOP}		1.58	2.00	2.45	µA
MINOP Operation Voltage Threshold of Dynamic MPPT Sensing Mode	V_{MINOP_DSM}				1.5	V
MPPT Bias Current of MPPT No Sensing Mode	I_{MPPT}		1.7	2.0	2.3	µA
LLD (ADP5091 Only)						
Pull-Up Resistor				12	17	kΩ
Pull-Down Resistor				12	17	kΩ
High Voltage	V_{LLD_IH}			V_{REG_OUT}		V
Leakage Current at CBP Pin	I_{CBP_LEAK}			10	2000	pA

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
ENERGY STORAGE MANAGEMENT						
Internal Reference Voltage	V_{INT_REF}		0.955	1.011	1.067	V
Battery Stop Discharging						
Threshold	V_{SETSD}		2.0		V_{BAT_TERM}	V
Hysteresis Resistor	R_{SETSD_HYS}		80	115	160	kΩ
Battery Terminal Charging						
Threshold	V_{BAT_TERM}		2.2		5.2	V
Hysteresis	$V_{BAT\_TERM\_HYS}$			3	3.1	%
PGOOD Rising Threshold at SYS Pin	V_{SYS_PG}		V_{SETSD}		V_{BAT_TERM}	V
PGOOD Pull-Up Resistor				11.6	17.0	kΩ
PGOOD Pull-Down Resistor				11.6	17.0	kΩ
PGOOD High Voltage	V_{PGOOD_HIGH}			V_{SYS}		V
Battery Switches On Resistance	$R_{BAT\_SW\_ON}$	Pin to pin measurement		0.59	0.85	Ω
Battery Source Current	I_{BAT}				1	A
Leakage Current at BAT Pin	I_{BAT_LEAK}	V_{BAT} = 2 V, V_{SETSD} = 2.2 V, V_{SYS} = 2 V		22	50	nA
		V_{BAT} = 3.3 V, V_{SETSD} = 2.2 V, V_{SYS} = 0 V		3.5	35	nA
BACK_UP POWER PATH						
Turning Off BACK_UP Switch						
Threshold on BAT	V_{SETBK}		2.0		V_{BAT_TERM}	V
Hysteresis Resistor	R_{SETBK_HYS}		80	115	160	kΩ
BACK_UP Switches On Resistance				0.85	1.20	Ω
BACK_UP and BAT Comparator		$V_{SYS} \geq V_{SYS\_TH}$				
Offset	V_{BKP_OFFSET}		158	190	271	mV
Hysteresis	V_{BAT_HYS}		68	75	108	mV
BACK_UP Current Capability	I_{BKP}	$V_{SYS} < V_{SYS\_TH}$		250		µA
Leakage Current at BACK_UP Pin	I_{BKP_LEAK}	$V_{BACK\_UP} = V_{SYS} = V_{BAT}$ = 3 V		16	40	nA
THERMAL SHUTDOWN						
Threshold	T_{SHDN}	$V_{SYS} \geq V_{SYS\_TH}$		142		°C
Hysteresis	T_{HYS}			15		°C

REGULATED OUTPUT SPECIFICATIONS

V_{IN} = 1.2 V, V_{SYS} = V_{BAT} = 3 V, V_{REG_OUT} = 2 V, L = 22 µH, C_{IN} = 4.7 µF, C_{SYS} = 4.7 µF, C_{REG_OUT} = 4.7 µF, T_J = −40°C to +125°C for minimum/maximum specifications, and T_A = 25°C for typical specifications, unless otherwise noted.

Table 2.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
REGULATED OUTPUT						
Output Options by VID Control	V_{REG_OUT}		1.5		3.6	V
Rating Current	I_{REG_OUT}	V_{REG_OUT} = 1.5 V to 3.6 V		150		mA
REG_OUT Pull-Down Resistance	R_{REG_OUT}			235		Ω
REG_OUT IN BOOST MODE						
REG_OUT Wake Threshold	V_{REG_WAKE}		1.008 × V_{REG_OUT}	1.027 × V_{REG_OUT}	1.048 × V_{REG_OUT}	V
REG_OUT Wake Threshold Hysteresis	$V_{REG\_WAKE\_HYS}$			1		%
Adjustable REG_OUT Wake Threshold	$V_{ADJ\_REG\_WAKE}$		1.008	1.028	1.048	V
Adjustable REG_OUT Sleep Threshold	$V_{ADJ\_REG\_SLEEP}$		1.018	1.038	1.058	V
High-Side Switches On Resistance	$R_{BST\_DS\_ON}$			1.63	2.15	Ω
Current-Limit Threshold of Boost Mode	$I_{REG\_BST\_LIM}$			100	155	mA
REG_OUT IN LOW DROPOUT (LDO) MODE						
REG_OUT Accuracy	V_{REG_LDO}	0 µA < I_{OUT} < 150 mA, V_{SYS} = (V_{REG_OUT} + 0.5 V)	−3.5		+3.5	%
Adjustable REG_OUT Accuracy	$V_{REG\_LDO\_ADJ}$	I_{OUT} = 1 mA	0.999	1.015	1.028	V
		0 µA < I_{OUT} < 150 mA, V_{SYS} = (V_{REG_OUT} + 0.5 V)	0.985	1.015	1.045	V
REG_OUT Dropout	V_{REG_DROP}	I_{OUT} = 150 mA		200		mV
Current-Limit Threshold of LDO Mode	I_{REG_LIM}	V_{SYS} ≥ V_{SYS_TH}	200	260		mA
Output Noise	OUT_{NOISE}	10 Hz to 100 kHz		700		µV rms
Power Supply Rejection Ratio	PSRR	100 Hz		60		dB
		1 kHz		40		dB
REG_D0 and REG_D1						
Input Logic						
High	$V_{REG\_DX\_IH}$		1.2			V
Low	$V_{REG\_DX\_IL}$				0.4	V
Input Leakage Current	$I_{REG\_DX\_LEAK}$			20		nA
REG_GOOD (ADP5092 ONLY)						
Rising Threshold	V_{REG_GOOD}		89.5	92.5	95.7	%
Hysteresis	$V_{REG\_GOOD\_HYS}$			2		%
Pull-Up Resistor				11.6	17	kΩ
Pull-Down Resistor				11.6	17	kΩ
High Voltage	$V_{REG\_GOOD\_IH}$			V_{REG_OUT}		V

ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Rating
VIN, MPPT, CBP, MINOP	−0.3 V to +3.6 V
DIS_SW, TERM, SETPG, SETSD, SETBK, PGOOD, SETHYST, REF, REG_D0, VID, REG_D1, LLD, REG_GOOD to AGND	−0.3 V to +6.0 V
SW, SYS, BAT, BACK_UP, REG_OUT, REG_FB to PGND	−0.3 V to +6.0 V
PGND to AGND	−0.3 V to +0.3 V

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 4.

Package Type	θ_{JA}	θ_{JC}	Unit
24-Lead LFCSP	58.7	36	°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

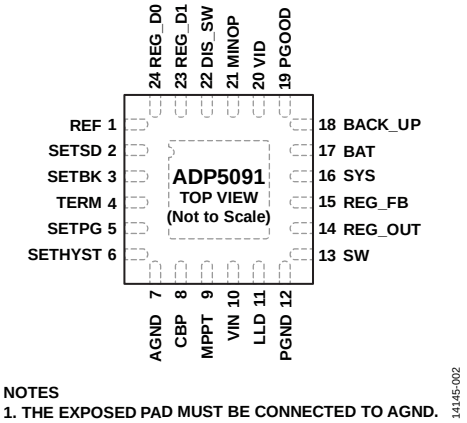

Figure 3. ADP5091 Pin Configuration

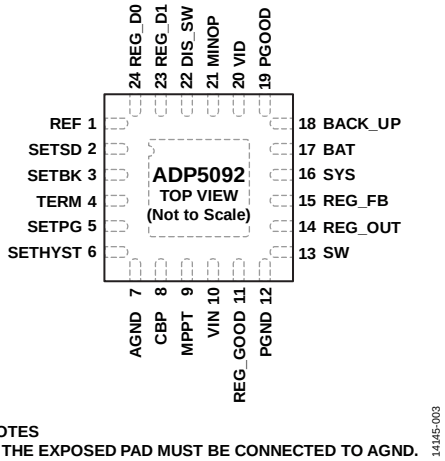

Figure 4. ADP5092 Pin Configuration

Table 5. Pin Function Descriptions

Pin No.[1]			
ADP5091	ADP5092	Mnemonic	Description
1	1	REF	Internal Voltage Reference Monitoring Node for the SETSD, SETPG, SETBK, and TERM Pins.
2	2	SETSD	Shutdown Setting. The SETSD pin sets the shutdown discharging voltage based on the BAT pin voltage level.
3	3	SETBK	BACK_UP Disabled Threshold Monitoring BAT Voltage Setting. Connect the SETBK pin to the AGND pin without the BACK_UP storage element.
4	4	TERM	Termination Charging Voltage. This pin sets the termination charging voltage based on the BAT pin voltage level.
5	5	SETPG	Power-Good Rising Threshold Monitoring SYS Node Voltage Level Setting.
6	6	SETHYST	PGOOD Falling Hysteresis Setting. Connect a resistor between SETPG and SETHYST to program the PGOOD falling hysteresis.
7	7	AGND	Analog Ground.
8	8	CBP	Capacitor Bypass. This pin samples and holds the maximum power point level. Connect a 10 nF capacitor from the CBP pin to the AGND pin. When the MPPT pin is disabled, tie the CBP pin to an external reference that is lower than the VIN pin.
9	9	MPPT	Maximum Power Point Tracking. This pin sets the maximum power point ratio for the different energy harvesters with a resistor divider. In no sensing mode, place a resistor through AGND to set the MPPT voltage. The typical current value is 2.0 µA.
10	10	VIN	Input Supply from Energy Harvester Source. Connect at least a 10 µF capacitor as close as possible between VIN and PGND.
11	N/A	LLD	Low Light Density Indicator to Microcontroller for the ADP5091. LLD pulls high at the MINOP voltage higher than the CBP voltage.
N/A	11	REG_GOOD	Regulated Output Power Good for the ADP5092.
12	12	PGND	Power Ground.
13	13	SW	Switching Node for the Inductive Boost Regulator with a Connection to an External Inductor. Connect a 22 µH inductor between SW and VIN.
14	14	REG_OUT	Regulated Output. Connect at least a 4.7 µF capacitor as close as possible between REG_OUT and PGND.
15	15	REG_FB	Regulated Output Feedback Voltage Sense Input. The fixed output connects this pin to REG_OUT. The adjustable output connects this pin to a resistor divider from REG_OUT.
16	16	SYS	Output Supply to System Load. Connect at least a 4.7 µF capacitor as close as possible between SYS and PGND.
17	17	BAT	SYS Output Supply Storage. This pin places the rechargeable battery or super capacitor as a storage for the SYS output supply.
18	18	BACK_UP	Optional Input Supply from the Backup Primary Battery Cell.

Pin No.[1]		Mnemonic	Description
ADP5091	ADP5092		
19	19	PGOOD	Output Signal to Microcontroller. This pin maintains a pulled high level when SYS is higher than the SETPG threshold.
20	20	VID	Voltage Configuration Pin for REG_OUT. This pin sets up to eight different regulated outputs tied low through a resistor to AGND. The output configuration details are in Table 7.
21	21	MINOP	Minimum Operating Power. Place a resistor on MINOP to set the minimum operating input voltage level. The boost regulator starts switching when the CBP voltage exceeds the MINOP voltage. When the MINOP pin is floating, the IC operates in no sensing mode with a fixed MPPT level. Connect this pin through AGND to disable the MINOP function.
22	22	DIS_SW	Control Signal from Microcontroller or RF Transceiver to Stop Switching Boost Charger.
23	23	REG_D1	Regulated Output Working Mode Set D1. Enable LDO mode by pulling this pin high.
24	24	REG_D0	Regulated Output Working Mode Set D0. Enable boost mode by pulling this pin high.
		EPAD	Exposed Pad. The exposed pad must be connected to AGND.

[1] N/A means not applicable.

TYPICAL PERFORMANCE CHARACTERISTICS

V_{BAT_TERM} = 3.5 V, V_{SYS_PG} = 2.8 V, V_{SETSD} = 2.4 V, MPPT (OCV) = 80%, L = 22 µH, C_{IN} = 10 µF, C_{SYS} = 4.7 µF, C_{REG_OUT} = 10 µF, C_{CBP} = 10 nF.

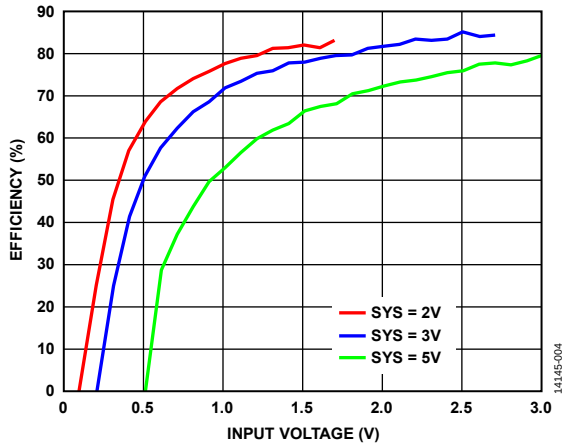

Figure 5. Efficiency vs. Input Voltage, I_{IN} = 10 µA

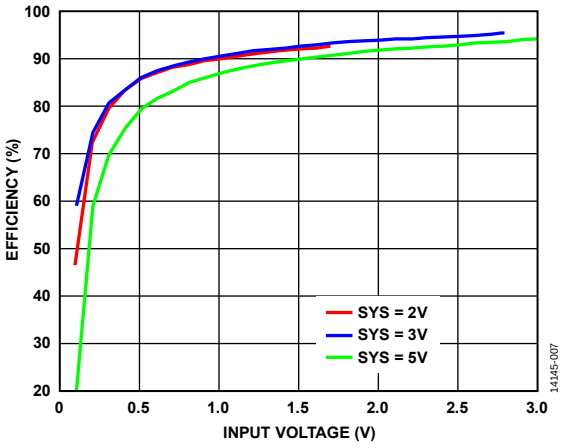

Figure 8. Efficiency vs. Input Voltage, I_{IN} = 100 µA

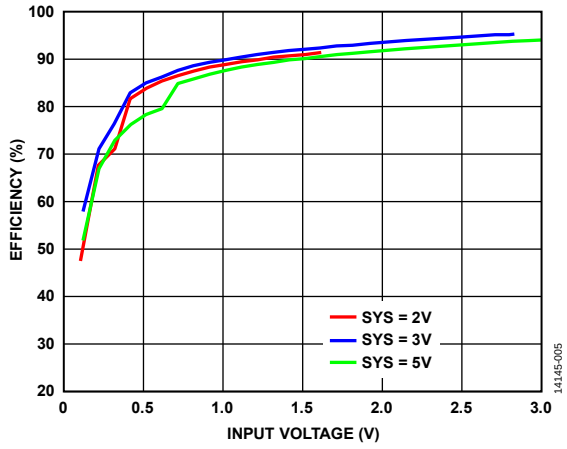

Figure 6. Efficiency vs. Input Voltage, I_{IN} = 10 mA

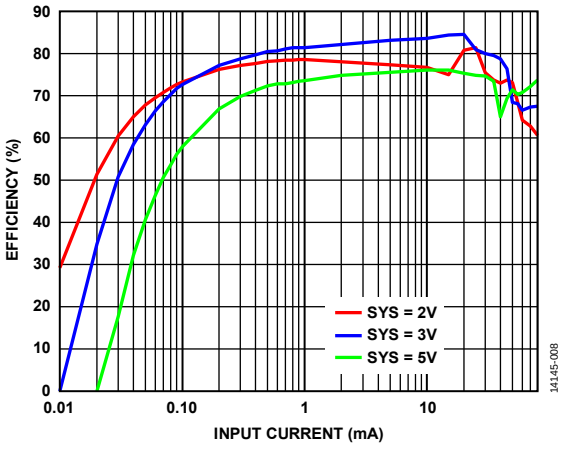

Figure 9. Efficiency vs. Input Current, V_{IN} = 0.2 V

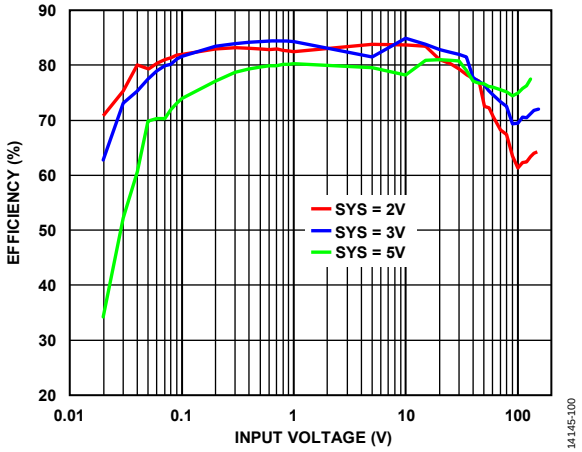

Figure 7. Efficiency vs. Input Voltage, V_{IN} = 0.5 V

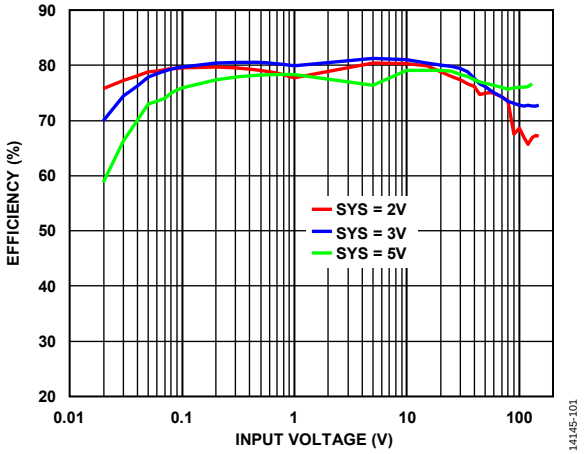

Figure 10. Efficiency vs. Input Voltage, V_{IN} = 1 V

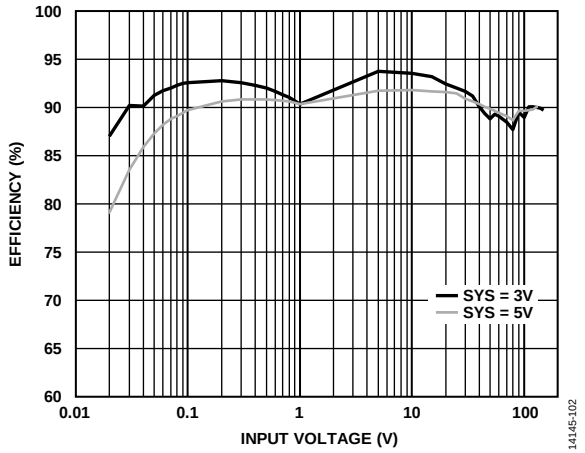

Figure 11. Efficiency vs. Input Voltage, V_{IN} = 2 V

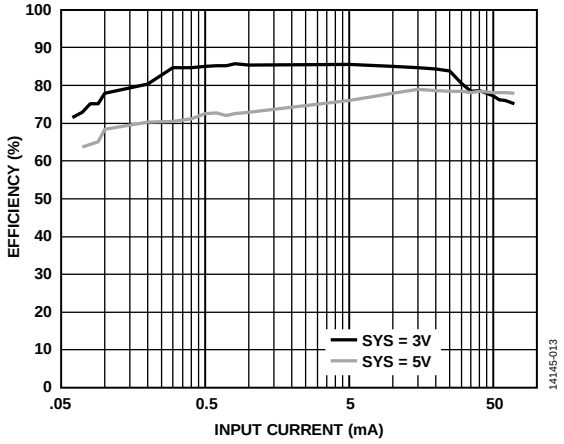

Figure 14. Efficiency vs. Input Current, V_{IN} = 0.5 V, V_{REG_OUT} = 2 V, I_{REG_OUT} = 10 µA

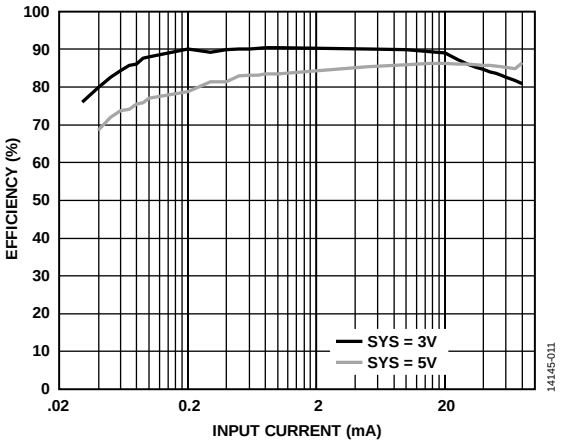

Figure 12. Efficiency vs. Input Current, V_{IN} = 1 V, V_{REG_OUT} = 2 V, I_{REG_OUT} = 10 µA

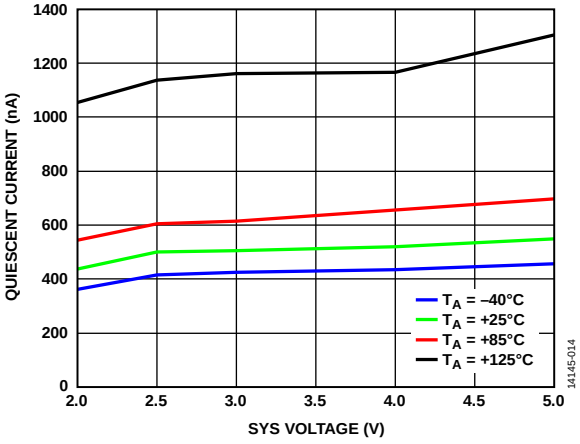

Figure 15. Quiescent Current vs. SYS Voltage, $V_{MINOP} \leq V_{CBP}$

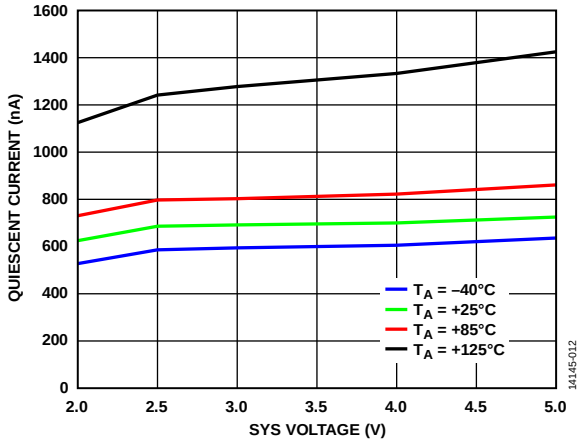

Figure 13. Quiescent Current vs. SYS Voltage, $V_{REG\_D0} = V_{REG\_D1} = V_{SYS}$, $V_{MINOP} \leq V_{CBP}$

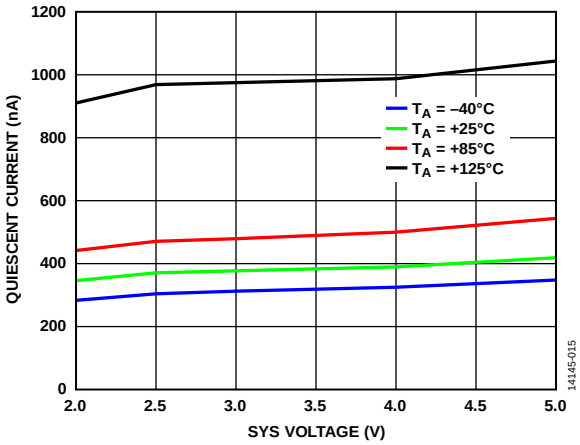

Figure 16. Quiescent Current vs. SYS Voltage, $V_{MINOP} > V_{CBP}$

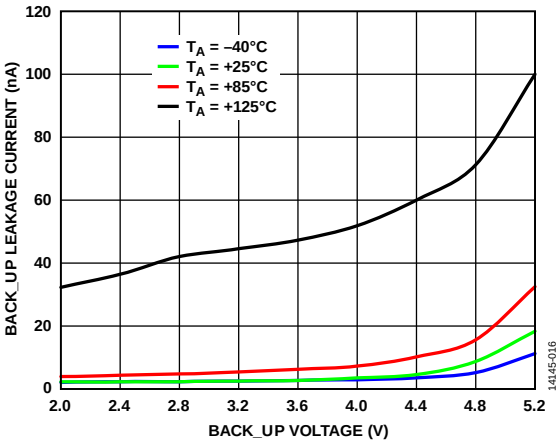

Figure 17. BACK_UP Leakage Current vs. BACK_UP Voltage

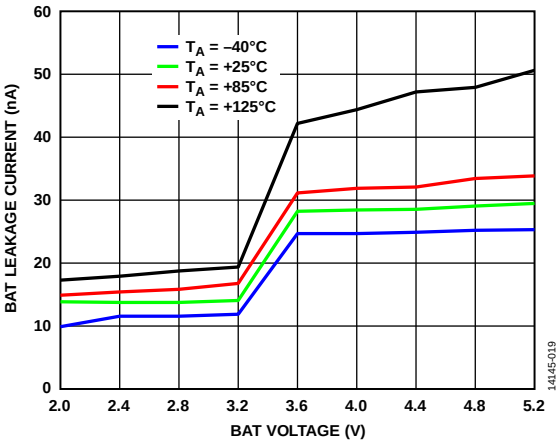

Figure 20. BAT Leakage Current vs. BAT Voltage

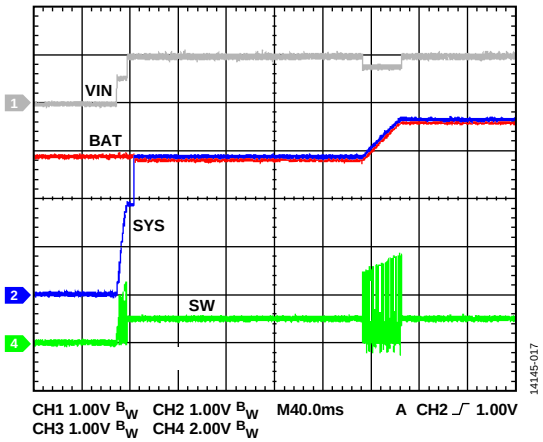

Figure 18. Startup with 100 µF Battery, $V_{BAT} > V_{SETSD}$

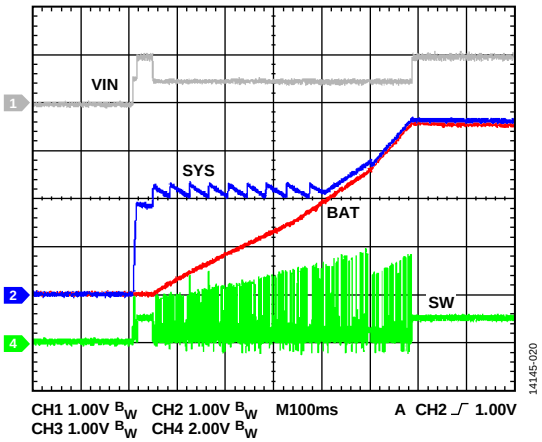

Figure 21. Startup with Empty 100 µF Capacitor

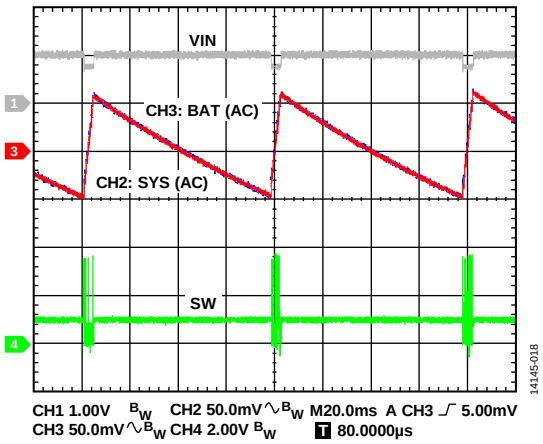

Figure 19. Output Ripple of TERM Function with 100 µA Load

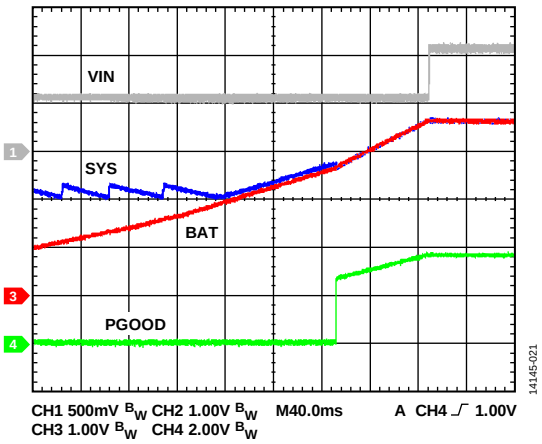

Figure 22. PGOOD Function Waveform

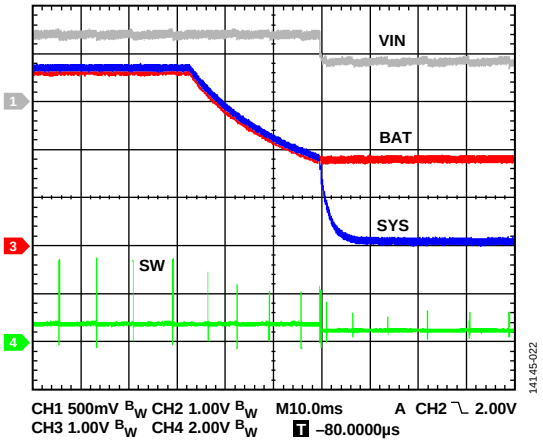

Figure 23. Battery Protection Function Waveform

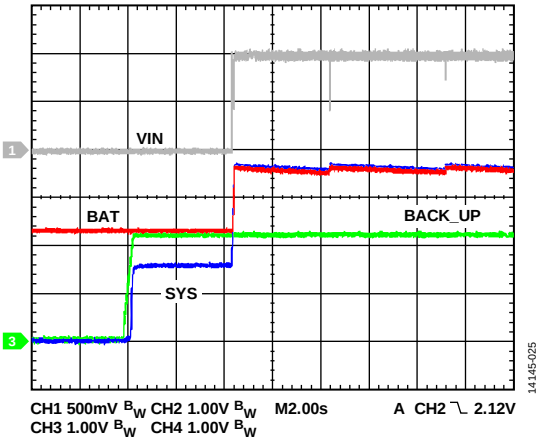

Figure 26. BACK_UP Function, $V_{BAT} < V_{SETBK}$, $V_{BACK\_UP} < V_{BAT}$

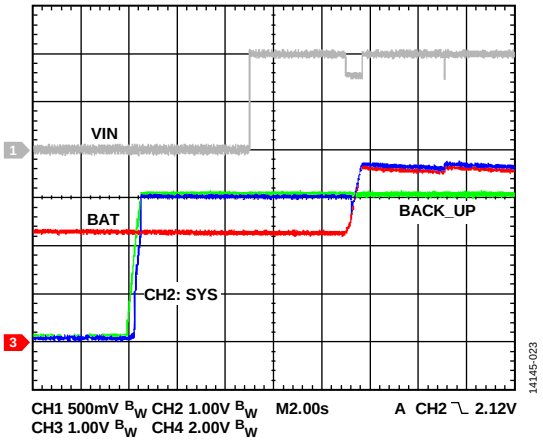

Figure 24. Backup Function, $V_{BAT} < V_{SETBK}$, $V_{BACK\_UP} > V_{BAT}$

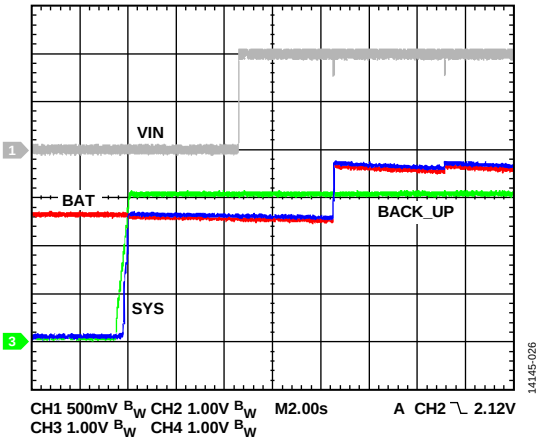

Figure 27. BACK_UP Function, $V_{BAT} > V_{SETBK}$, $V_{BACK\_UP} > V_{BAT}$

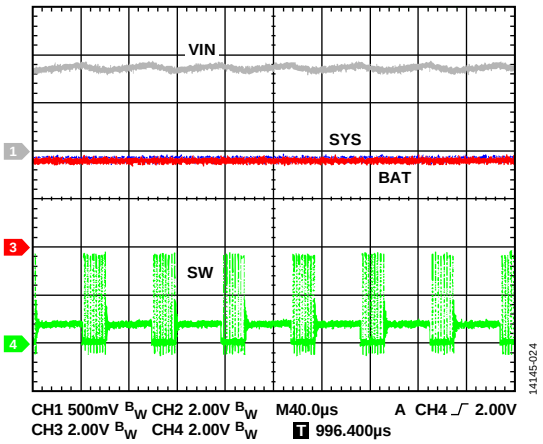

Figure 25. Main Boost Pulse Frequency Modulation (PFM) Waveform with 200 µA Load

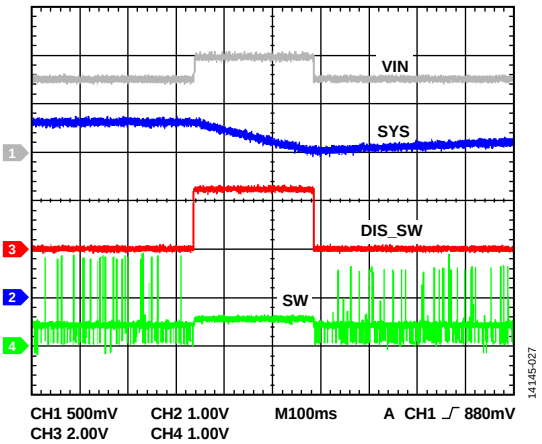

Figure 28. DIS_SW Function Waveform

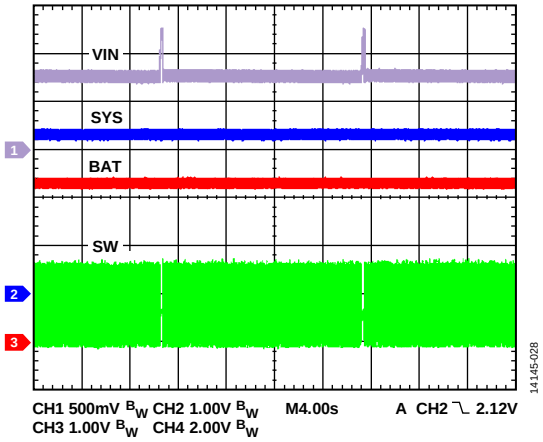

Figure 29. MPPT No Sensing Mode, R_{MPPT} = 400 kΩ

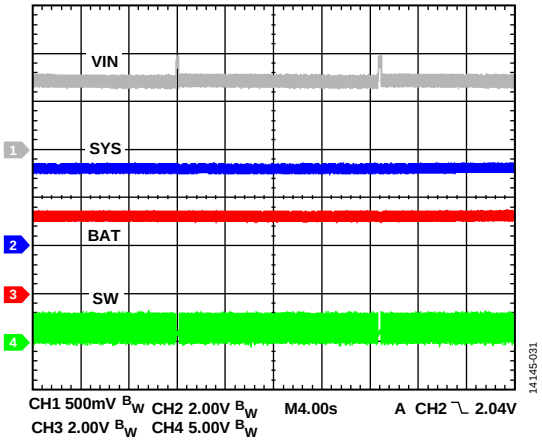

Figure 32. MPPT Dynamic Sensing Mode

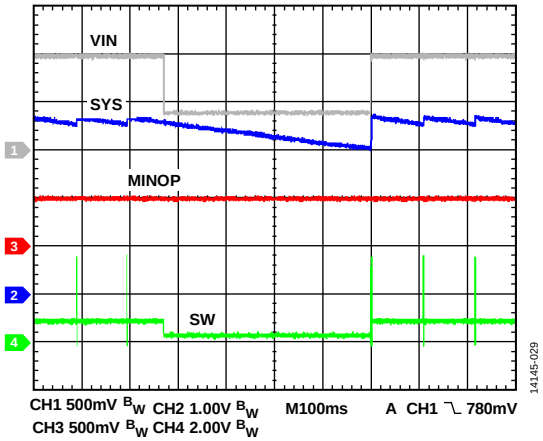

Figure 30. MINOP Function

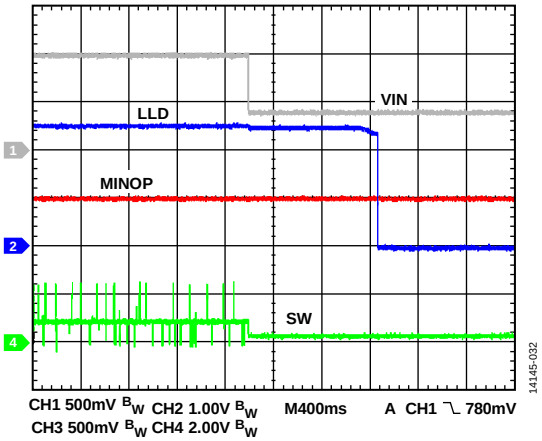

Figure 33. LLD Function

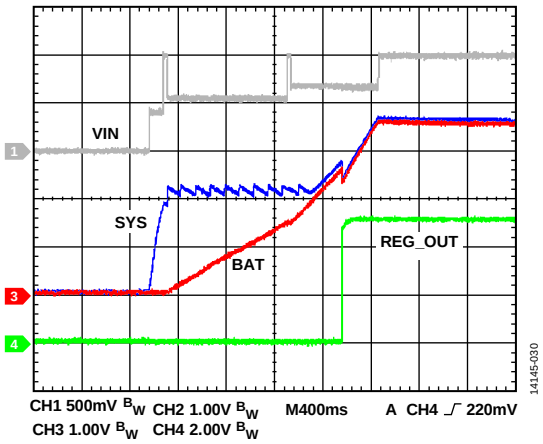

Figure 31. REG_OUT Start (Hybrid Mode)

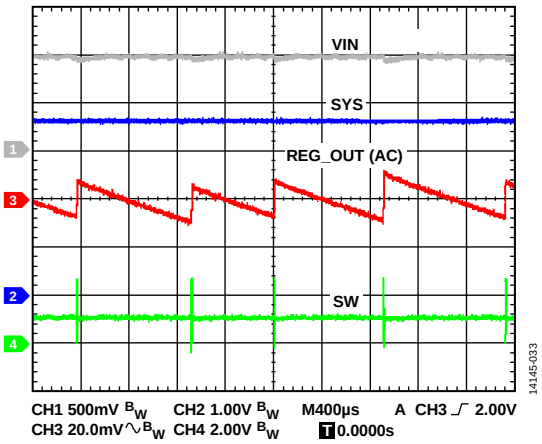

Figure 34. REG_OUT Ripple (Boost Mode)

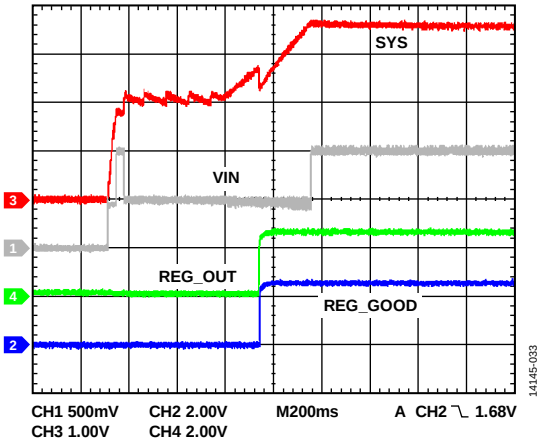

Figure 35. REG_GOOD Function

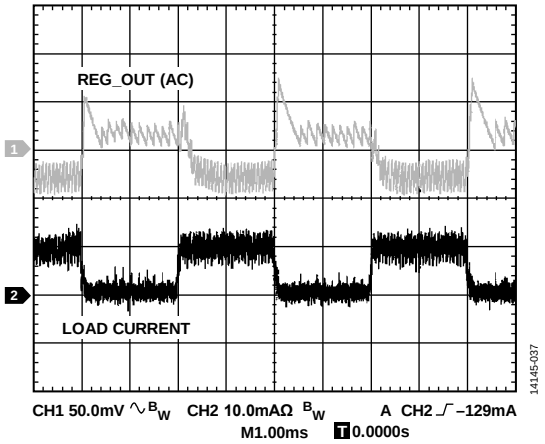

Figure 38. REG_OUT Load Transient (Hybrid), I_{REG_OUT} from 10 µA to 10 mA

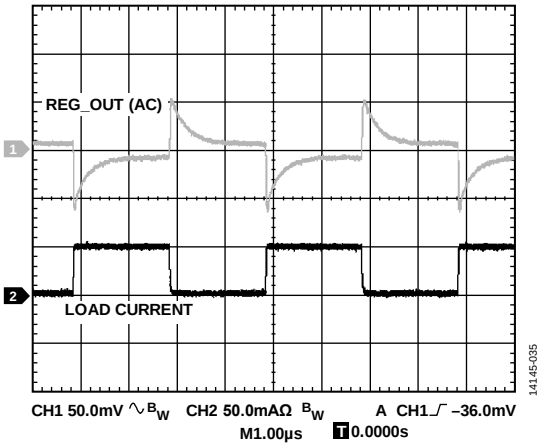

Figure 36. REG_OUT Load Transient (LDO), I_{REG_OUT} from 10 µA to 50 mA

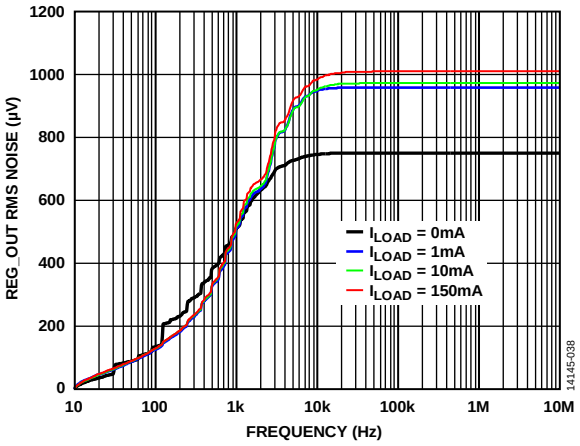

Figure 39. REG_OUT RMS Noise vs. Frequency

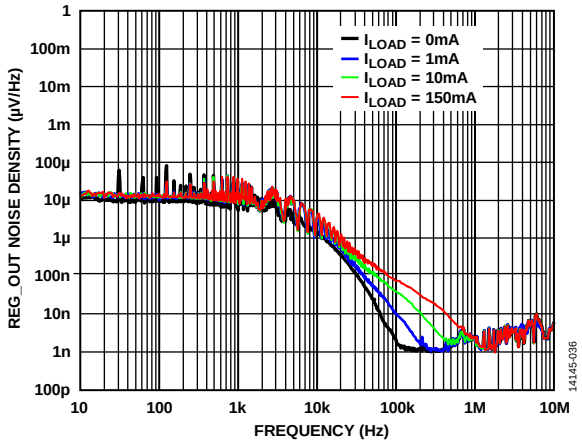

Figure 37. REG_OUT Noise Density vs. Frequency at Various Current Loads (I_{LOAD})

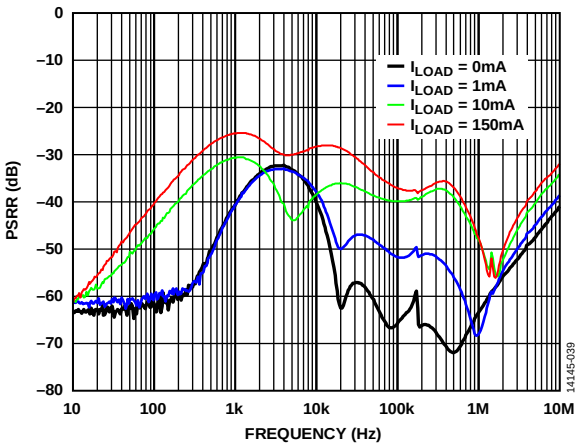

Figure 40. Power Supply Rejection Ratio (PSRR) vs. Frequency

THEORY OF OPERATION

The ADP5091/ADP5092 are intelligent, integrated energy harvesting, ultralow power management solutions that include a cold start-up circuit, one synchronous main boost controller, and one regulated output hybrid controller with integrated switches, a charging controller with integrated switches, and backup power path switches. The main boost controller converts maximum power from low voltage, high impedance dc sources, such as PV cells, TEGs, and piezoelectric modules, to store energy in a rechargeable battery or capacitor with storage protection and provides power to the load. Another regulated output with automatic hysteresis boost/LDO mode, or pure LDO mode, is optimized to provide high efficiency across low output currents (10 μA), see Figure 14) to high currents of 200 mA. The ADP5091/ADP5092 can also control an additional power path from a primary battery cell to the system. An external signal can temporarily stop the two boost circuits to prevent interference with RF transmission.

FAST COLD START-UP CIRCUIT ($V_{SYS} < V_{SYS\_TH}$, $V_{IN} > V_{IN\_COLD}$)

The fast cold start-up circuit extracts energy available at the VIN pin and charges only the capacitors at the SYS pin up to V_{SYS_TH} above which the main boost regulator and charge controller start working. The efficient boost regulator charges storage elements on the BAT pin when the SYS voltage is more than the internal BAT charging threshold (V_{SYS_CHG}). When the SYS voltage is less than the internal BAT charging threshold with a hysteresis, it stops charging the BAT pin and restarts charging the SYS pin to ensure that it does not enter cold startup. Figure 41 shows the fast cold start-up sequence.

The cold start-up circuit is required when the VIN pin is more than the minimum input voltage for the cold start (V_{IN_COLD}), and the energy storage voltage at the SYS pin is less than the end of the cold start operation threshold (V_{SYS_TH}). To complete the cold startup, the energy harvester must supply sufficient power (see the Energy Harvester Selection section). The cold startup, with much lower efficiency compared to the main boost regulator, achieves a short start-up time, creating a low shutdown current from the system load enabled by the PGOOD signal. To bypass the cold startup, place a primary battery at the BACK_UP pin (see the Backup Storage Path section).

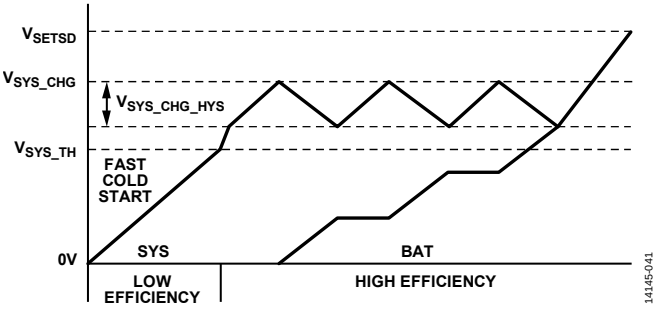

Figure 41. Fast Cold Start-Up Sequence

MAIN BOOST REGULATOR ($V_{BAT\_TERM} > V_{SYS} > V_{SYS\_TH}$)

The switching mode synchronous boost regulator, with an external inductor connected between the VIN and the SW pins, operates in pulse frequency modulation (PFM) mode, transferring energy stored in the input capacitor to the energy storage connected to the BAT pin. The MPPT control loop regulates the VIN voltage at the level sampled at the MPPT pin and stored at the capacitor through the CBP and the AGND pins. To maintain the high efficiency of the regulator across a wide input power range, the current sense circuitry employs an internal dither peak current limit to control the inductor current.

The main boost regulator operation reaches an asynchronous mode via the energy storage controller if the BAT pin voltage is less than the battery terminal charging threshold programmed at the SETSD pin, or stops switching if the BAT pin voltage is more than the battery overcharging threshold programmed at the TERM pin. The boost regulator disables when the voltage on the CBP pin decreases to the threshold set by the resistor at the MINOP pin. In addition, the boost is periodically stopped by an open voltage sampling circuit and can also be temporary disabled by driving the DIS_SW pin high.

VIN OPEN CIRCUIT AND MPPT

By floating the MINOP pin, the MPPT no sensing mode can operate on a fixed MPPT voltage. The MPPT pin, with a 2.0 μA (typical) bias current through a resistor, sets the MPPT voltage, which is the boost input regulation reference.

When the MINOP pin voltage is set lower than V_{MINOP_DSM} through a resistor to AGND, the ADP5091/ADP5092 operate in MPPT dynamic sensing mode. The boost input regulation reference is the open circuit voltage at the VIN pin scaled to a ratio programmed by the resistor divider at the MPPT pin. To keep the VIN voltage operating at the maximum power points available from the energy harvester at the input of the ADP5091/ADP5092, periodically sample the MPPT voltage and store it in the capacitor connected to the CBP pin. The reference voltage refreshes every 16 sec (default value) by periodically disabling the boost regulator for 256 ms (default value) and by sampling the ratio of the open circuit voltage when the BAT voltage level exceeds the SETSD rising threshold. The factory bit can program the sampling cycle. Set the reference voltage by

$$V_{MPPT} = V_{IN}(Open\ Circuit)\left(\frac{R_{OC1}}{R_{OC1} + R_{OC2}}\right) \quad (1)$$

where:

V_{IN} *(Open Circuit)* is the input open circuit voltage (V_{IN_OCV}) of the input voltage.

See Figure 2 for R_{OC1} and R_{OC2}.

The typical MPPT ratio depends on the type of harvester. For example, it is 0.7 to 0.85 for PV cells, and 0.5 for TEGs. The sampling OCV rate is adjustable depending on the previously sampled OCV level. To disable the MPPT function, leave the MPPT pin floating and set the CBP pin to an external voltage reference lower than the VIN voltage.

MINIMUM OPERATION THRESHOLD FUNCTION

By setting the MINOP pin voltage lower than the MINOP operation voltage range of the dynamic MPPT sensing mode (V_{MINOP_DSM}) through a resistor to AGND, the minimum operation threshold function can disable the main boost regulator to prevent discharging the storage element when the energy generated by the harvester is less than the system consumption. When the voltage of the CBP pin decreases to the threshold set by the resistor at the MINOP pin, the boost regulator stops switching. The typical MINOP bias current is 2.00 µA. The minimum operation threshold function disables the MPPT function to achieve the sleeping quiescent current of 390 nA (typical). Disable this function by connecting the MINOP pin to the AGND pin.

The low light density (LLD) indicator (ADP5091 only) is the MINOP comparator output that signals the microprocessor to calculate the cycle with insufficient input energy in a certain period.

DISABLING BOOST

For noise or electromagnetic interference (EMI) sensitive applications, pull the DIS_SW pin high to stop the boost switcher temporarily to prevent interference with RF circuits. Pull the DIS_SW pin low to resume the boost switching. The transition delay is 1 µs (typical).

REGULATED OUTPUT WORKING MODE

The 150 mA regulated output of the ADP5091/ADP5092 not only operates in the hysteresis boost mode or the LDO mode but also operates in the hybrid mode in which the regulator can smoothly transition between these two modes automatically. After the BAT voltage exceeds the SETSD threshold or the SYS voltage is greater than SETPG threshold, the regulator can be enabled.

In hysteresis boost mode, the boost regulator in the ADP5091/ADP5092 charges the output voltage slightly higher than its preset output voltage. When the output voltage increases until the output sense signal exceeds the hysteresis comparator upper threshold (the sleep threshold), the regulator enters sleep mode. In sleep mode, to allow a low quiescent current as well as high efficiency performance, the low-side and high-side switches and a majority of the circuitry are disabled.

During sleep mode, the output capacitor supplies the energy into the load, the output voltage decreases until it falls below the hysteresis comparator lower threshold (the wake threshold), and the boost regulator wakes up and generates the pulse-width modulation (PWM) pulses to charge the output again. The hysteresis mode allows the regulator to act as the keep alive power supply.

In LDO mode, the output generates power from the SYS pin with at least a small 4.7 µF ceramic output capacitor. Using new innovative design techniques, the LDO provides ultralow quiescent current and superior transient performance for digital and RF applications, and supports noise sensitive applications.

In hybrid mode, the VIN and SYS pins both extract energy to the REG_OUT pin. When the load power is lower than the input power, the regulator exits LDO mode and obtains the energy only from the input side.

REG_D0 AND REG_D1

The REG_D0 and REG_D1 pins allow flexible configuration of the working mode of the regulated output. Table 6 details the working mode configuration set by these two pins.

Table 6. Regulated Output Working Mode Configuration

Working Mode	REG_D0	REG_D1
Boost Disable	Low	Not applicable
Boost Enable	High	Not applicable
LDO Disable	Not applicable	Low
LDO Enable	Not applicable	High

REGULATED OUTPUT CONFIGURATION

The 150 mA regulated output of the ADP5091/ADP5092 is available in eight fixed output voltage options ranging from 1.5 V to 3.6 V by connecting one resistor through the VID pin to the AGND pin. Table 7 shows the output voltage options set by the VID pin.

Table 7. Output Voltage Options Set by the VID Pin

VID Configuration	Output Voltage Set by the VID Pin
Short to Ground	Programmed with external resistors
Floating	V_{OUT} = 2.5 V
R_{VID} = 7 kΩ	V_{OUT} = 1.5 V
R_{VID} = 14 kΩ	V_{OUT} = 1.8 V
R_{VID} = 27.7 kΩ	V_{OUT} = 3.6 V
R_{VID} = 55.6 kΩ	V_{OUT} = 3.3 V
R_{VID} = 111 kΩ	V_{OUT} = 2.0 V
R_{VID} = 221 kΩ	V_{OUT} = 3.0 V
R_{VID} = 442 kΩ	V_{OUT} = 2.8 V

The external resistor divider or the VID pin can program the regulated output. The ratio of the two external resistors sets the adjustable output voltage range of 1.5 V to 3.6 V, as shown in Figure 47. The device acts as a servo to the output to maintain the voltage at the REG_FB pin at 1.0 V referenced to ground. The current in R1 is then equal to 1.0 V/R2, and the current in R1 is the current in R2 plus the REG_FB pin bias current. Calculate the output voltage by

$$V_{OUT} = 1.02\ V \times (1 + R1/R2) \quad (2)$$

where:

$V_{OUT} = V_{REG\_OUT}$.

See Figure 47 for *R1* and *R2*.

To minimize quiescent current, it is recommended to use large resistance values for R1 and R2.

REG_GOOD (ADP5092 ONLY)

A logic high on the REG_GOOD pin indicates that the REG_OUT voltage is above 92.5% (typical) of its nominal output for a delay time greater than approximately 2 ms. The logic high level on REG_GOOD is equal to the REG_OUT voltage, and the logic low level is ground. When the REG_OUT voltage falls below a 2% hysteresis (typical) of the rising threshold, the REG_GOOD pin goes low. The logic high level has about 11.6 kΩ internally in series to limit the available current.

ENERGY STORAGE CHARGE MANAGEMENT

Energy storage is connected to the BAT pin. The storage can be a rechargeable battery, super capacitor, or 100 µF or larger capacitor. The energy storage controller manages the charging and discharging operations, monitors the SYS pin voltage, and asserts the PGOOD signal high when it is above the threshold programmed at the SETPG pin.

When the BAT pin voltage exceeds the battery terminal charging threshold programmed at the TERM pin, the boost operation terminates to prevent battery overcharging. The battery terminal charging threshold is programmable from 2.2 V to 5.2 V. When the BAT voltage drops below the battery stop charging threshold level programmed at the SETSD pin, the switches between the BAT pin and the SYS pin are turned off to prevent a deep, destructive battery discharge, and the boost operates in asynchronous mode. Although there is no current limit at the SYS and the BAT pins, it is recommended to limit the system load current to lower than 1000 mA. The large system load current generates a droop between the SYS pin and the rechargeable battery at the BAT pin, with consideration given to the resistance of the SYS switch, the BAT switch, and the rechargeable battery internal resistance.

When no input source is attached, discharge the SYS pin to ground before attaching a storage element to the BAT pin. After hot plugging a charged storage element, release the SYS pin because a SYS voltage that is less than the end of the cold start operation threshold (V_{SYS_TH}) results in the BAT switch remaining off to protect the storage element until the SYS voltage reaches V_{SYS_TH}. The BAT switches remaining off can also be described as store mode, a state with the lowest leakage (3.5 nA typical) that allows a long store period without discharging the storage element on BAT.

BACKUP STORAGE PATH

The ADP5091/ADP5092 provide an optional backup storage energy path, an integrated backup controller, and two back to back power switches between the BACK_UP pin and the SYS pin. When the system operates at a condition where the harvested and stored energy is periodically insufficient, attach a backup energy storage element to the BACK_UP pin.

The backup controller enables when the SYS voltage exceeds the end of the cold start operation threshold (V_{SYS_TH}). Before the BAT voltage lowers the SETBK threshold, the backup switches turn off. While the BAT voltage is less than the SETBK threshold, the switches status depends on the voltage level of the BACK_UP pin and the BAT pin. The internal BACK_UP_Mx and BACK_UP control circuit automatically determine the BACK_UP switches (BACK_UP_M1 and BACK_UP_M2) on/off status and selects the high voltage terminal as the power source of SYS. The 190 mV (typical) comparator input offset of the BAT pin prevents the input source and the BAT pin from charging the BACK_UP pin (see Figure 44).

In addition, the backup storage element can bypass the cold startup with inrush current protection circuitry. Nevertheless, the current capability is only 250 µA (typical) when plugging in the backup battery before completing the cold start. It is recommended to restrict the system load current from the SYS pin to ensure that the power path can enter normal operation status. Table 9 explains the power path working state. For long-term store mode, disconnect the backup storage element and then discharge SYS to ground.

BACKUP AND BAT SELECTION THRESHOLD

To determine when to enable the BACK_UP function, the switch threshold on the BAT pin must be set by using external resistors at SETBK pin. When the BAT voltage is lower than the SETBK threshold, the internal BACK_UP_Mx control circuit automatically selects the high voltage terminal as the SYS power source. Figure 42 shows the V_{SETBK} falling threshold voltage given by Equation 3.

$$V_{SETBK} = V_{INT\_REF}\left(1+\frac{R_{BK1}}{R_{BK2}}\right) \quad (3)$$

The ADP5091/ADP5092 have an internal resistor, R_{SETBK_HYS} = 115 kΩ (typical), to program the hysteresis, given by Equation 4.

$$V_{SETBK\_HYS} = V_{SETBK} \times \frac{R_{SETBK\_HYS}}{R_E} \quad (4)$$

where R_E is the equivalent resistor of the four external configuration resistor dividers.

Considering the quiescent current consumption, the sum of the resistors that comprise the resistor divider (R_{SETBK_HYS}, R_{BK1}, and R_{BK2}) must be greater than 6 MΩ, that is,

$$R_{SETBK\_HYS} + R_{BK1} + R_{BK2} > 6\ \text{MΩ} \quad (5)$$

The equivalent resistor of the four external configuration resistor dividers (R_E) is equivalent to the paralleling value of the three resistor dividers.

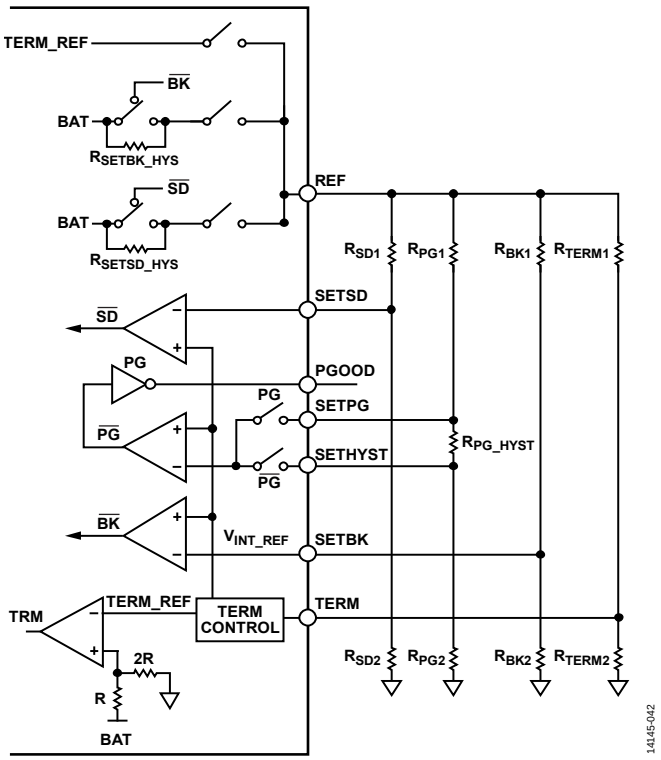

Figure 42. ADP5091/ADP5092 Program Paramater Setting

BATTERY OVERCHARGING PROTECTION

To prevent rechargeable batteries from being overcharged and damaged, the battery terminal charging threshold (V_{BAT_TERM}) must be set by using external resistors. Figure 42 shows the V_{BAT_TERM} rising threshold voltage given by Equation 6.

$$V_{BAT\_TERM} = \frac{3}{2} \times V_{INT\_REF} \times \left(1+\frac{R_{TERM1}}{R_{TERM2}}\right) \quad (6)$$

Considering the quiescent current consumption, the sum of the resistors must be more than 6 MΩ, that is,

$$R_{TERM1} + R_{TERM2} \geq 6\ \text{MΩ} \quad (7)$$

The battery terminal charging threshold is given by $V_{BAT\_TERM\_HYS}$, which is internally set to the battery terminal charging threshold minus an internal hysteresis voltage denoted by $V_{BAT\_TERM\_HYS}$. When the voltage at the battery exceeds the V_{BAT_TERM} threshold, the main boost regulator disables. The main boost starts again when the battery voltage falls below the $V_{BAT\_TERM\_HYS}$ level. When input energy is excessive, the VBAT pin voltage ripples between the V_{BAT_TERM} and the $V_{BAT\_TERM\_HYS}$ levels.

BATTERY DISCHARGING PROTECTION

To prevent rechargeable batteries from being deeply discharged and damaged, the battery stop discharging threshold (V_{SETSD}) must be set by using external resistors. Figure 42 shows the V_{SETSD} falling threshold voltage given by Equation 8.

$$V_{SETSD} = V_{INT\_REF}\left(1+\frac{R_{SD1}}{R_{SD2}}\right) \quad (8)$$

The ADP5091/ADP5092 have an internal resistor, R_{SETSD_HYS} = 115 kΩ (typical), to program the hysteresis, given by Equation 9.

$$V_{SETSD\_HYS} = V_{SETSD} \times \frac{R_{SETSD\_HYS}}{R_E} \quad (9)$$

Considering the quiescent current consumption, the sum of the resistors that comprise the resistor divider (R_{SETSD_HYS}, R_{SD1}, and R_{SD2}) must be more than 6 MΩ, that is,

$$R_{SETSD\_HYS} + R_{SD1} + R_{SD2} \geq 6\ \text{MΩ} \quad (10)$$

The equivalent resistor of the three external configuration resistor dividers (R_E) is equivalent to the paralleling value of the three resistor dividers.

POWER GOOD (PGOOD)

The ADP5091/ADP5092 allow users to set a programmable PGOOD voltage threshold, which indicates that the SYS voltage is at an acceptable level. It must be set by using external resistors. Figure 42 shows the V_{SETPG} falling threshold voltage given by Equation 11.

$$V_{SETPG\_FALLING} = V_{INT\_REF}\left(1 + \frac{R_{PG1}}{R_{PG2} + R_{PG\_HYST}}\right) \quad (11)$$

The SETHYST pin can program the hysteresis with an external resistor (R_{PG_HYST}) given by Equation 12.

$$V_{SETPG\_RISING} = V_{INT\_REF}\left(1 + \frac{R_{PG1} + R_{PG\_HYST}}{R_{PG2}}\right) \quad (12)$$

Considering the quiescent current consumption, the sum of the resistors that comprise the power-good resistor divider (R_{PG_HYST}, R_{PG1}, and R_{PG2}) must be more than 6 MΩ, that is,

$$R_{PG\_HYST} + R_{PG1} + R_{PG2} \geq 6\ M\Omega$$

The logic high level on PGOOD is equal to the SYS voltage and the logic low level is ground. The logic high level has approximately 11.6 kΩ (typical) internally in series to limit the available current. The $V_{SETPG\_FALLING}$ threshold must be greater than the V_{SETSD} threshold.

For the best operation of the system, use PGOOD to enable the system load or to turn on an ultralow power load switch or to drive an external positive channel field effect transistor (PFET) between SYS and the system load via an inverter to determine when the system load can be connected or removed (see Figure 48).

Table 8 shows programming threshold resistor examples corresponding to various voltages with a 10 MΩ resistor divider. Figure 43 shows various threshold voltages states.

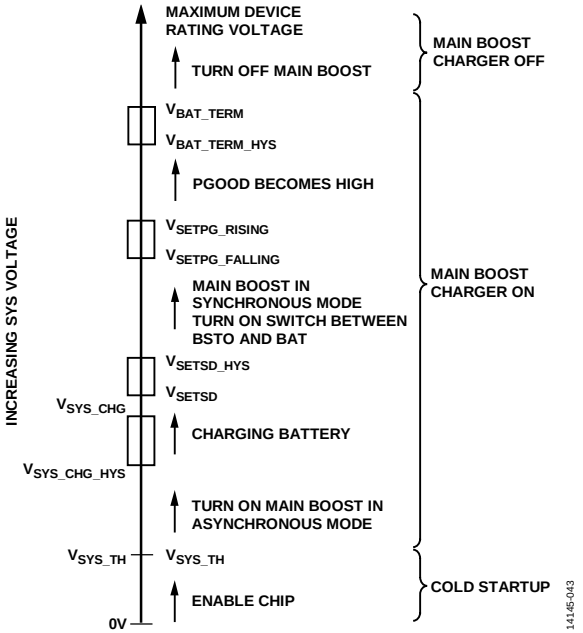

Figure 43. ADP5091/ADP5092 Various Threshold Voltages States (See Equation 8 and Equation 9)

POWER PATH WORKING FLOW

Figure 44 shows the power switches structure when the backup primary battery is used. During the cold start, when a primary battery connects to the BACK_UP pin, the S1 switch turns on. The primary battery with the Diode D1 forward voltage drop can be the SYS power source.

After completing the cold start, if the BAT voltage is above the SETBK falling threshold, the BACK_UP switches remain off. When the BAT voltage is lower than the SETBK falling threshold, the backup control automatically selects the high voltage terminal as the SYS power source as long as the SYS voltage is more than V_{SYS_CHG}. The backup control also prevents the BACK_UP primary battery from charging the BAT pin. Meanwhile, the BAT offset of the comparator prevents the input source from charging the BACK_UP primary battery. Table 9 shows the power path of the working state.

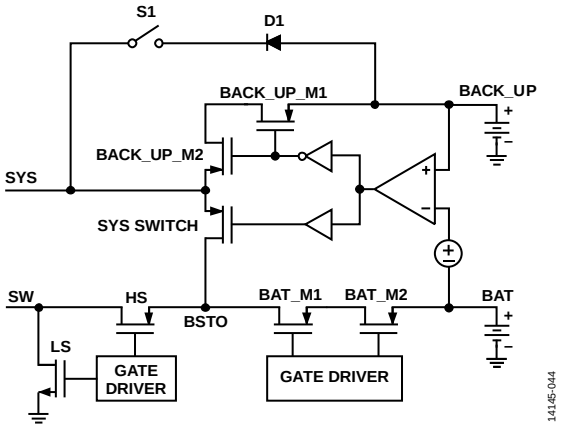

Figure 44. ADP5091/ADP5092 Power Switches Structure

CURRENT-LIMIT AND SHORT-CIRCUIT PROTECTION

The boost regulator and regulated output in hysteresis boost mode in the ADP5091/ADP5092 includes current-limit protection circuitry to limit the amount of positive current flowing through the low-side boost switch. The boost regulator current-limit protection circuitry is a cycle-by-cycle, three-level peak current-limit protection with a third level of 200 mA (typical), and the regulated output current-limit protection circuitry is 100 mA (typical). In LDO mode, the current-limit protection is designed to limit the current when the output load reaches 260 mA (typical). When the output load exceeds 260 mA, the output voltage reduces to maintain a constant current limit.

Although there is no current limit at the SYS and the BAT pins, it is recommended to limit the system load current to lower than 1000 mA. The total resistance of the SYS switch and the BAT switch (1.03 Ω, typical) generates a voltage drop when the system load sinks a large current from BAT. It is also necessary to consider the internal resistance of the storage elements connected to the BAT pin.

THERMAL SHUTDOWN

In the event that the ADP5091/ADP5092 junction temperature rises above 142°C, the thermal shutdown circuit turns off the switch between the BAT pin and the SYS pin to prevent the damage of the energy storage at a high ambient temperature. In addition, the boost operation terminates. A 15°C hysteresis is included, allowing the ADP5091/ADP5092 to return to operation when the on-chip temperature drops to less than 127°C. When exiting thermal shutdown, the boost and the energy storage controller resume their functions.

Table 8. Programming Threshold Resistors (See Figure 42)

Voltage Threshold (V)	R_{BK1}, R_{SD1}, and R_{PG1} (MΩ)	R_{BK2}, R_{SD2}, and R_{PG2} (MΩ)	R_{TERM1} (MΩ)	R_{TERM2} (MΩ)
2	5	5	Not applicable	Not applicable
2.1	5.23	4.75	Not applicable	Not applicable
2.2	5.49	4.53	3.2	6.81
2.3	5.62	4.32	3.48	6.49
2.4	5.9	4.12	3.74	6.2
2.5	6.04	4	4	6.04
2.6	6.19	3.83	4.22	5.76
2.7	6.34	3.74	4.42	5.6
2.8	6.49	3.57	4.64	5.36
2.9	6.6	3.48	4.87	5.23
3	6.65	3.32	5	5
3.1	6.8	3.24	5.11	4.87
3.2	6.81	3.09	5.36	4.7
3.3	6.98	3.01	5.49	4.53
3.4	6.98	2.94	5.6	4.42
3.5	7.15	2.87	5.76	4.3
3.6	7.15	2.8	5.9	4.12
3.7	7.32	2.7	5.9	4.02
3.8	7.32	2.61	6.04	3.92
3.9	7.5	2.55	6.19	3.83
4	7.5	2.5	6.2	3.74
4.1	7.5	2.43	6.34	3.65
4.2	7.68	2.37	6.49	3.57
4.3	7.68	2.32	6.49	3.48
4.4	7.68	2.26	6.6	3.4
4.5	7.87	2.21	6.65	3.32
4.6	7.87	2.15	6.8	3.24
4.7	7.87	2.15	6.81	3.2
4.8	7.87	2.1	6.81	3.09
4.9	7.87	2.05	6.98	3.09
5	8.06	2	6.98	3
5.1	8.06	1.96	6.98	2.94
5.2	8.06	1.91	7.15	2.87

Table 9. Power Path Working State (See Figure 44)

Backup Battery	Power Condition[1]	Main Boost	BAT_M1	BAT_M2	SYS Switch	BACK_UP_M1	BACK_UP_M2
Without	$V_{SYS\_CHG} > V_{SYS} > V_{SYS\_TH}$, $V_{SETSD} > V_{BAT}$	Asynchronous	Off	Off	On	Off	Off
	$V_{SYS} > V_{SYS\_CHG}$, $V_{SETSD} > V_{BAT}$	Asynchronous	On	Off	On	Off	Off
	$V_{BAT\_TERM} > V_{BAT} = V_{SYS} > V_{SETSD}$	Synchronous	On	On	On	Off	Off
	$V_{SYS} > V_{SYS\_TH}$, $V_{BAT} > V_{BAT\_TERM}$	Disabled	On	On	On	Off	Off
With	$V_{SYS\_CHG} > V_{SYS} > V_{SYS\_TH}$, $V_{SETSD} > V_{BAT}$	Asynchronous	Off	Off	On	Off	Off
	$V_{SYS} > V_{SYS\_CHG}$, $V_{SETSD} > V_{BAT}$, $V_{BACK\_UP} > V_{BAT}$	Asynchronous	On	Off	Off	On	On
	$V_{SYS} > V_{SYS\_TH}$, $V_{BAT} > V_{SETSD}$, $V_{BAT} > V_{SETBK}$	Synchronous	On	On	On	Off	Off
	$V_{SYS} > V_{SYS\_TH}$, $V_{BAT} > V_{SETSD}$, $V_{BAT} < V_{SETBK}$, $V_{BACK\_UP} > V_{BAT}$	Synchronous	On	On	Off	On	On
	$V_{SYS} < V_{SYS\_TH}$	Disabled	Off	Off	On	Off	Off

[1] V_{BACK_UP} is the voltage on the BACK_UP pin, and V_{SETBK} is the threshold of the SETBK pin.

APPLICATIONS INFORMATION

The ADP5091/ADP5092 extract the energy from the VIN pin to charge the SYS and the BAT pins. This process occurs in three stages: cold start, asynchronous boost, and synchronous boost. This section describes the procedures for selecting the external components to maintain the energy transmission system with the layout and assembly considerations.

ENERGY HARVESTER SELECTION

The energy harvester input source must provide a minimum level of power for cold start, asynchronous boost, and synchronous boost. To estimate the minimum input power required to complete the cold start using the following equation:

$$V_{IN} \times I_{IN} \times \eta_{COLD} > V_{SYS\_TH} \times I_{SYS\_LOAD} \quad (13)$$

where:

V_{IN} is clamped to V_{IN_COLD} = 380 mV (typical), which indicates the minimum input voltage for cold start.

I_{IN} is the input current.

η_{COLD} is the cold start efficiency, which is about 5% to 7%.

(V_{SYS_TH} is the end of cold start operation.

I_{SYS_LOAD} is the system load current of the SYS pin. Minimizing the system load accelerates the cold start. Programming the PGOOD threshold to enable the system load current is recommended.

After the ADP5091/ADP5092 complete the cold start, the MPPT function enables. To meet the average system load current, the input source must provide the boost regulator with enough power to fully charge the storage element while the system is in low power or sleep mode. To estimate the power required by the system, use the following equation:

$$V_{IN} \times I_{IN} \times \eta_{BOOST} > V_{BAT\_TERM} \times (I_{STR\_LEAK} + I_{SYS\_LOAD}) \quad (14)$$

where:

V_{IN} is regulated to the MPPT pin voltage (MPPT ratio × OCV).

I_{IN} is the input current.

η_{BOOST} is the boost regulator efficiency. See Figure 5 through Figure 12 in the Typical Performance Characteristics section for more information.

V_{BAT_TERM} is the battery terminal charging threshold (see Table 1).

I_{STR_LEAK} is the storage element leakage current at the BAT pin.

I_{SYS_LOAD} is the average system load current of the SYS pin.

Table 10. Recommended Solar Cells

Vendor	Device Type
Alta Devices	GaAs
Fujikura	Dye sensitized solar cell
Gcell	Dye sensitized solar cell
ElectricFilm	Dye sensitized solar cell

ENERGY STORAGE ELEMENT SELECTION

To protect the storage element from overcharging or overdischarging, the storage element must be connected to the BAT pin and the system load tied to the SYS pin. The ADP5091/ADP5092 support many types of storage elements, such as rechargeable batteries, super capacitors, and conventional capacitors. A storage element with a 100 µF equivalent capacitance is required to filter the pulse currents of the PFM switching converter. The storage element capacity must provide the entire system load when the input source is no longer generating power.

If there is a high pulse current or the storage element has significant impedance, it may be necessary to increase the SYS capacitor from the 4.7 µF minimum, or add additional capacitance to the BAT pin to prevent a droop in the SYS voltage. Note that increasing the SYS capacitor causes the boost regulator to operate in the less efficient cold start stage for a longer period at startup. If the application is unable to accept the longer cold start time, place the additional capacitor parallel to the storage element. See the Capacitor Selection section for more information.

INDUCTOR SELECTION

The boost regulator needs an appropriate inductor for proper operation. The inductor saturation current must be at least 30% higher than the expected peak inductor currents, as well as a low series resistance (DCR) to maintain high efficiency. The boost regulator internal control circuitry is designed to optimize the efficiency and control the switching behavior with a nominal inductance of 22 µH ± 20%. Table 11 lists some of the recommended inductors.

Table 11. Recommended Inductors

Vendor	Device No.	L (µH)	I_{SAT} (A)[1]	I_{RMS} (A)[2]	DCR (mΩ)
Würth Elektronik	74437324220	22	2	1	470
	744042220	22	0.6	0.88	255
Coilcraft	LPS4018-223M	22	0.8	0.65	360

[1] I_{SAT} is the dc current that causes the 20% inductance drop from its value without current.
[2] I_{RMS} is the current that causes a 20°C rise from a 25°C ambient temperature.

CAPACITOR SELECTION

Low leakage capacitors are required for ultralow power applications that are sensitive to the leakage current. Any leakage from the capacitors reduces efficiency, increases the quiescent current, and degrades the MPPT effectiveness.

Input Capacitor

A capacitor (C_{IN}) connected to the VIN pin and the PGND pin stores energy from the input source. For the energy harvester, capacitive behavior dominates the source impedance. Scale the input capacitor according to the value of the output capacitance of the energy harvester; a minimum of 10 µF is recommended.

For the primary battery application, a larger capacitance helps to reduce the input voltage ripple and keeps the source current stable to extend the battery life.

SYS Capacitor

The ADP5091/ADP5092 require two capacitors to be connected between the SYS pin and the PGND pin. Connect a low ESR ceramic capacitor of at least 4.7 µF parallel to a high frequency, 0.1 µF bypass capacitor. Connect the bypass capacitor as close as possible between SYS and PGND.

REG_OUT Capacitor

The ADP5091/ADP5092 regulated output is designed for operation with small, space-saving ceramic capacitors but functions with the most commonly used capacitors as long as care is taken with regard to the effective series resistance (ESR) value. The ESR of the output capacitor affects stability of the LDO control loop. A minimum capacitance of 4.7 µF with an ESR of 1 Ω or less is recommended to ensure stability of the regulated output. Transient response to changes in load current is also affected by output capacitance. Using a larger value of output capacitance improves the transient response of the regulated output to large changes in load current.

CBP Capacitor

The operation of the MPPT pin depends on the sampled value of the OCV. The voltage stored on the CBP capacitor regulates to the VIN pin. This capacitor is sensitive to leakage because the holding period is around 16 sec. As the capacitor voltage drops due to leakage, the VIN regulation voltage also drops and influences the effectiveness of MPPT. When the IC junction temperature exceeds 85°C, a larger capacitance is beneficial to the effectiveness of MPPT, and for a higher CPB pin leakage current. It is recommended to keep the same RC time constant of the MPPT resistors and CBP capacitor (up to 22 µF) as shown in the typical application circuit in Figure 45. Considering the time constant of the MPPT resistor divide and the CBP capacitor, a low leakage X7R or C0G 10 nF ceramic capacitor is recommended.

LAYOUT AND ASSEMBLY CONSIDERATIONS

Carefully consider the printed circuit board (PCB) layout during the design of the switching power supply, especially at high peak currents and high switching frequency. Therefore, it is recommended to use wide and short traces for the main power path and the power ground paths. Place the input capacitors, output capacitors, inductor, and storage elements as close as possible to the IC. It is most important for the boost regulator to minimize the power path from output to ground. Therefore, place the output capacitor as close as possible between the SYS pin and the PGND pin. Keep a minimum power path from the input capacitor to the inductor from the VIN pin to the PGND pin. Place the input capacitor as close as possible between the VIN pin and the PGND pin, and place the inductor close to the VIN pin and the SW pin. It is best to use vias and bottom traces for connecting the inductors to their respective pins. To minimize noise pickup by the high impedance threshold setting nodes (REF, TERM, SETBK, SETSD, and SETPG), place the external resistors close to the IC with short traces.

The CBP capacitor must hold the MPPT voltage for 16 sec, because any leakage can degrade the MPPT effectiveness. During board assembly and cleaning, contaminants such as solder flux and residue may form parasitic resistance to ground, especially in humid environments with fast airflow. Contamination can significantly degrade the voltage regulation and change threshold levels set by the external resistors. Therefore, it is recommended that no ground planes be poured near the CBP capacitor or the threshold setting resistors. In addition, carefully clean the boards. If possible, clean ionic contamination with deionized water for the CBP capacitor and the threshold setting resistors.

TYPICAL APPLICATION CIRCUITS

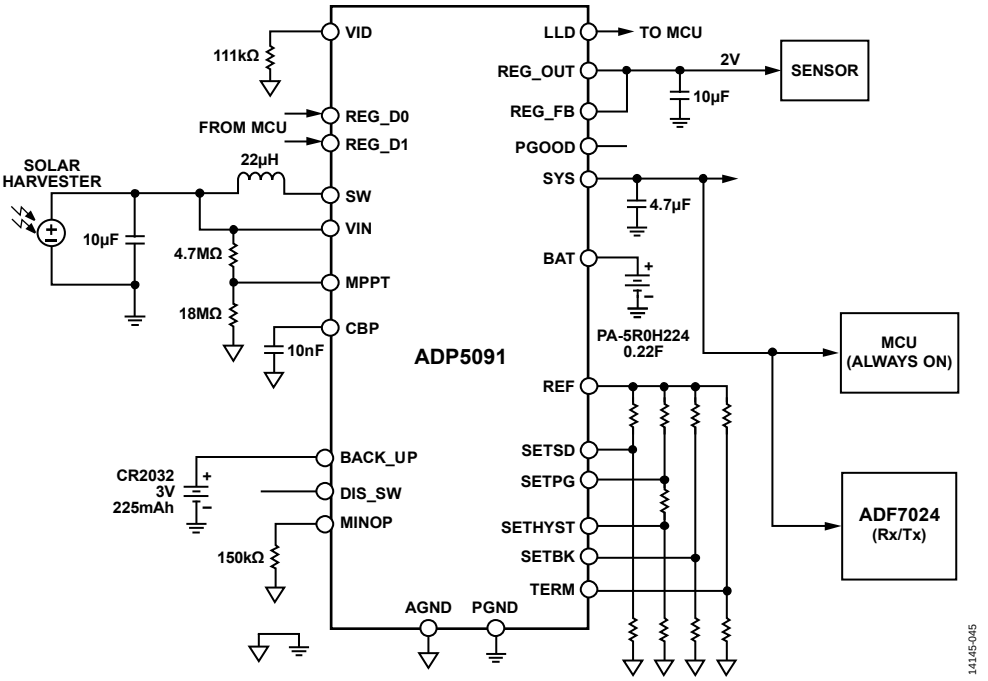

Figure 45. ADP5091-Based Energy Harvester Wireless Sensor Application with PV Cell as the Harvesting Energy Source (Trony 0.7 V, 60 µA, Alta Devices 0.72 V, 42 µA, Gcell 1.1 V, 100 µA), Cooper Bussmann Super Capacitor PA-5R0H224 as the Harvested Energy Storage, and Panasonic Primary Li-Ion Coin Cell CR2032 as the Backup Battery

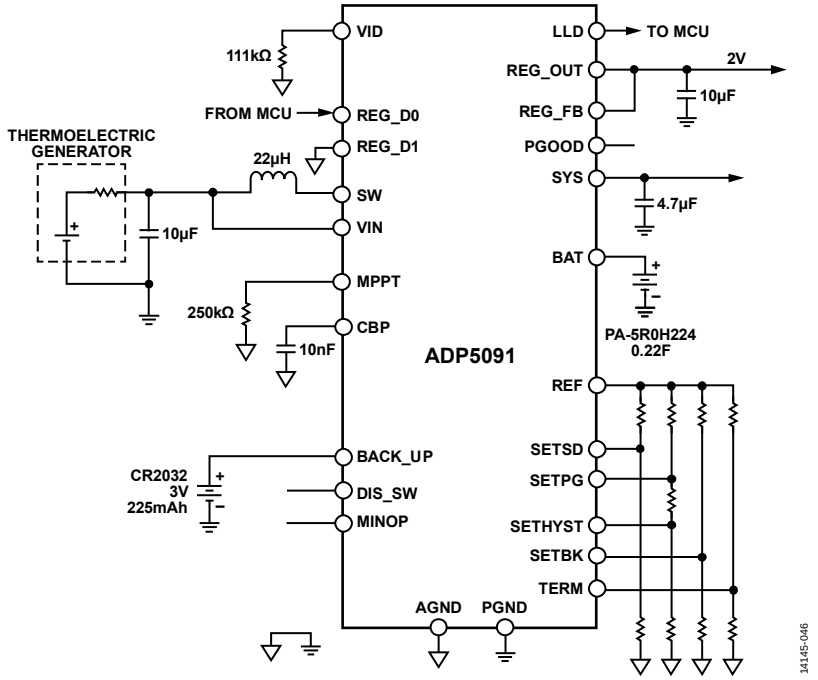

Figure 46. ADP5091-Based Energy Harvester Circuit with a Thermoelectric Generator as the Harvesting Energy Source, Cooper Bussmann Super Capacitor PA-5R0H224 as the Harvested Energy Storage, and Panasonic Primary Li-Ion Coin Cell CR2032 as the Backup Battery

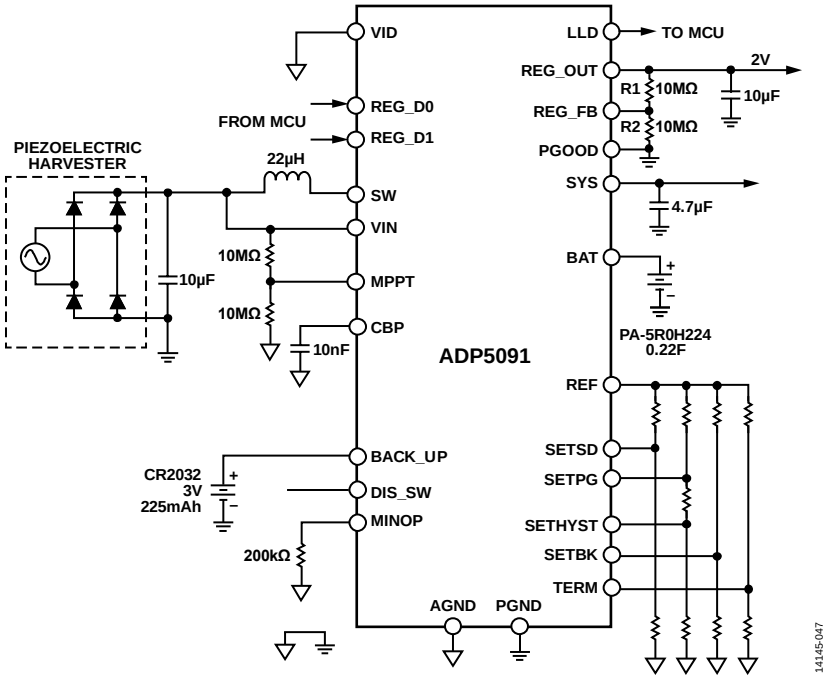

Figure 47. ADP5091-Based Energy Harvester Circuit with a Piezoelectric Generator as the Harvesting Energy Source, Cooper Bussmann Super Capacitor PA-5R0H224 as the Harvested Energy Storage, and Panasonic Primary Li-Ion Coin Cell CR2032 as the Backup Battery

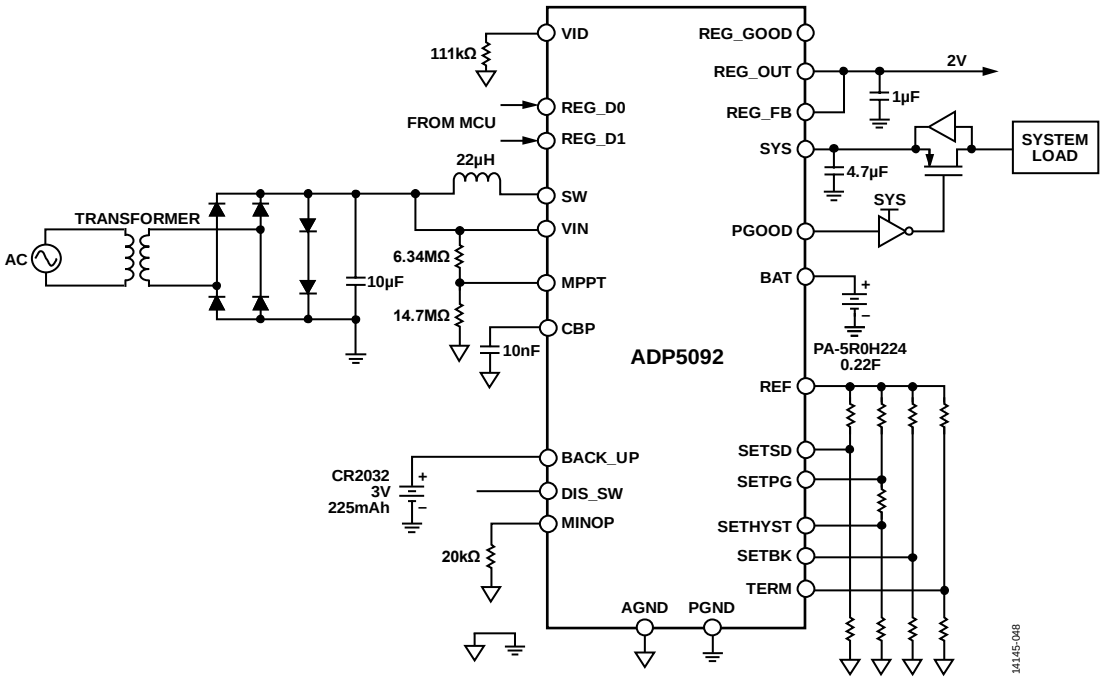

Figure 48. ADP5092 AC Input Source and PGOOD Function Determines the Time to Enable the System Load

FACTORY PROGRAMMABLE OPTIONS

To order a device with options other than the default options, contact a local Analog Devices, Inc., sales or distribution representative.

Table 12. Input Current-Limit Options

Option	Description
Option 0	200 mA (default)
Option 1	300 mA

Table 13. VIN Open Circuit Voltage Sampling Cycle Options

Option	Description
Option 0	4 sec
Option 1	8 sec
Option 2	16 sec (default)
Option 3	32 sec

OUTLINE DIMENSIONS

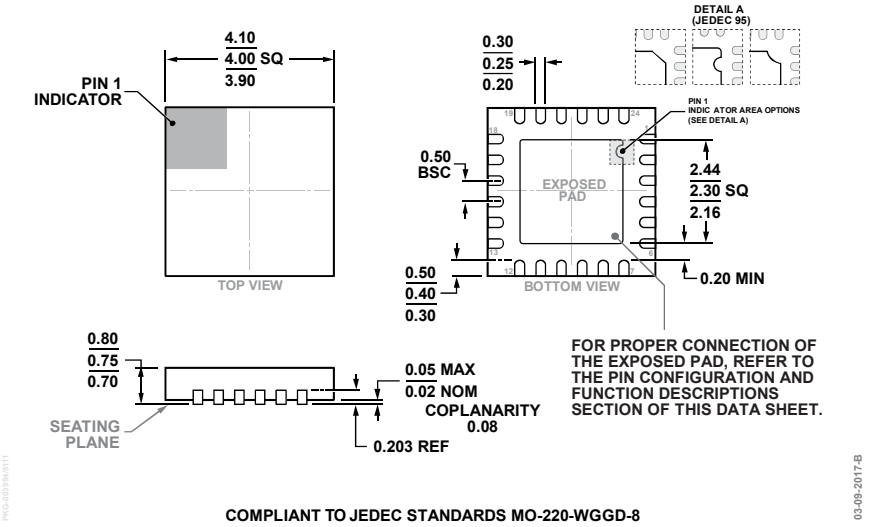

Figure 49. 24-Lead Lead Frame Chip Scale Package [LFCSP]
4 mm × 4 mm Body and 0.75 mm Package Height
(CP-24-14)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
ADP5091ACPZ-1-R7	−40°C to + 125°C	24-Lead Lead Frame Chip Scale Package [LFCSP], 200 mA Input Peak Current	CP-24-14
ADP5091ACPZ-2-R7	−40°C to + 125°C	24-Lead Lead Frame Chip Scale Package [LFCSP], 300 mA Input Peak Current	CP-24-14
ADP5092ACPZ-1-R7	−40°C to + 125°C	24-Lead Lead Frame Chip Scale Package [LFCSP], 200 mA Input Peak Current	CP-24-14
ADP5091-1-EVALZ		Evaluation Board	
ADP5091-2-EVALZ		Evaluation Board with Solar Harvester and Super Capacitor	
ADP5092-1-EVALZ		Evaluation Board	

[1] Z = RoHS Compliant Part.