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REVISION HISTORY

9/07—Rev. B to Rev. C

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7/07—Rev. A to Rev. B

Added Backside-Coated WLCSP Package ... Universal
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7/06—Rev. 0 to Rev. A

Added WLCSP Package ... Universal
Added Figure 4 ... 7
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1/05—Revision 0: Initial Version

SPECIFICATIONS

V_{CCY} = 1.65 V to 5.5 V, V_{CCA} = 1.15 V to V_{CCY}, GND = 0 V. All specifications T_{MIN} to T_{MAX}, unless otherwise noted. [1]

Table 1.

Parameter	Symbol	Conditions	Min	Typ[2]	Max	Unit
LOGIC INPUTS/OUTPUTS						
A Side						
Input High Voltage[3]	V_{IHA}	V_{CCA} = 1.15 V	V_{CCA} – 0.3			V
	V_{IHA}	V_{CCA} = 1.2 V to 5.5 V	0.65 × V_{CCA}			V
Input Low Voltage[3]	V_{ILA}				0.35 × V_{CCA}	V
Output High Voltage	V_{OHA}	V_Y = V_{CCY}, I_{OH} = 20 µA, see Figure 29	V_{CCA} – 0.4			V
Output Low Voltage	V_{OLA}	V_Y = 0 V, I_{OL} = 20 µA, see Figure 29			0.4	V
Capacitance[3]	C_A	f = 1 MHz, EN = 0, see Figure 34		10		pF
Leakage Current	$I_{LA, HIGH-Z}$	V_A = 0 V or V_{CCA}, EN = 0, see Figure 31			±1	µA
Y Side						
Input High Voltage[3]	V_{IHY}		0.65 × V_{CCY}			V
Input Low Voltage[3]	V_{ILY}				0.35 × V_{CCY}	V
Output High Voltage	V_{OHY}	V_A = V_{CCA}, I_{OH} = 20 µA, see Figure 30	V_{CCY} – 0.4			V
Output Low Voltage	V_{OLY}	V_A = 0 V, I_{OL} = 20 µA, see Figure 30			0.4	V
Capacitance[3]	C_Y	f = 1 MHz, EN = 0, see Figure 35		6.8		pF
Leakage Current	$I_{LY, HIGH-Z}$	V_Y = 0 V or V_{CCY}, EN = 0, see Figure 32			±1	µA
Enable (EN)						
Input High Voltage[3]	V_{IHEN}					
ADG3308 (TSSOP, LFCSP)			0.65 × V_{CCY}			V
ADG3308-1/ADG3308-2 (WLCSP)		V_{CCA} = 1.15 V	V_{CCA} – 0.3			V
		V_{CCA} = 1.2 V to 5.5 V	0.65 × V_{CCA}			V
Input Low Voltage[3]	V_{ILEN}					
ADG3308 (TSSOP, LFCSP)					0.35 × V_{CCY}	V
ADG3308-1/ADG3308-2 (WLCSP)					0.35 × V_{CCA}	V
Leakage Current	I_{LEN}	V_{EN} = 0 V or V_{CCY}, V_A = 0 V, see Figure 33			±1	µA
Capacitance[3]	C_{EN}			4.5		pF
Enable Time[3]	t_{EN}	R_S = R_T = 50 Ω, V_A = 0 V or V_{CCA} (A→Y), V_Y = 0 V or V_{CCY} (Y→A), see Figure 36		1	1.8	µs
SWITCHING CHARACTERISTICS[3]						
3.3 V ± 0.3 V ≤ V_{CCA} ≤ V_{CCY}, V_{CCY} = 5 V ± 0.5 V						
A→Y Level Translation		R_S = R_T = 50 Ω, C_L = 50 pF, see Figure 37				
Propagation Delay	$t_{P, A→Y}$			6	10	ns
Rise Time	$t_{R, A→Y}$			2	3.5	ns
Fall Time	$t_{F, A→Y}$			2	3.5	ns
Maximum Data Rate	$D_{MAX, A→Y}$		50			Mbps
Channel-to-Channel Skew	$t_{SKEW, A→Y}$			2	4	ns
Part-to-Part Skew	$t_{PPSKEW, A→Y}$				3	ns
Y→A Level Translation		R_S = R_T = 50 Ω, C_L = 15 pF, see Figure 38				
Propagation Delay	$t_{P, Y→A}$			4	7	ns
Rise Time	$t_{R, Y→A}$			1	3	ns
Fall Time	$t_{F, Y→A}$			3	7	ns
Maximum Data Rate	$D_{MAX, Y→A}$		50			Mbps
Channel-to-Channel Skew	$t_{SKEW, Y→A}$			2	3.5	ns
Part-to-Part Skew	$t_{PPSKEW, Y→A}$				2	ns

Parameter	Symbol	Conditions	Min	Typ[2]	Max	Unit
1.8 V ± 0.15 V ≤ V_{CCA} ≤ V_{CCY}, V_{CCY} = 3.3 V ± 0.3 V						
A→Y Level Translation		R_S = R_T = 50 Ω, C_L = 50 pF, see Figure 37				
Propagation Delay	$t_{P, A→Y}$			8	11	ns
Rise Time	$t_{R, A→Y}$			2	5	ns
Fall Time	$t_{F, A→Y}$			2	5	ns
Maximum Data Rate	$D_{MAX, A→Y}$		50			Mbps
Channel-to-Channel Skew	$t_{SKEW, A→Y}$			2	4	ns
Part-to-Part Skew	$t_{PPSKEW, A→Y}$				4	ns
Y→A Level Translation		R_S = R_T = 50 Ω, C_L = 15 pF, see Figure 38				
Propagation Delay	$t_{P, Y→A}$			5	8	ns
Rise Time	$t_{R, Y→A}$			2	3.5	ns
Fall Time	$t_{F, Y→A}$			2	3.5	ns
Maximum Data Rate	$D_{MAX, Y→A}$		50			Mbps
Channel-to-Channel Skew	$t_{SKEW, Y→A}$			2	3	ns
Part-to-Part Skew	$t_{PPSKEW, Y→A}$				3	ns
1.15 V to 1.3 V ≤ V_{CCA} ≤ V_{CCY}, V_{CCY} = 3.3 V ± 0.3 V						
A→Y Level Translation		R_S = R_T = 50 Ω, C_L = 50 pF, see Figure 37				
Propagation Delay	$t_{P, A→Y}$			9	18	ns
Rise Time	$t_{R, A→Y}$			3	5	ns
Fall Time	$t_{F, A→Y}$			2	5	ns
Maximum Data Rate	$D_{MAX, A→Y}$		40			Mbps
Channel-to-Channel Skew	$t_{SKEW, A→Y}$			2	5	ns
Part-to-Part Skew	$t_{PPSKEW, A→Y}$				10	ns
Y→A Level Translation		R_S = R_T = 50 Ω, C_L = 15 pF, see Figure 38				
Propagation Delay	$t_{P, Y→A}$			5	9	ns
Rise Time	$t_{R, Y→A}$			2	4	ns
Fall Time	$t_{F, Y→A}$			2	4	ns
Maximum Data Rate	$D_{MAX, Y→A}$		40			Mbps
Channel-to-Channel Skew	$t_{SKEW, Y→A}$			2	4	ns
Part-to-Part Skew	$t_{PPSKEW, Y→A}$				4	ns
1.15 V to 1.3 V ≤ V_{CCA} ≤ V_{CCY}, V_{CCY} = 1.8 V ± 0.3 V						
A→Y Level Translation		R_S = R_T = 50 Ω, C_L = 50 pF, see Figure 37				
Propagation Delay	$t_{P, A→Y}$			12	25	ns
Rise Time	$t_{R, A→Y}$			7	12	ns
Fall Time	$t_{F, A→Y}$			3	5	ns
Maximum Data Rate	$D_{MAX, A→Y}$		25			Mbps
Channel-to-Channel Skew	$t_{SKEW, A→Y}$			2	5	ns
Part-to-Part Skew	$t_{PPSKEW, A→Y}$				15	ns
Y→A Level Translation		R_S = R_T = 50 Ω, C_L = 15 pF, see Figure 38				
Propagation Delay	$t_{P, Y→A}$			14	35	ns
Rise Time	$t_{R, Y→A}$			5	16	ns
Fall Time	$t_{F, Y→A}$			2.5	6.5	ns
Maximum Data Rate	$D_{MAX, Y→A}$		25			Mbps
Channel-to-Channel Skew	$t_{SKEW, Y→A}$			3	6.5	ns
Part-to-Part Skew	$t_{PPSKEW, Y→A}$				23.5	ns

Parameter	Symbol	Conditions	Min	Typ[2]	Max	Unit
2.5 V ± 0.2 V ≤ V_{CCA} ≤ V_{CCY}, V_{CCY} = 3.3 V ± 0.3 V						
A→Y Level Translation		R_S = R_T = 50 Ω, C_L = 50 pF, see Figure 37				
Propagation Delay	$t_{P, A→Y}$			7	10	ns
Rise Time	$t_{R, A→Y}$			2.5	4	ns
Fall Time	$t_{F, A→Y}$			2	5	ns
Maximum Data Rate	$D_{MAX, A→Y}$		60			Mbps
Channel-to-Channel Skew	$t_{SKEW, A→Y}$			1.5	2	ns
Part-to-Part Skew	$t_{PPSKEW, A→Y}$				4	ns
Y→A Level Translation		R_S = R_T = 50 Ω, C_L = 15 pF, see Figure 38				
Propagation Delay	$t_{P, Y→A}$			5	8	ns
Rise Time	$t_{R, Y→A}$			1	4	ns
Fall Time	$t_{F, Y→A}$			3	5	ns
Maximum Data Rate	$D_{MAX, Y→A}$		60			Mbps
Channel-to-Channel Skew	$t_{SKEW, Y→A}$			2	3	ns
Part-to-Part Skew	$t_{PPSKEW, Y→A}$				3	ns
POWER REQUIREMENTS						
Power Supply Voltages	V_{CCA}	V_{CCA} ≤ V_{CCY}	1.15		5.5	V
	V_{CCY}		1.65		5.5	V
Quiescent Power Supply Current	I_{CCA}	V_A = 0 V or V_{CCA}, V_Y = 0 V or V_{CCY}, V_{CCA} = V_{CCY} = 5.5 V, EN = V_{CCY}		0.17	1	µA
	I_{CCY}	V_A = 0 V or V_{CCA}, V_Y = 0 V or V_{CCY}, V_{CCA} = V_{CCY} = 5.5 V, EN = V_{CCY}		0.27	1	µA
Three-State Mode Power Supply Current	$I_{HIGH-ZA}$	V_{CCA} = V_{CCY} = 5.5 V, EN = 0		0.1	1	µA
	$I_{HIGH-ZY}$	V_{CCA} = V_{CCY} = 5.5 V, EN = 0		0.1	1	µA

[1] Temperature range is −40°C to +85°C (B Version) for the TSSOP, the LFCSP, the WLCSP, and the backside-coated WLCSP.
[2] All typical values are at T_A = 25°C, unless otherwise noted.
[3] Guaranteed by design; not subject to production test.

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 2.

Parameter	Rating
V_{CCA} to GND	−0.3 V to +7 V
V_{CCY} to GND	V_{CCA} to +7 V
Digital Inputs (A)	−0.3 V to (V_{CCA} + 0.3 V)
Digital Inputs (Y)	−0.3 V to (V_{CCY} + 0.3 V)
EN to GND	−0.3 V to +7 V
Operating Temperature Range	
Extended Industrial Range (B Version)	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature	150°C
θ_{JA} Thermal Impedance	
20-Lead TSSOP	78°C/W
20-Lead LFCSP	30.4°C/W
20-Ball WLCSP	100°C/W
20-Ball Backside-Coated WLCSP	100°C/W
Lead Temperature, Soldering (10 sec)	300°C
IR Reflow, Peak Temperature (<20 sec)	260°C (+0°C/−5°C)

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Only one absolute maximum rating may be applied at any one time.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

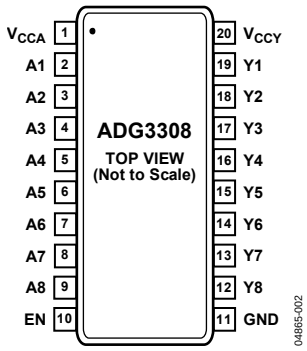


Figure 2. 20-Lead TSSOP

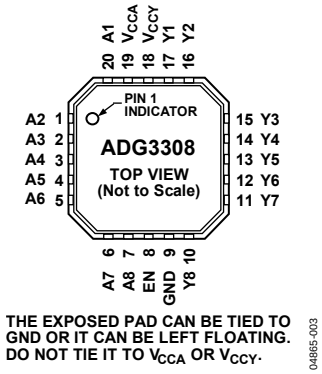


Figure 3. 20-Lead LFCSP

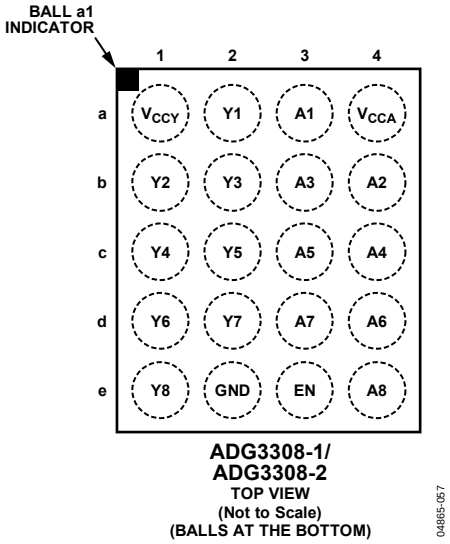


Figure 4. 20-Ball WLCSP

Table 3. Pin Function Descriptions

Pin/Ball No.				
TSSOP	**LFCSP**	**WLCSP**	**Mnemonic**	**Description**
1	19	a4	V_{CCA}	Power Supply. Power supply voltage input for the A1 I/O pin to the A8 I/O pin ($1.15\ V \le V_{CCA} < V_{CCY}$).
2	20	a3	A1	Input/Output A1. Referenced to V_{CCA}.
3	1	b4	A2	Input/Output A2. Referenced to V_{CCA}.
4	2	b3	A3	Input/Output A3. Referenced to V_{CCA}.
5	3	c4	A4	Input/Output A4. Referenced to V_{CCA}.
6	4	c3	A5	Input/Output A5. Referenced to V_{CCA}.
7	5	d4	A6	Input/Output A6. Referenced to V_{CCA}.
8	6	d3	A7	Input/Output A7. Referenced to V_{CCA}.
9	7	e4	A8	Input/Output A8. Referenced to V_{CCA}.
10	8	e3	EN	Active High Enable Input.
11	9	e2	GND	Ground.
12	10	e1	Y8	Input/Output Y8. Referenced to V_{CCY}.
13	11	d2	Y7	Input/Output Y7. Referenced to V_{CCY}.
14	12	d1	Y6	Input/Output Y6. Referenced to V_{CCY}.
15	13	c2	Y5	Input/Output Y5. Referenced to V_{CCY}.
16	14	c1	Y4	Input/Output Y4. Referenced to V_{CCY}.
17	15	b2	Y3	Input/Output Y3. Referenced to V_{CCY}.
18	16	b1	Y2	Input/Output Y2. Referenced to V_{CCY}.
19	17	a2	Y1	Input/Output Y1. Referenced to V_{CCY}.
20	18	a1	V_{CCY}	Power Supply. Power supply voltage input for the Y1 I/O pin to the Y8 I/O pin ($1.65\ V \le V_{CCY} \le 5.5\ V$).

TYPICAL PERFORMANCE CHARACTERISTICS

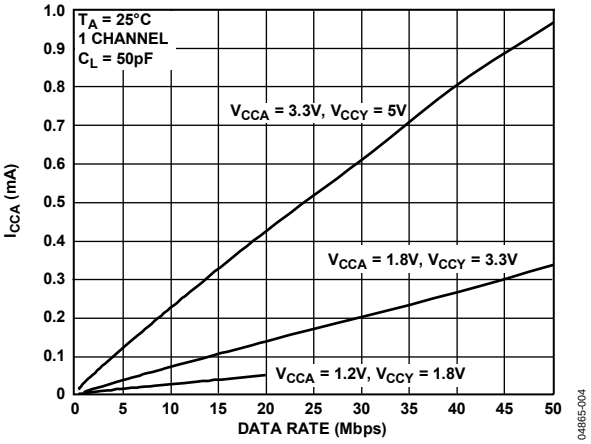


Figure 5. I_{CCA} vs. Data Rate (A→Y Level Translation)

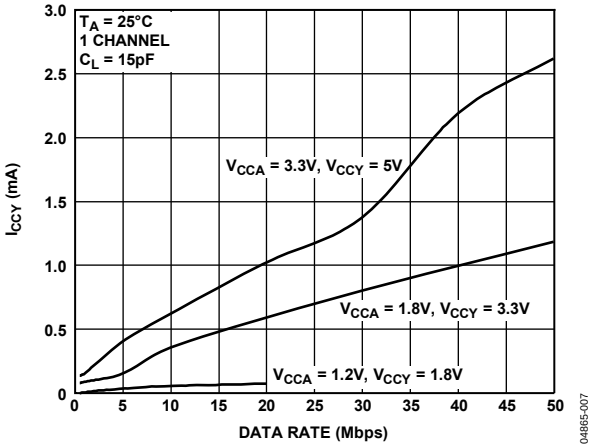


Figure 8. I_{CCY} vs. Data Rate (Y→A Level Translation)

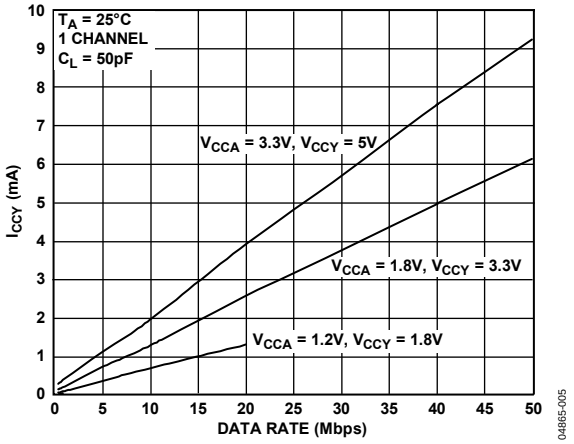


Figure 6. I_{CCY} vs. Data Rate (A→Y Level Translation)

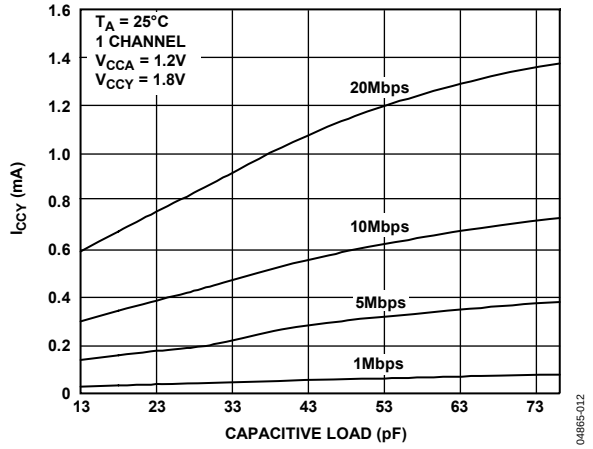


Figure 9. I_{CCY} vs. Capacitive Load at Pin Y for A→Y (1.2 V→1.8 V) Level Translation

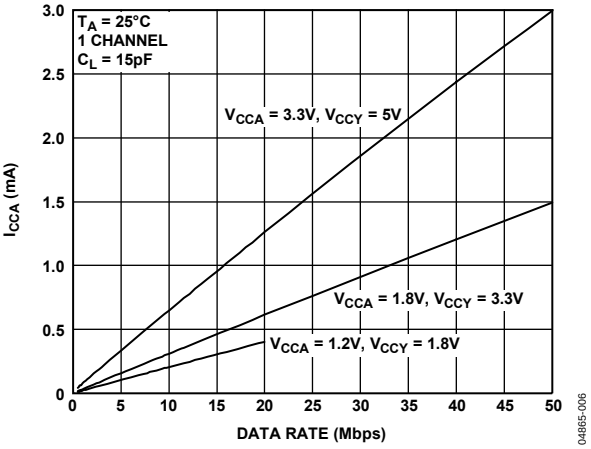


Figure 7. I_{CCA} vs. Data Rate (Y→A Level Translation)

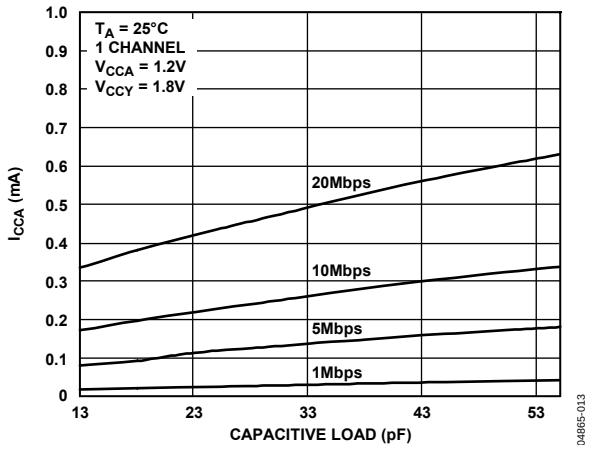


Figure 10. I_{CCA} vs. Capacitive Load at Pin A for Y→A (1.8 V→1.2 V) Level Translation

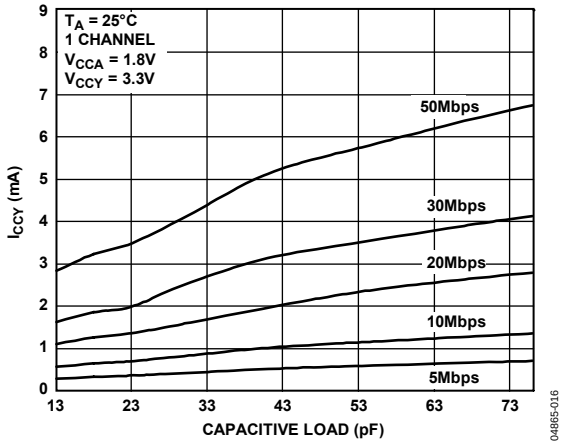


Figure 11. I_{CCY} vs. Capacitive Load at Pin Y for A→Y (1.8 V→3.3 V) Level Translation

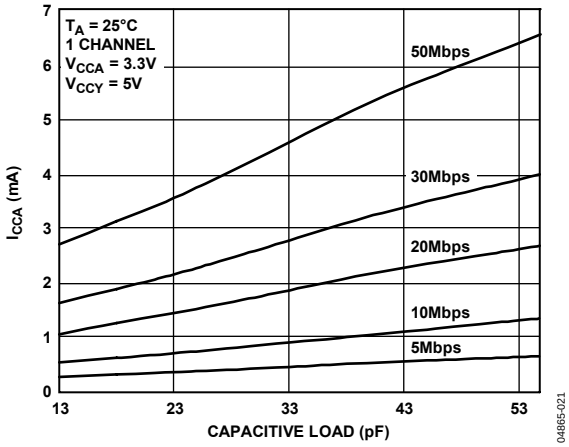


Figure 14. I_{CCA} vs. Capacitive Load at Pin A for Y→A (5 V→3.3 V) Level Translation

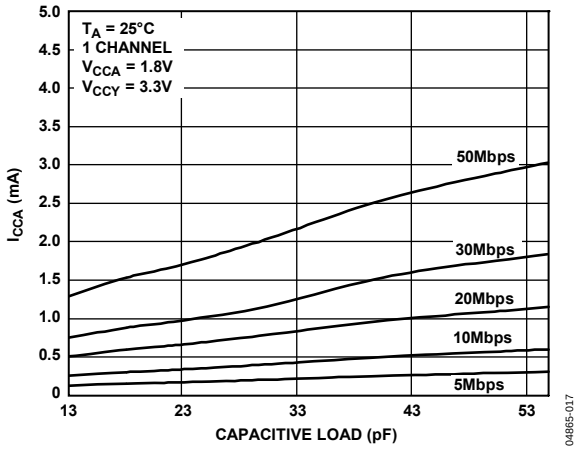


Figure 12. I_{CCA} vs. Capacitive Load at Pin A for Y→A (3.3 V→1.8 V) Level Translation

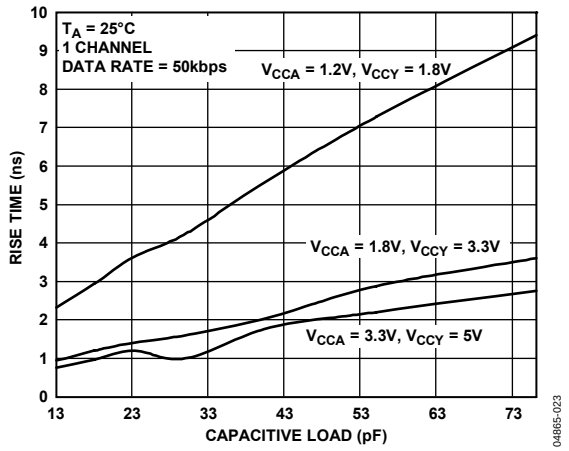


Figure 15. Rise Time vs. Capacitive Load at Pin Y (A→Y Level Translation)

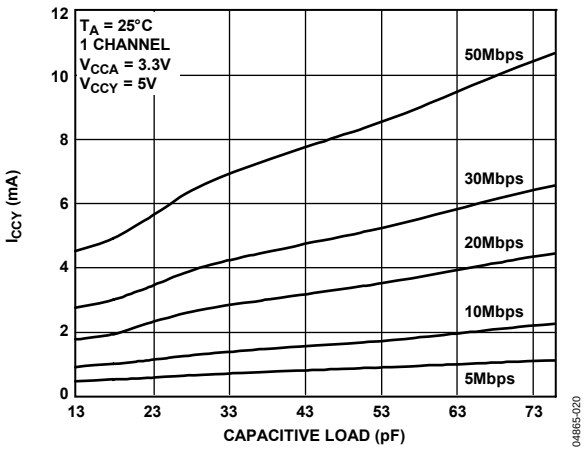


Figure 13. I_{CCY} vs. Capacitive Load at Pin Y for A→Y (3.3 V→5 V) Level Translation

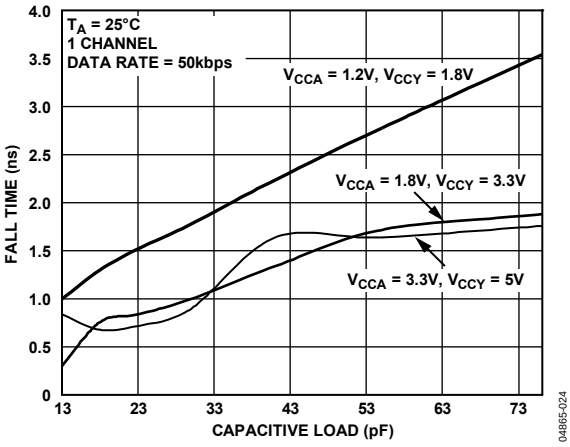


Figure 16. Fall Time vs. Capacitive Load at Pin Y (A→Y Level Translation)

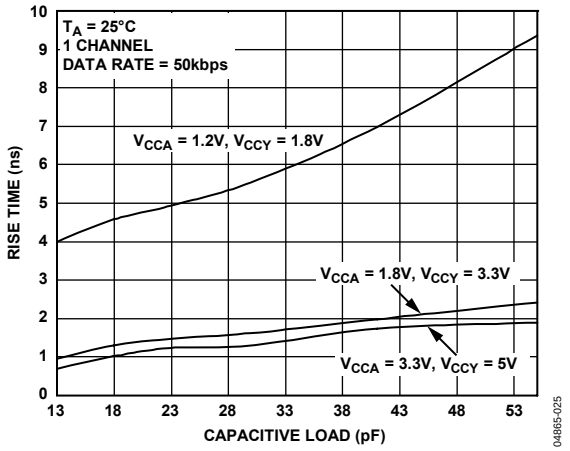


Figure 17. Rise Time vs. Capacitive Load at Pin A (Y→A Level Translation)

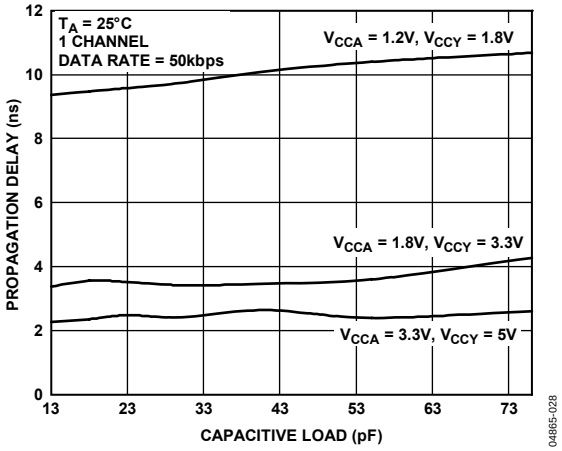


Figure 20. Propagation Delay (t_{PHL}) vs. Capacitive Load at Pin Y (A→Y Level Translation)

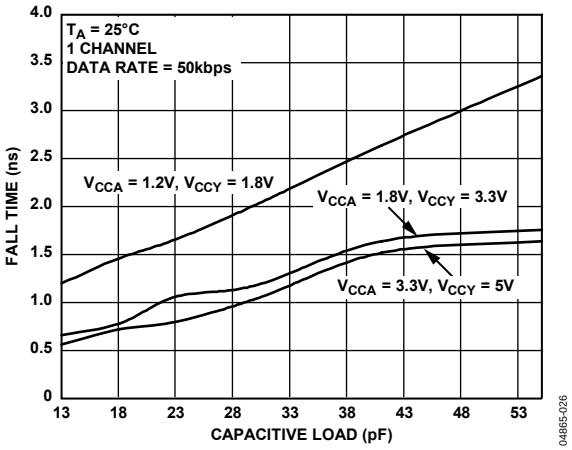


Figure 18. Fall Time vs. Capacitive Load at Pin A (Y→A Level Translation)

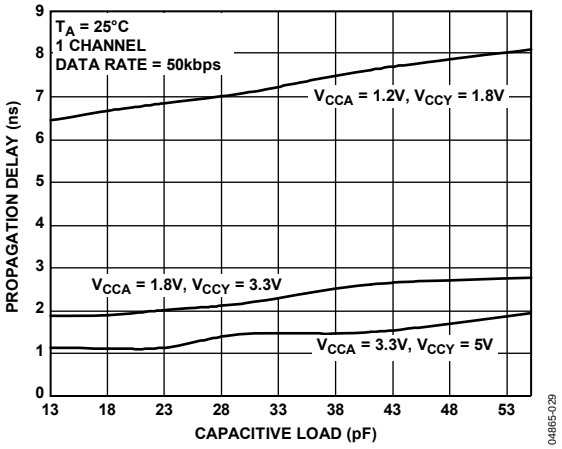


Figure 21. Propagation Delay (t_{PLH}) vs. Capacitive Load at Pin A (Y→A Level Translation)

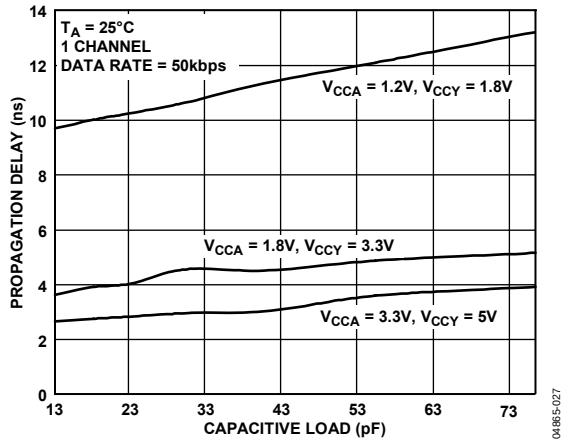


Figure 19. Propagation Delay (t_{PLH}) vs. Capacitive Load at Pin Y (A→Y Level Translation)

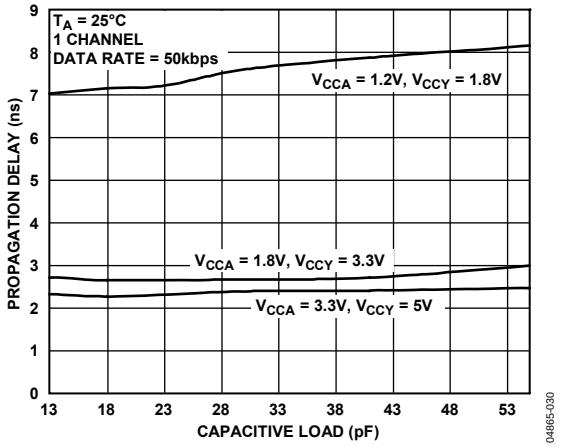


Figure 22. Propagation Delay (t_{PHL}) vs. Capacitive Load at Pin A (Y→A Level Translation)

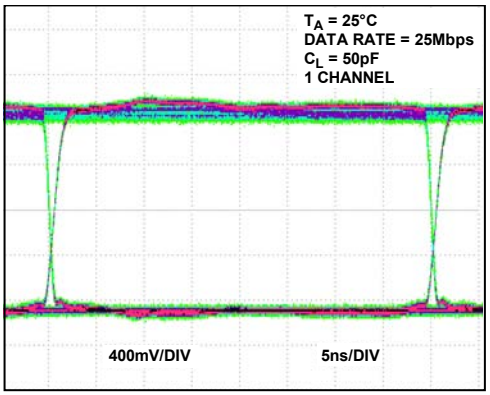


Figure 23. Eye Diagram at Y Output
(1.2 V→1.8 V Level Translation, 25 Mbps)

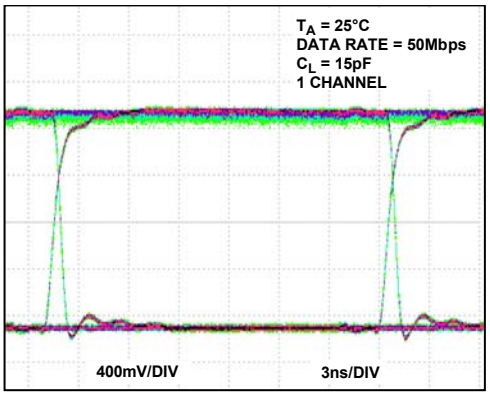


Figure 26. Eye Diagram at A Output
(3.3 V→1.8 V Level Translation, 50 Mbps)

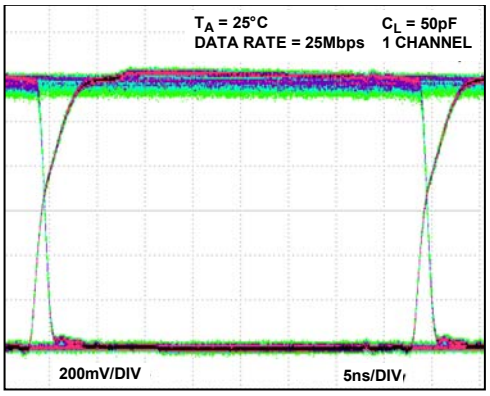


Figure 24. Eye Diagram at A Output
(1.8 V→1.2 V Level Translation, 25 Mbps)

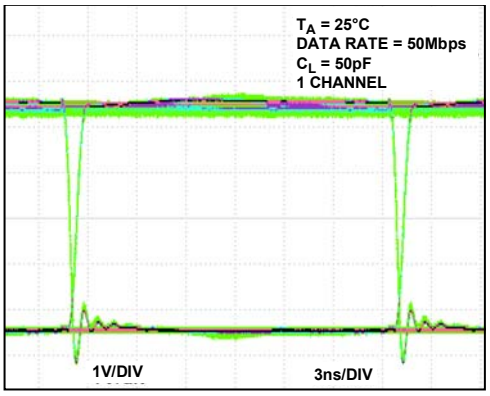


Figure 27. Eye Diagram at Y Output
(3.3 V→5 V Level Translation, 50 Mbps)

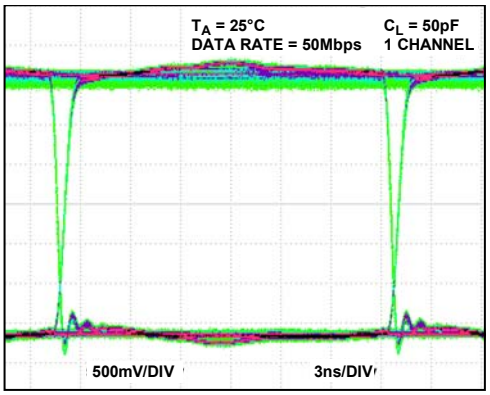


Figure 25. Eye Diagram at Y Output
(1.8 V→3.3 V Level Translation, 50 Mbps)

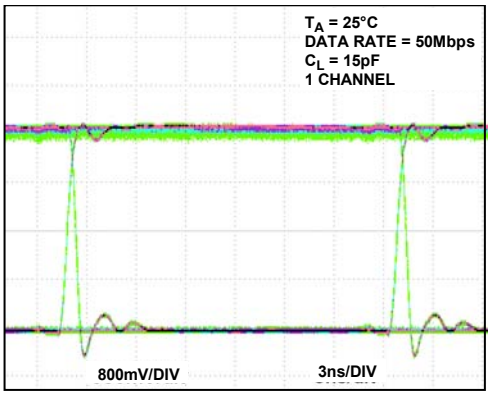


Figure 28. Eye Diagram at A Output
(5 V→3.3 V Level Translation, 50 Mbps)

TEST CIRCUITS

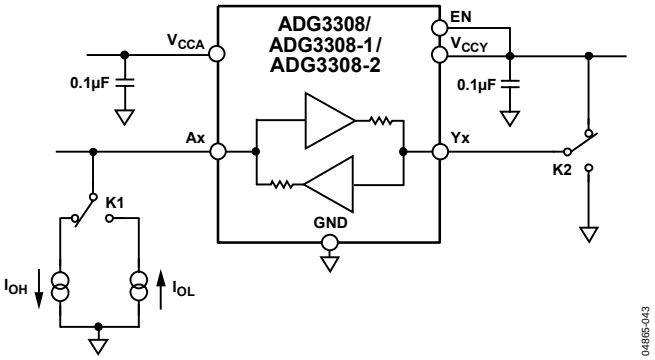


Figure 29. V_{OH}/V_{OL} Voltages at Pin A

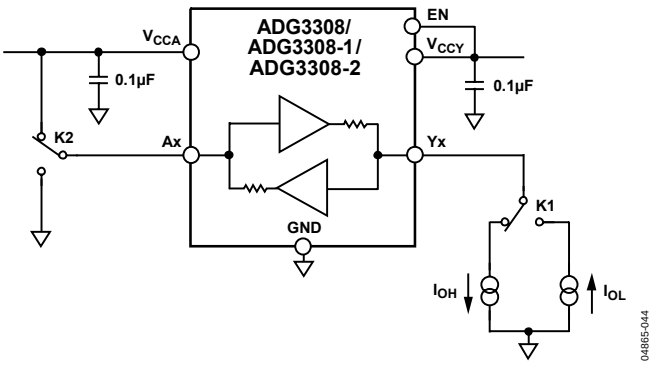


Figure 30. V_{OH}/V_{OL} Voltages at Pin Y

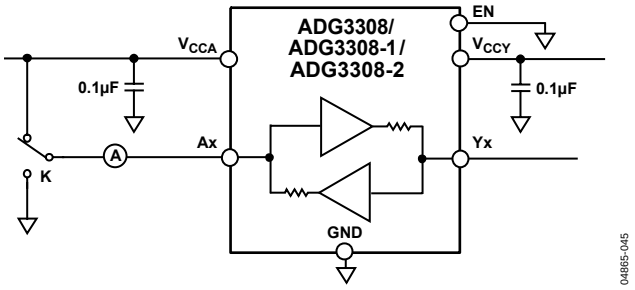


Figure 31. Three-State Leakage Current at Pin A

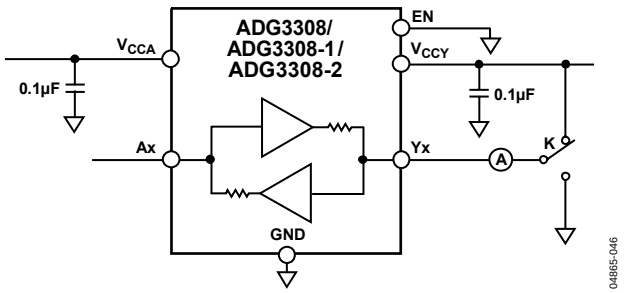


Figure 32. Three-State Leakage Current at Pin Y

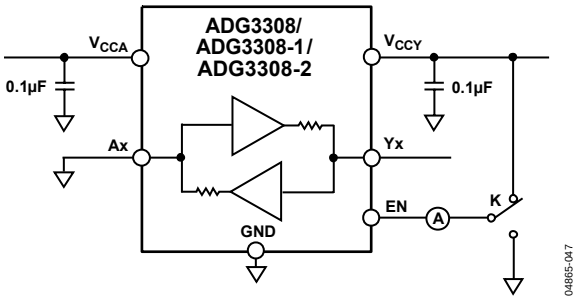


Figure 33. EN Pin Leakage Current

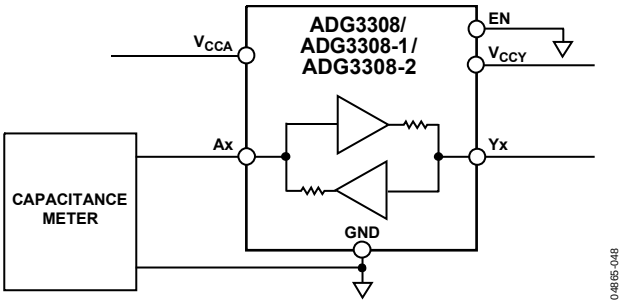


Figure 34. Capacitance at Pin A

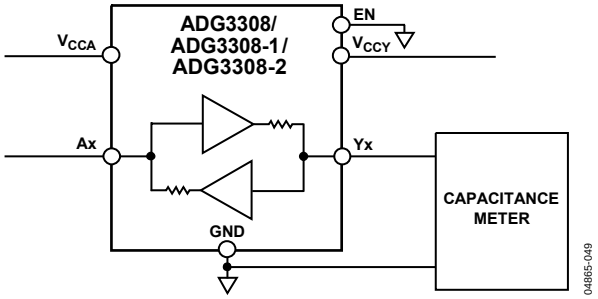


Figure 35. Capacitance at Pin Y

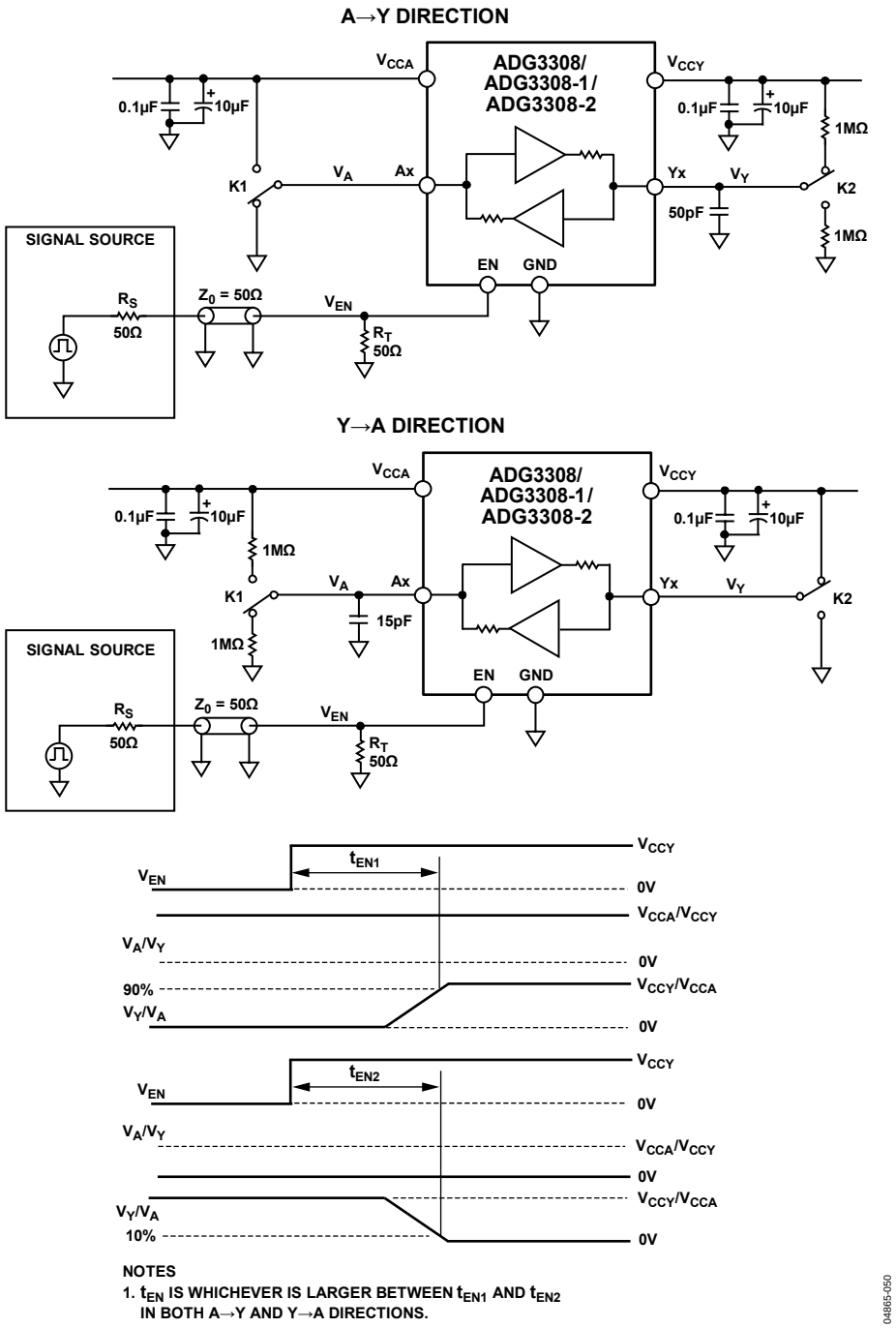


Figure 36. Enable Time

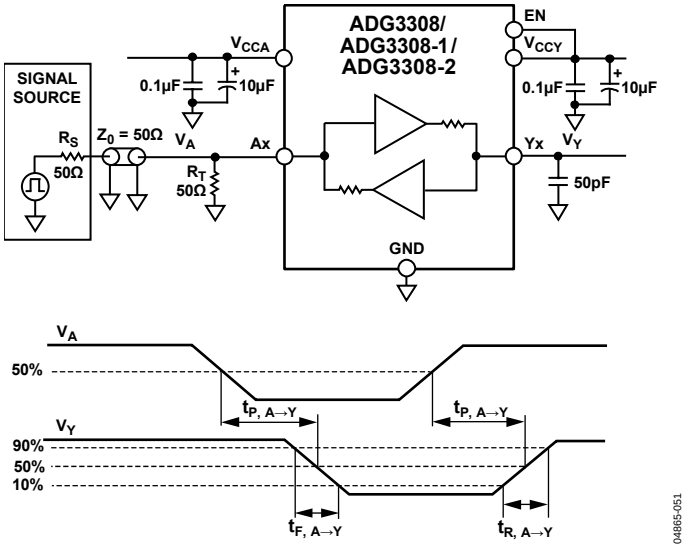


Figure 37. Switching Characteristics (A→Y Level Translation)

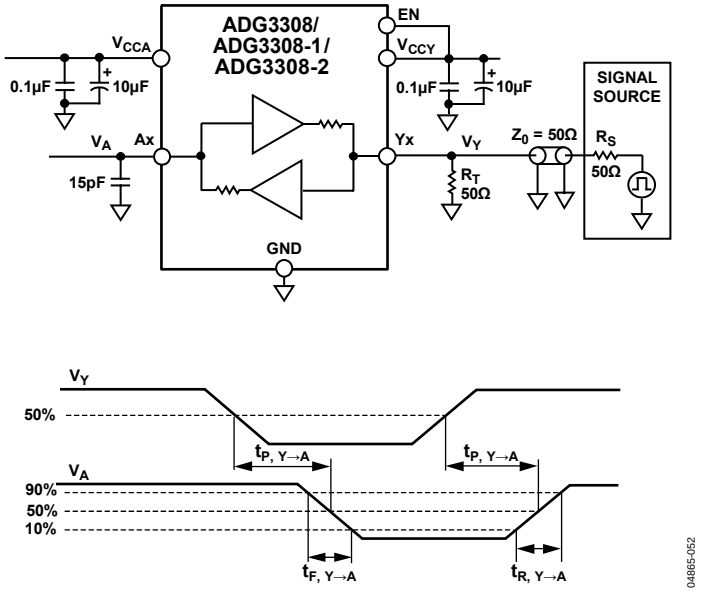


Figure 38. Switching Characteristics (Y→A Level Translation)

TERMINOLOGY

V_{IHA}
Logic input high voltage at Pin A1 to Pin A8.

V_{ILA}
Logic input low voltage at Pin A1 to Pin A8.

V_{OHA}
Logic output high voltage at Pin A1 to Pin A8.

V_{OLA}
Logic output low voltage at Pin A1 to Pin A8.

C_A
Capacitance measured at Pin A1 to Pin A8 (EN = 0).

$I_{LA, HIGH-Z}$
Leakage current at Pin A1 to Pin A8 when EN = 0 (high impedance state at Pin A1 to Pin A8).

V_{IHY}
Logic input high voltage at Pin Y1 to Pin Y8.

V_{ILY}
Logic input low voltage at Pin Y1 to Pin Y8.

V_{OHY}
Logic output high voltage at Pin Y1 to Pin Y8.

V_{OLY}
Logic output low voltage at Pin Y1 to Pin Y8.

C_Y
Capacitance measured at Pin Y1 to Pin Y8 (EN = 0).

$I_{LY, HIGH-Z}$
Leakage current at Pin Y1 to Pin Y8 when EN = 0 (high impedance state at Pin Y1 to Pin Y8).

V_{IHEN}
Logic input high voltage at the EN pin.

V_{ILEN}
Logic input low voltage at the EN pin.

C_{EN}
Capacitance measured at EN pin.

I_{LEN}
Enable (EN) pin leakage current.

t_{EN}
Three-state enable time for Pin A1 to Pin A8/Pin Y1 to Pin Y8.

$t_{P, A\rightarrow Y}$
Propagation delay when translating logic levels in the A→Y direction.

$t_{R, A\rightarrow Y}$
Rise time when translating logic levels in the A→Y direction.

$t_{F, A\rightarrow Y}$
Fall time when translating logic levels in the A→Y direction.

$D_{MAX, A\rightarrow Y}$
Guaranteed data rate when translating logic levels in the A→Y direction under the driving and loading conditions specified in Table 1.

$t_{SKEW, A\rightarrow Y}$
Difference between propagation delays on any two channels when translating logic levels in the A→Y direction.

$t_{PPSKEW, A\rightarrow Y}$
Difference in propagation delay between any one channel and the same channel on a different part (under same driving/loading conditions) when translating in the A→Y direction.

$t_{P, Y\rightarrow A}$
Propagation delay when translating logic levels in the Y→A direction.

$t_{R, Y\rightarrow A}$
Rise time when translating logic levels in the Y→A direction.

$t_{F, Y\rightarrow A}$
Fall time when translating logic levels in the Y→A direction.

$D_{MAX, Y\rightarrow A}$
Guaranteed data rate when translating logic levels in the Y→A direction under the driving and loading conditions specified in Table 1.

$t_{SKEW, Y\rightarrow A}$
Difference between propagation delays on any two channels when translating logic levels in the Y→A direction.

$t_{PPSKEW, Y\rightarrow A}$
Difference in propagation delay between any one channel and the same channel on a different part (under same driving/loading conditions) when translating in the Y→A direction.

V_{CCA}
V_{CCA} supply voltage.

V_{CCY}
V_{CCY} supply voltage.

I_{CCA}
V_{CCA} supply current.

I_{CCY}
V_{CCY} supply current.

$I_{HIGH-ZA}$
V_{CCA} supply current during three-state mode (EN = 0).

$I_{HIGH-ZY}$
V_{CCY} supply current during three-state mode (EN = 0).

THEORY OF OPERATION

The ADG3308/ADG3308-1/ADG3308-2 level translators allow the level shifting necessary for data transfer in a system where multiple supply voltages are used. The device requires two supplies, V_{CCA} and V_{CCY} ($V_{CCA} \leq V_{CCY}$). These supplies set the logic levels on each side of the device. When driving the A pins, the device translates the V_{CCA} compatible logic levels to V_{CCY} compatible logic levels available at the Y pins. Similarly, because the device is capable of bidirectional translation, when driving the Y pins the V_{CCY} compatible logic levels are translated to the V_{CCA} compatible logic levels available at the A pins. When EN = 0, the A1 pin to the A8 pin and the Y1 pin to the Y8 pin are three-stated. When EN is driven high, the ADG3308/ADG3308-1/ADG3308-2 go into normal operation mode and perform level translation.

LEVEL TRANSLATOR ARCHITECTURE

The ADG3308/ADG3308-1/ADG3308-2 consist of eight bidirectional channels. Each channel can translate logic levels in either the A→Y or the Y→A direction. They use a one-shot accelerator architecture, ensuring excellent switching characteristics. Figure 39 shows a simplified block diagram of a bidirectional channel.

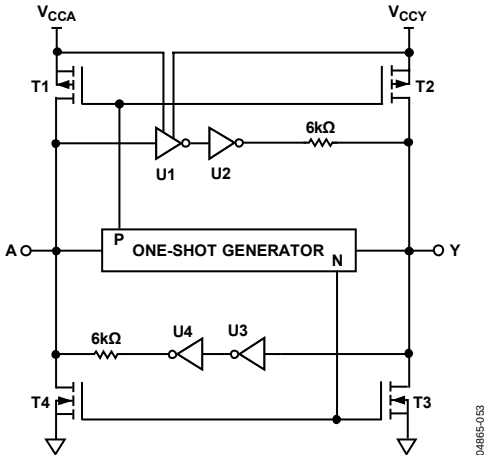


Figure 39. Simplified Block Diagram of an ADG3308/ADG3308-1/ADG3308-2 Channel

The logic level translation in the A→Y direction is performed using a level translator (U1) and an inverter (U2), whereas the translation in the Y→A direction is performed using the U3 inverter and U4 inverter. The one-shot generator detects a rising or falling edge present on either the A side or the Y side of the channel. It sends a short pulse that turns on the PMOS transistors (T1 and T2) for a rising edge, or the NMOS transistors (T3 and T4) for a falling edge. This charges/discharges the capacitive load faster, resulting in fast rise and fall times.

The inputs of the unused channels (A or Y) should be tied to their corresponding V_{CC} rail (V_{CCA} or V_{CCY}) or to GND.

INPUT DRIVING REQUIREMENTS

To ensure correct operation of the ADG3308/ADG3308-1/ADG3308-2, the circuit that drives the input of the device should be able to ensure rise/fall times of less than 3 ns when driving a load consisting of a 6 kΩ resistor in parallel with the input capacitance of the ADG3308/ADG3308-1/ADG3308-2 channel.

OUTPUT LOAD REQUIREMENTS

The ADG3308/ADG3308-1/ADG3308-2 level translators are designed to drive CMOS-compatible loads. If current-driving capability is required, it is recommended to use buffers between the ADG3308/ADG3308-1/ADG3308-2 outputs and the load.

ENABLE OPERATION

The ADG3308/ADG3308-1/ADG3308-2 provide three-state operation at the A I/O pins and the Y I/O pins by using the enable (EN) pin, as shown in Table 4.

Table 4. Truth Table

EN	Y I/O Pins	A I/O Pins
0	High-Z[1]	High-Z[1]
1	Normal operation[2]	Normal operation[2]

[1] High impedance state.
[2] In normal operation, the ADG3308/ADG3308-1/ADG3308-2 perform level translation.

When EN = 0, the ADG3308/ADG3308-1/ADG3308-2 enter into three-state mode. In this mode, the current consumption from both the V_{CCA} and V_{CCY} supplies is reduced, allowing the user to save power, which is critical, especially in battery-operated systems. The EN input pin can only be driven with V_{CCY} compatible logic levels for the ADG3308, whereas the ADG3308-1/ADG3308-2 can be driven with either V_{CCA}- or V_{CCY} compatible logic levels.

POWER SUPPLIES

For proper operation of the device, the voltage applied to the V_{CCA} must always be less than or equal to the voltage applied to V_{CCY}. To meet this condition, the recommended power-up sequence is V_{CCY} first and then V_{CCA}. The ADG3308/ADG3308-1/ADG3308-2 operate properly only after both supply voltages reach their nominal values. It is not recommended to use the part in a system where, during power-up, V_{CCA} may be greater than V_{CCY} due to a significant increase in the current taken from the V_{CCA} supply. For optimum performance, the V_{CCA} and V_{CCY} pins should be decoupled to GND as close as possible to the device.

DATA RATE

The maximum data rate at which the device is guaranteed to operate is a function of the V_{CCA} and V_{CCY} supply voltage combination and the load capacitance. It represents the maximum frequency of a square wave that can be applied to the I/O pins, ensuring that the device operates within the data sheet specifications in terms of output voltage (V_{OL} and V_{OH}) and power dissipation (the junction temperature does not exceed the value specified under the Absolute Maximum Ratings section). Table 5 shows the guaranteed data rates at which the ADG3308/ADG3308-1/ADG3308-2 can operate in both directions (A→Y level translation or Y→A level translation) for various V_{CCA} and V_{CCY} supply combinations.

Table 5. Guaranteed Data Rates[1]

	V_{CCY}			
V_{CCA}	**1.8 V (1.65 V to 1.95 V)**	**2.5 V (2.3 V to 2.7 V)**	**3.3 V (3.0 V to 3.6 V)**	**5 V (4.5 V to 5.5 V)**
1.2 V (1.15 V to 1.3 V)	25 Mbps	30 Mbps	40 Mbps	40 Mbps
1.8 V (1.65 V to 1.95 V)		45 Mbps	50 Mbps	50 Mbps
2.5 V (2.3 V to 2.7 V)			60 Mbps	50 Mbps
3.3 V (3.0 V to 3.6 V)				50 Mbps
5 V (4.5 V to 5.5 V)				

[1] The load capacitance used is 50 pF when translating in the A→Y direction and 15 pF when translating in the Y→A direction.

APPLICATIONS

The ADG3308/ADG3308-1/ADG3308-2 are designed for digital circuits that operate at different supply voltages; therefore, logic level translation is required. The lower voltage logic signals are connected to the A pins, and the higher voltage logic signals to the Y pins. The ADG3308/ADG3308-1/ADG3308-2 can provide level translation in both directions (A→Y or Y→A) on all eight channels, eliminating the need for a level translator IC for each direction. The internal architecture allows the ADG3308/ADG3308-1/ADG3308-2 to perform bidirectional level translation without an additional signal to set the direction in which the translation is made. It also allows simultaneous data flow in both directions on the same part, for example, when two channels translate in the A→Y direction while the other two translate in the Y→A direction. This simplifies the design by eliminating the timing requirements for the direction signal and reduces the number of ICs used for level translation.

Figure 40 shows an application where a 3.3 V microprocessor can read or write data to and from a 1.8 V peripheral device using an 8-bit bus.

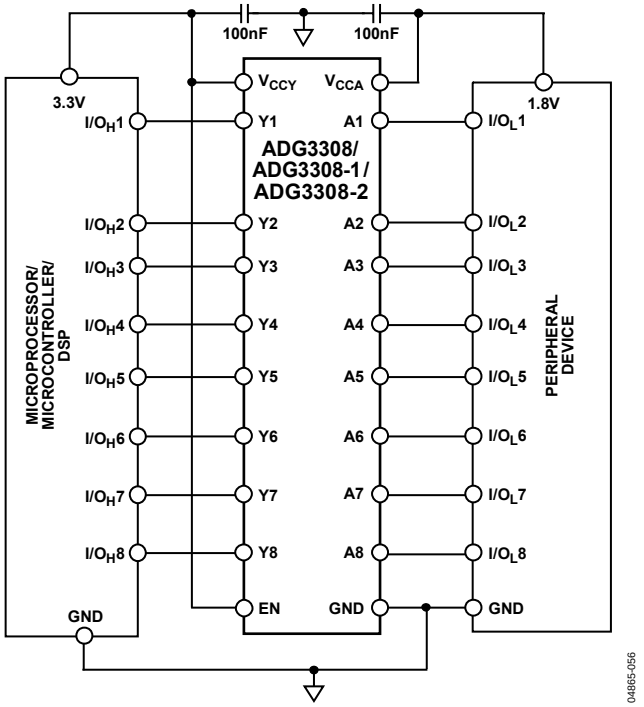


Figure 40. 1.8 V to 3.3 V 8-Bit Level Translation Circuit

When the application requires level translation between a microprocessor and multiple peripheral devices, the ADG3308/ADG3308-1/ADG3308-2 I/O pins can be three-stated by setting EN = 0. This feature allows the ADG3308/ADG3308-1/ADG3308-2 to share the data buses with other devices without causing contention issues. Figure 41 shows an application where a 3.3 V microprocessor is connected to 1.8 V peripheral devices using the three-state feature.

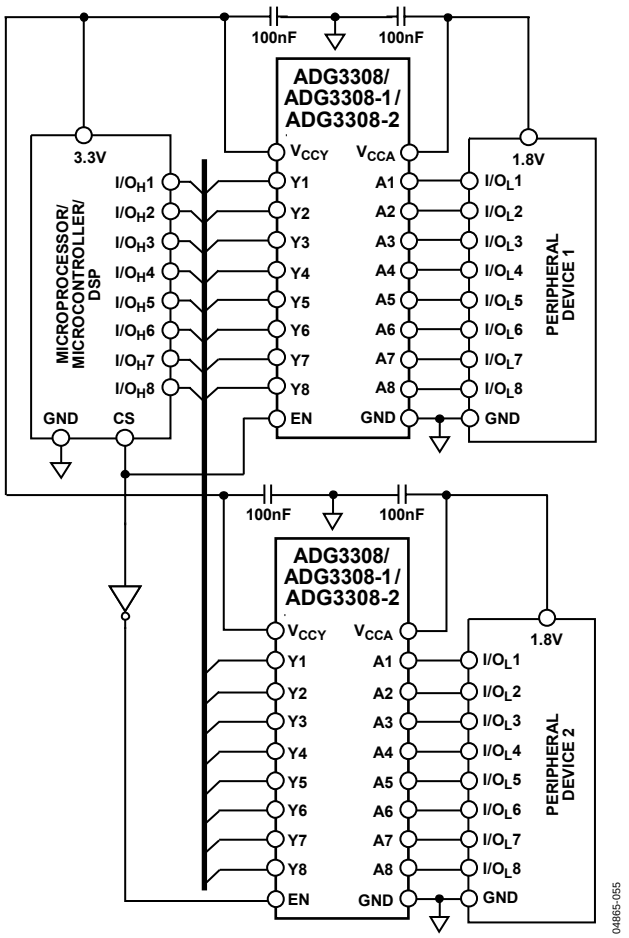
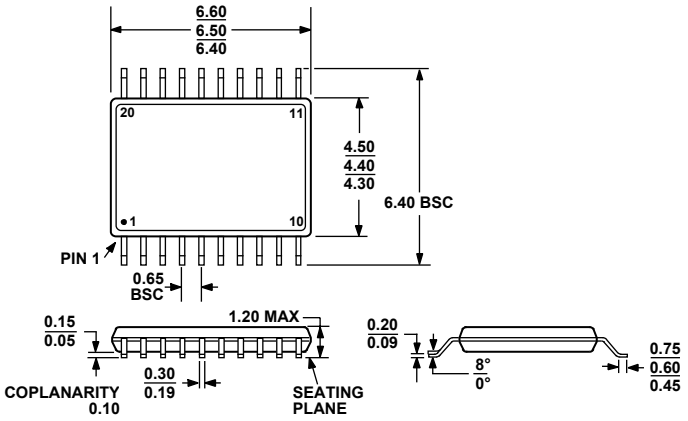


Figure 41. 1.8 V to 3.3 V Level Translation Circuit Using the Three-State Feature

LAYOUT GUIDELINES

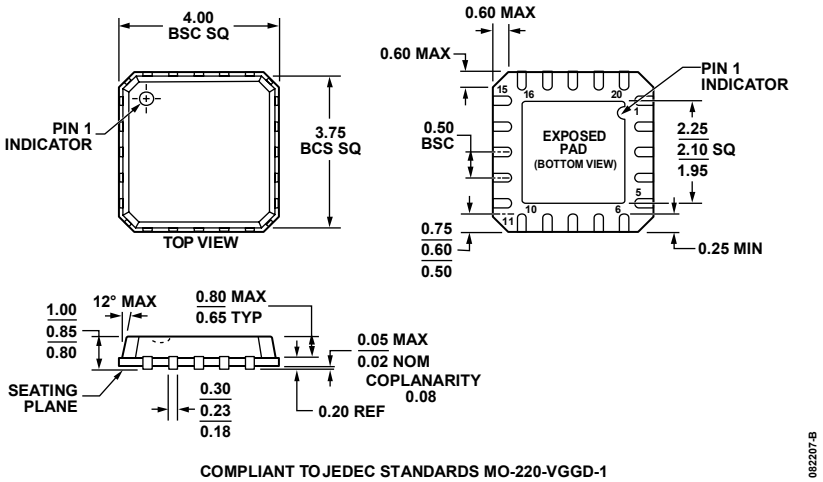
As with any high speed digital IC, the printed circuit board layout is important in the overall performance of the circuit. Care should be taken to ensure proper power supply bypass and return paths for the high speed signals. Each V_{CC} pin (V_{CCA} and V_{CCY}) should be bypassed using low effective series resistance (ESR) and effective series inductance (ESI) capacitors placed as close as possible to the V_{CCA} and V_{CCY} pins. The parasitic inductance of the high speed signal track can cause significant overshoot. This effect can be reduced by keeping the length of the tracks as short as possible. A solid copper plane for the return path (GND) is also recommended.

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-153-AC

Figure 42. 20-Lead Thin Shrink Small Outline Package [TSSOP]
(RU-20)
Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MO-220-VGGD-1

Figure 43. 20-Lead Lead Frame Chip Scale Package [LFCSP_VQ]
4 mm × 4 mm Body, Very Thin Quad
(CP-20-1)
Dimensions shown in millimeters

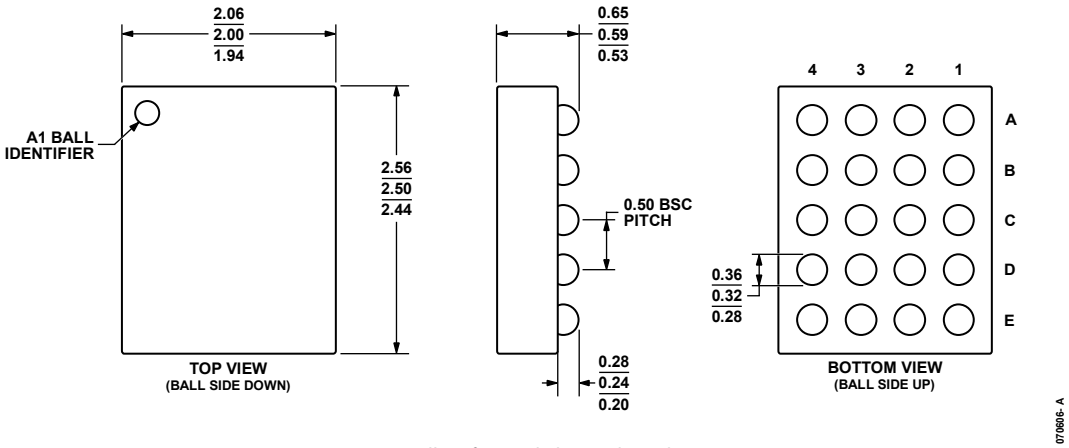


Figure 44. 20-Ball Wafer Level Chip Scale Package [WLCSP]
(CB-20-2)
Dimensions shown in millimeters

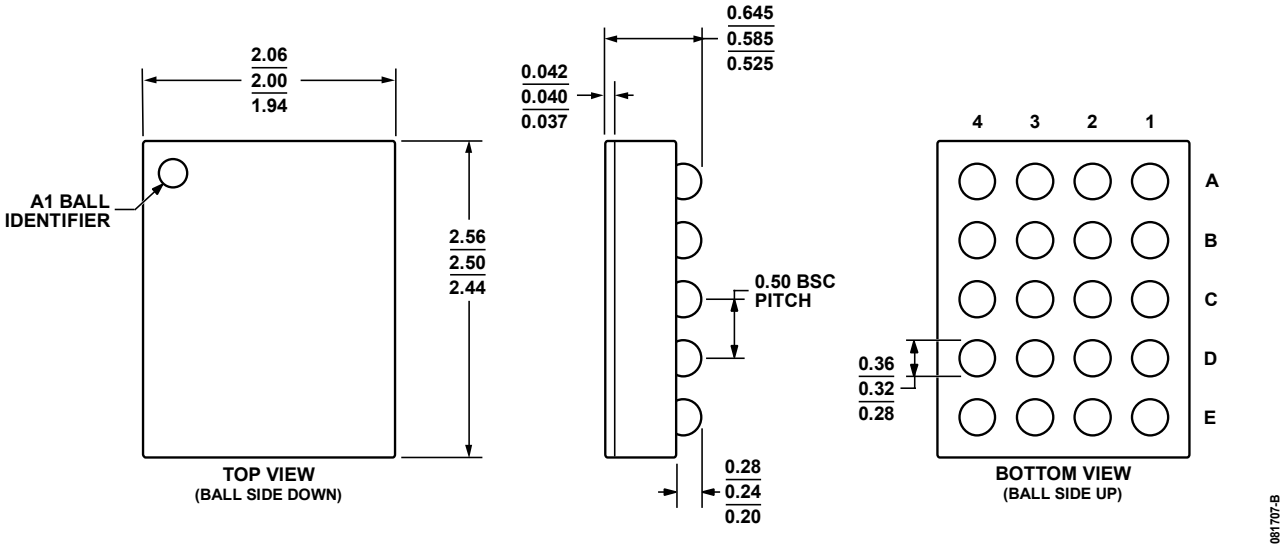


Figure 45. Backside-Coated 20-Ball Wafer Level Chip Scale Package [WLCSP]
(CB-20-3)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
ADG3308BRUZ[1]	−40°C to +85°C	20-Lead Thin Shrink Small Outline Package [TSSOP]	RU-20
ADG3308BRUZ-REEL[1]	−40°C to +85°C	20-Lead Thin Shrink Small Outline Package [TSSOP]	RU-20
ADG3308BRUZ-REEL7[1]	−40°C to +85°C	20-Lead Thin Shrink Small Outline Package [TSSOP]	RU-20
ADG3308BCPZ-REEL[1]	−40°C to +85°C	20-Lead Lead Frame Chip Scale Package [LFCSP_VQ]	CP-20-1
ADG3308BCPZ-REEL7[1]	−40°C to +85°C	20-Lead Lead Frame Chip Scale Package [LFCSP_VQ]	CP-20-1
ADG3308BCBZ-1-RL7[1]	−40°C to +85°C	20-Ball Wafer Level Chip Scale Package [WLCSP]	CB-20-2
ADG3308BCBZ-1-REEL[1]	−40°C to +85°C	20-Ball Wafer Level Chip Scale Package [WLCSP]	CB-20-2
ADG3308BCBZ-2-RL7[1]	−40°C to +85°C	Backside-Coated 20-Ball Wafer Level Chip Scale Package [WLCSP]	CB-20-3
ADG3308BCBZ-2-REEL[1]	−40°C to +85°C	Backside-Coated 20-Ball Wafer Level Chip Scale Package [WLCSP]	CB-20-3

[1] Z = RoHS Compliant Part.