

**ABSOLUTE MAXIMUM RATINGS**

Positive Supply, pin 12 .....	+ 16V dc
Negative Supply, pin 4 .....	- 16V dc
Logic Supply, pin 17 .....	+ 7V dc
Logic Inputs .....	+ 7V dc
Analog Inputs .....	± Twice selected analog input range

**FUNCTIONAL SPECIFICATIONS**

Typical at +25°C, ±15V dc and +5V dc supplies, unless otherwise noted.

**INPUTS**

Analogue Input Ranges unipolar <sup>1</sup> .....	0 to -5V, 0 to -10V, 0 to -20V
bipolar .....	± 2.5V, ± 5V, ± 10V
reference .....	-9.5V to -10.5V
Input Impedance <sup>2</sup> .....	312Ω
5V range .....	625Ω
10V range .....	1.25 kΩ
20V range .....	1 kΩ
bipolar Input .....	2 kΩ
reference (pin 5) .....	2 kΩ
Start Conversion .....	2V min. to 5.5V max. positive pulse with duration of 25 nsec. min. Rise and fall times typical 10 nsec. Logic "1" resets converter. Logic "0" initiates conversion. Loading: 1 TTL load.

**OUTPUTS**

Parallel Output Data .....	11 Parallel lines of data (10 binary bits + MSB) held until next conversion command. V <sub>OUT</sub> ("0") ≤ +0.4V. V <sub>OUT</sub> ("1") ≥ +2.4V. Loading: 2 TTL loads
Coding <sup>3</sup> , unipolar .....	Straight Binary
bipolar <sup>4</sup> .....	Offset Binary, Two's Complement
Serial Output Data .....	NRZ successive decision pulses out, MSB first, at internal clock frequency Loading: 4 TTL loads.
End of Conversion (EOC) .....	Conversion Status Signal. Output is logic high during reset and conversion, low when conversion is complete. Loading: 4 TTL loads.
Clock Output .....	Train of positive going, 0 to +5V, 30 nsec. pulses.
Clock Frequency ADC-816MC/MM .....	14.6 MHz
ADC-826MC/MM .....	8.1 MHz
Reference Output, Voltage .....	-10.00V ± 0.02V
Current .....	0 to +20 mA (sink only)
Impedance .....	100 max. f <sub>0</sub> ≤ 10 MHz

**PERFORMANCE**

Resolution .....	10 bits
Conversion Time <sup>5</sup> , ADC-816MC .....	800 nsec. max.
ADC-826MC/MM .....	1.4 μsec. max.
Nonlinearity .....	± 1/2 LSB max.
Differential Nonlinearity <sup>6</sup> .....	± 1/2 LSB max.
Gain Error <sup>7</sup> , before adjustment, unipolar .....	± 0.3% of FSR max. <sup>8</sup>
bipolar .....	± 0.2% of FSR max.
Zero Error, before adjustment, unipolar .....	± 0.2% of FSR max.
Offset Error, before adjustment, bipolar .....	± 0.1% of FSR max.
Gain Tempco <sup>9</sup> , unipolar .....	± 37 ppm/°C max.
bipolar .....	± 28 ppm/°C max.
Zero Tempco, unipolar .....	± 12 ppm/°C max.
bipolar .....	± 23 ppm/°C max.
Conversion Time Tempco .....	± 0.1%/°C
Reference Output Tempco .....	± 20 ppm/°C max.
Power Supply Rejection .....	± 0.008%/% supply
No missing codes .....	Over operating Temp. Range

**POWER REQUIREMENTS**

Analog Supply, pin 12 .....	+ 15V dc ± 1V dc at 106 mA max.
pin 4 .....	- 15V dc ± 1V dc at 60 mA max.
Reference Supply, pin 3 .....	- 15V dc ± 0.5V dc at 34 mA max.
Logic Supply, pin 17 .....	+ 5V dc ± 0.25V dc at 80 mA max.
Power Dissipation .....	1.7 watts typical, 2.9 watts max.

**PHYSICAL/ENVIRONMENTAL**

Operating Temp. Range Suffix C .....	0°C to +70°C
Suffix M .....	- 55°C to +125°C
Storage Temperature Range .....	- 65°C to +150°C
Package Type .....	32-pin hermetically sealed Ceramic DIP
Pins .....	0.010 x 0.018 inch gold plated Kovar
Weight .....	0.8 ounces (23 grams)

**FOOTNOTES:**

1. Bipolar input must be tied to ground.
2. Resistance tolerance is -30%, +50%, ± 50 ppm/°C.
3. All coding is inverted analog.
4. Two's Complement Binary available for parallel output only.
5. Maximum conversion time is specified at full rated operating temperature. The ADC-816MM has a maximum conversion time of 900 nanoseconds at full rated operating temperature. See Technical note 3 for 25°C conversion time.
6. Tested over full rated operating temperature range.
7. Includes Zero Error.
8. FSR is Full-Scale Range.
9. Includes internal reference Tempco. Given as a maximum for 5V FSR, these values improve by 10% for 10V FSR, and by 20% for 20V FSR.

**TECHNICAL NOTES**

1. Use of good high frequency circuit board layout techniques is required for rated performance. The power common (pin 1), comparator common (pin 7), and signal common (pin 6) are not connected internally, and therefore must be connected externally as directly as possible, through a low resistance, low inductance path. The extensive use of a ground plane for all common connections is highly recommended. Also, it is recommended that the analog and digital supplies, although they are internally bypassed with 0.033 μF capacitors, be additionally bypassed externally at the supply pins with 1 μF electrolytic capacitors.
2. The digital outputs are not buffered from their internal application and so are sensitive to unusual loading or long lines. Terminate these outputs with normal TTL inputs not more than 3 inches from the data output pin. Analog inputs must be non-reactive such that leads should be short and purely resistive. The reactive component of any analog input source, as seen at the analog input pin, should be less than 0.3% of the analog input resistance at that pin, for frequencies below 20 MHz.
3. Conversion time is measured from the rising edge of a 40 nanosecond start input pulse to the falling edge of the EOC output. The conversion time is factory set at +25°C for the ADC-816MC/MM at 750 nanoseconds and 1.25 microseconds for the ADC-826MC/MM. The worst case conversion time at the maximum rated operating temperature is given as a maximum specification.
4. To use the internal reference, the reference supply pin (pin 3) must be connected to the -15V supply. If the reference supply pin (pin 3) is disconnected or grounded, the internal reference will be disabled at a power saving of approximately 200 mW.

5. Serial output data is available in NRZ format successive decision pulses, MSB first, in straight binary or offset binary coding. Synchronization of the serial output data is achieved through the use of the clock output (pin 30). This same clock output also controls the output register such that at the rising edge of the output clock the previous data bit may be clocked out. However, there will be no clock edge to clock out the LSB. A Serial DATA Recovery circuit is diagrammed on the applications page that will correct this.
6. These converters have a case-to-ambient thermal resistance of  $22^{\circ}\text{C}$  per watt. At temperatures above  $+70^{\circ}\text{C}$ , an air flow of at least 400 linear feet per minute is recommended. To

operate at elevated temperatures it is recommended that the converter be mounted directly to the circuit board (without the use of a mounting socket) and that good thermal contact be established between the case bottom and the circuit board ground plane by use of a silicone thermal joint compound such as Wakefield Type 120 or equivalent.

7. Applications of these converters that require the use of a sample-hold may be satisfied by DATEL's model SHM-HU, an ultra-fast hybrid unit featuring 25 nanoseconds acquisition time and a  $\pm 2.5\text{V}$  input range.

## APPLICATIONS

### CALIBRATION PROCEDURE

1. Connect the converter as shown in the applicable connections diagram. A trigger pulse of between 40 nanoseconds and 100 nanoseconds is applied to the start conversion input (pin 31) at the rate of 200 kHz.

#### 2. Zero and Offset Adjustments

Apply a precision voltage reference source between the appropriate input for the selected full scale range and ground. Adjust the output of the reference source to the value shown in the Calibration Table for the unipolar zero adjustment ( $0 - \frac{1}{2}$  LSB) or the bipolar offset adjustment ( $\pm FS - \frac{1}{2}$  LSB). Adjust the appropriate timing potentiometer so that the output code flickers equally between X0000 00000 and X0000 00001. The MSB indicated by X will be 0 for straight binary and offset binary coding or 1 for two's complement output coding.

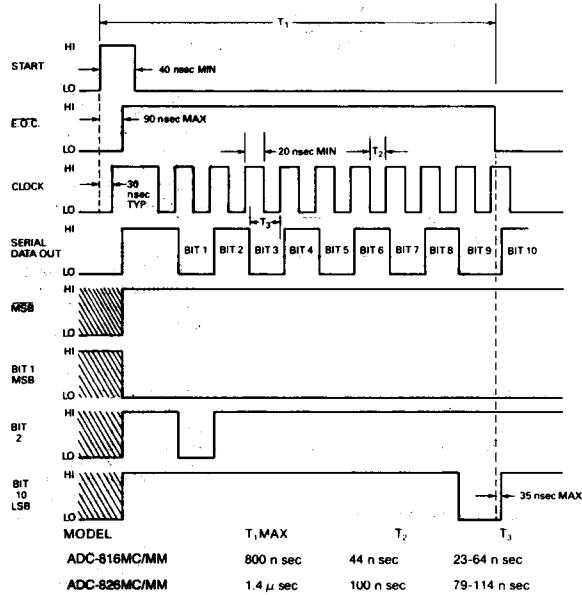
#### 3. Full Scale Adjustment

Set the output of the voltage reference source used in step 2 to the value shown in the Calibration Table for the unipolar or bipolar gain adjustment ( $-FS + \frac{1}{2}$  LSB). Adjust the gain trimming potentiometer so that the output code flickers equally between X1111 11111 and X1111 11110. The MSB indicated by X, will be 1 for straight binary and offset binary coding or coding or 0 for two's complement output coding.

UNIPOLAR RANGE	ADJUST.	INPUT VOLTAGE
0 To $-5\text{V}$	Zero Gain	$-2.4\text{ mV}$ $-4.9927\text{V}$
0 To $-10\text{V}$	Zero Gain	$-4.9\text{ mV}$ $-9.9854\text{V}$
0 To $-20\text{V}$	Zero Gain	$-9.8\text{ mV}$ $-19.9707\text{V}$

BIPOLAR RANGE	ADJUST.	INPUT VOLTAGE
$\pm 2.5\text{V}$	Offset Gain	$\pm 2.4975\text{V}$ $-2.4927\text{V}$
$\pm 5\text{V}$	Offset Gain	$\pm 4.9951\text{V}$ $-4.9854\text{V}$
$\pm 10\text{V}$	Offset Gain	$\pm 9.9902\text{V}$ $-9.9707\text{V}$

TIMING DIAGRAM FOR ADC-816, ADC-826



### CODING TABLES

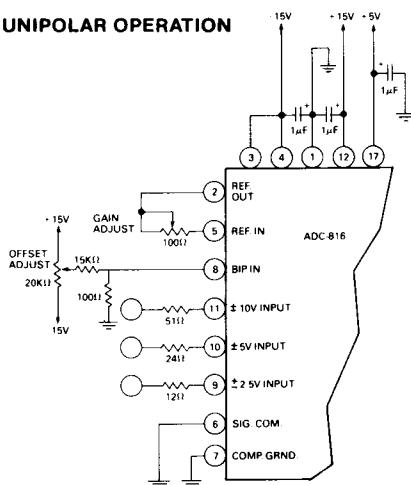
#### UNIPOLAR OPERATION

INPUT RANGE		STRAIGHT BINARY	
0 to $-20\text{V}$	0 to $-10\text{V}$	0 to $-5\text{V}$	MSB      LSB
-19.9805	-9.9902V	-4.9951	1111 11 1111
-17.5000	-8.7500	-4.3750	1110 00 0000
-15.0000	-7.5000	-3.7500	1100 00 0000
-10.0000	-5.0000	-2.5000	1000 00 0000
-5.0000	-2.5000	-1.2500	0100 00 0000
-2.5000	-1.2500	-0.6250	0010 00 0000
-0.0198	-0.0098	-0.0049	0000 00 0001
0.0000	0.0000	0.0000	0000 00 0000

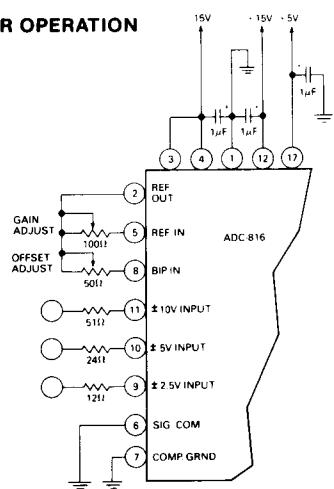
#### BINARY OPERATION

INPUT RANGE		OFFSET BINARY		TWO'S COMPLEMENT		
$\pm 10\text{V}$	$\pm 5\text{V}$	$\pm 2.5\text{V}$	MSB	LSB	MSB	LSB
-9.9805	-4.9902	-2.4951	1111 11 1111	0111 11 1111	0111 11 1111	0111 11 1111
-7.5000	-3.7500	-1.8750	1110 00 0000	0110 00 0000	0110 00 0000	0110 00 0000
-5.0000	-2.5000	-1.2500	1100 00 0000	0100 00 0000	0100 00 0000	0100 00 0000
0.0000	0.0000	0.0000	1000 00 0000	0000 00 0000	0000 00 0000	0000 00 0000
+5.0000	+2.5000	+1.2500	0100 00 0000	1000 00 0000	1100 00 0000	1100 00 0000
+7.5000	+3.7500	+1.8750	0110 00 0000	0010 00 0000	1010 00 0000	1010 00 0000
+9.9805	+4.9902	+2.4951	0000 00 0001	1000 00 0001	1000 00 0001	1000 00 0001
+10.0000	+5.0000	+2.5000	0000 00 0000	0000 00 0000	1000 00 0000	1000 00 0000

## UNIPOLAR OPERATION

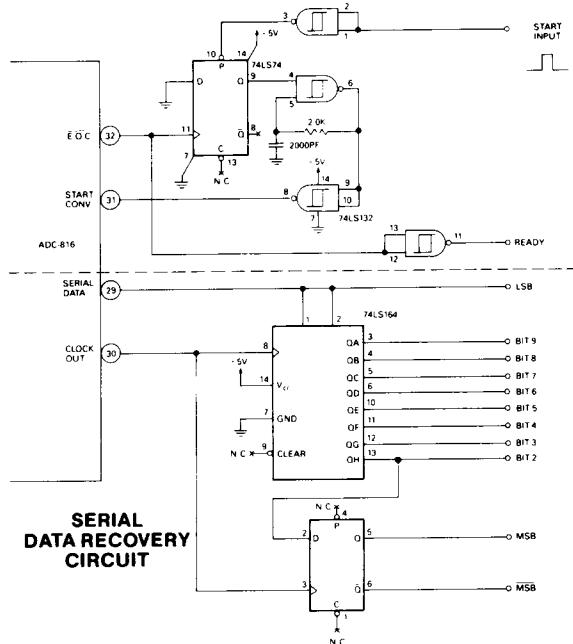


## BIPOLAR OPERATION



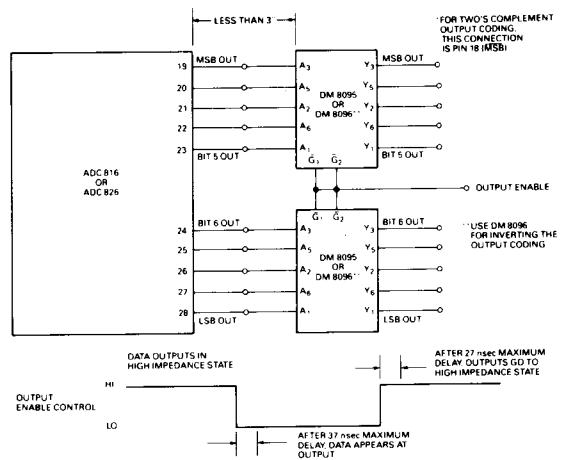
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## UNCONDITIONAL/START CIRCUIT



## SERIAL DATA RECOVERY CIRCUIT

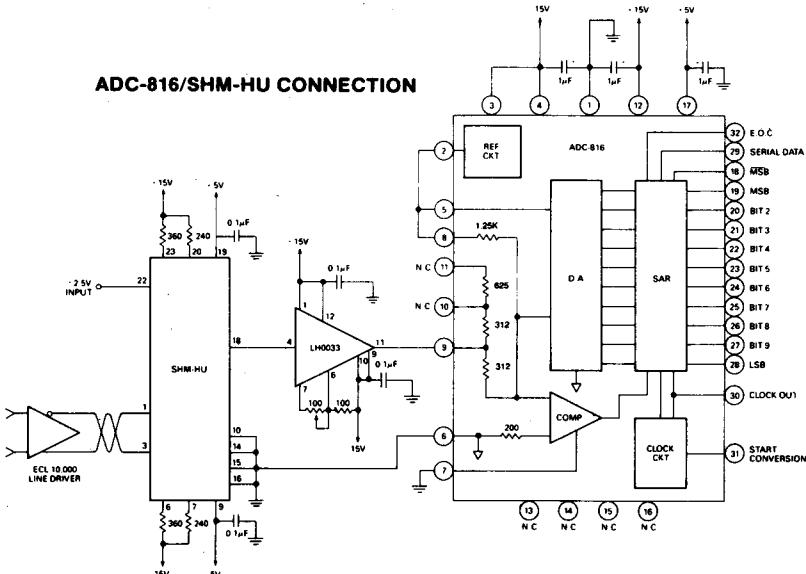
## HIGH SPEED THREE-STATE OUTPUT BUFFER GROUND PLANE LAYOUT



The Unconditional Start Circuit, shown for the ADC-816/826 insures the initiation of a conversion cycle upon the application of one start pulse of 40 nanoseconds minimum pulse width regardless of converter status.

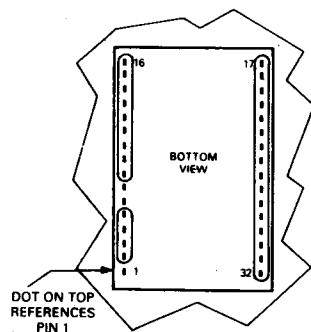
The serial data output of the ADC-816/826 is converted into parallel form, with the addition of an MSB output, by the Serial Data Recovery circuit. Users should refer to technical note No. 2 on the loading of the ADC-816/826 digital outputs when using these circuits.

## ADC-816/SHM-HU CONNECTION



When the ADC-816 or ADC-826 is configured as shown here with DATEL's SHM-HU hybrid sample-hold, a  $\pm 2.5\text{V}$  input step can be acquired to 0.1% accuracy in 30 nanoseconds and held to within 40  $\mu\text{V}$  while the A/D conversion takes place. Use of the SHM-HU reduces the time over which the input signal is averaged to a few nanoseconds (an A/D converter without a sample-hold averages the analog input signal over the total conversion time of the A/D).

## GROUND PLANE LAYOUT



## ORDERING INFORMATION

## MODEL NO.

ADC-816MC  
ADC-816MM

## OPERATING TEMP. RANGE

0°C To +70°C  
-55°C To +125°C

ADC-826MC  
ADC-826MM

-0°C To +70°C  
-55°C To +125°C

ACCESSORIES  
Part Number

DILS-2  
TP20K, TP100,  
TP50

Description  
Mating Socket (2 per converter)  
Trimming Potentiometers

For military devices compliant to MIL-STD-883, consult DATEL.