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REVISION HISTORY

7/10—Rev. 0 to Rev. A

Deleted Figure 15 7
Changes to Setting Active Load Current with Pin 6 ISF Section and Setting Bandwidth with Pin 4 (IDRV) Section 10

6/10—Revision 0: Initial Version

SPECIFICATIONS

BUFFER ELECTRICAL CHARACTERISTICS

T_A = 25°C, V_{CC} = 15 V, V_{EE} = 0 V, R_{IDRV} = 249 kΩ connected to V_{IDRV}, R_{LOAD} = 1 kΩ in parallel with 22 pF in series with 10 Ω, V_{IN} = 7.5 V, unless otherwise noted (see Figure 2 for a test circuit).

Table 1.

Parameter	Condition	Min	Typ	Max	Unit
GAIN					
Voltage Gain	V_{IN} = 6.5 V to 8.5 V, R_{ISF} = 0 Ω	0.995	0.998	1.005	V/V
INPUT/OUTPUT CHARACTERISTICS					
I/O Offset Voltage			30	41	mV
IDRV Current	R_{IDRV} = 249 kΩ, V_{IDRV} = 15 V		52	59	µA
Input/Output Voltage Range		V_{EE} + 1.4		V_{CC} − 1.4	V
Input Bias Current (I_{BUFF})			1		µA
DYNAMIC PERFORMANCE					
−3 dB Bandwidth	R_{IDRV} = 300 kΩ (I_{CC} = 1.1 mA), V_{OUT} = 0.1 V p-p		182		MHz
	R_{IDRV} = 150 kΩ (I_{CC} = 2.1 mA), V_{OUT} = 0.1 V p-p		288		MHz
	R_{IDRV} = 50 kΩ (I_{CC} = 4.7 mA), V_{OUT} = 0.1 V p-p		400		MHz
Slew Rate	V_{OUT} = 2 V step		415		V/µs
Rise Time	V_{IN} = 7.5 V to 8.5 V, 10% to 90%		2.2		ns
Fall Time	V_{IN} = 8.5 V to 7.5 V, 10% to 90%		1.8		ns
1% Settling Time	V_{IN} = 9.5 V to 7.5 V (falling edge)		5		ns
	V_{IN} = 7.5 V to 9.5 V (rising edge)		4.5		ns
	V_{IN} = 8.5 V to 7.5 V (falling edge)		4.5		ns
	V_{IN} = 7.5 V to 8.5 V (rising edge)		4		ns
I/O Delay Time	V_{IN} = 8.5 V to 7.5 V (falling edge)		0.4		ns
	V_{IN} = 7.5 V to 8.5 V (rising edge)		0.35		ns
Output Voltage Noise	@ 20 MHz		1.5		nV/√Hz
POWER SUPPLY					
Supply Voltage Range		4	15	17	V
Supply Current (I_{CC})			1.4	1.8	mA
OPERATING TEMPERATURE RANGE		−40		+85	°C

ACTIVE CURRENT LOAD ELECTRICAL CHARACTERISTICS

T_A = 25°C, V_{EE} = 0 V, V_{ISF} = 3 V, R_{ISF} = 10 kΩ connected to V_{ISF}, V_{IN} = 7.5 V, unless otherwise noted (see Figure 2 for a test circuit).

Table 2.

Parameter	Condition	Min	Typ	Max	Unit
INPUT/OUTPUT CHARACTERISTICS					
Active Load Current (I_{AL})	V_{ISF} = 0 V		1		µA
	V_{ISF} = 3 V		3		mA
	V_{ISF} = 7.5 V		12.7		mA
ISF Current (I_{ISF})	R_{ISF} = 10 kΩ		111	120	µA
Input Voltage Range		V_{EE} + 1.7		V_{CC}	V
OPERATING TEMPERATURE RANGE		−40		+85	°C

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 2.

Parameter	Rating
Supply Voltage	18 V
Input Voltage	V_{EE} to V_{CC}
ISF Pin	V_{EE} to V_{CC}
IDRV Pin	V_{EE} to V_{CC}
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	−40°C to +85°C
Junction Temperature Range	−65°C to +150°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 3. Thermal Resistance

Package Type	θ_{JA}	Unit
6-Lead LFCSP	160	°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

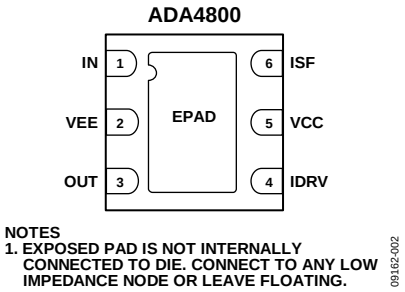

Figure 3. Pin Configuration

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	IN	Input. Connect this pin to the CCD sensor output.
2	VEE	Negative Power Supply Voltage.
3	OUT	Output. Connect this pin to the AFE input.
4	IDRV	Bandwidth Adjustment Pin. Connect this pin to VCC or an external voltage with an external resistor. This pin allows bandwidth to be controlled by adjusting I_{CC}. This pin can also be used to power down the buffer.
5	VCC	Positive Power Supply Voltage.
6	ISF	Active Load Current Adjustment Pin. Connect to VCC or an external voltage with an external resistor. This pin can also be connected to the microcontroller logic output through an external resistor for power save mode. This pin can also be used to power down the active current load.
EPAD	EPAD	Exposed Pad. Not internally connected to die. Connect to any low impedance node or leave floating.

TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, V_{CC} = 7.5 V, V_{EE} = −7.5 V, R_{IDRV} = 249 kΩ connected to V_{IDRV}, V_{ISF} = −4.5 V, R_{ISF} = 10 kΩ connected to V_{ISF}, V_{IN} shunt terminated with 49.9 Ω to 0 V, R_{LOAD} = 1 kΩ in parallel with 22 pF in series with 10 Ω to 0 V.

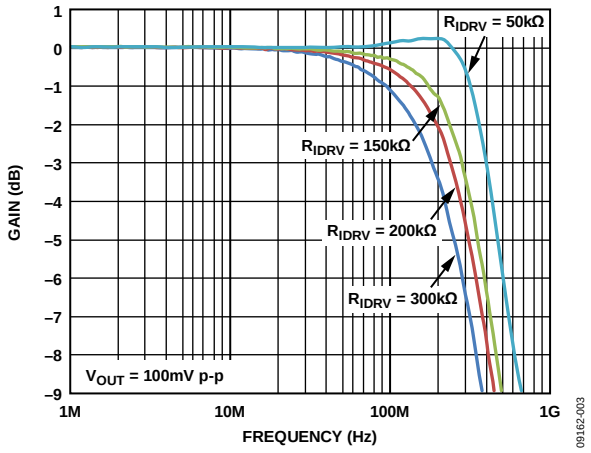

Figure 4. Small Signal Frequency Response with Various IDRV Resistances

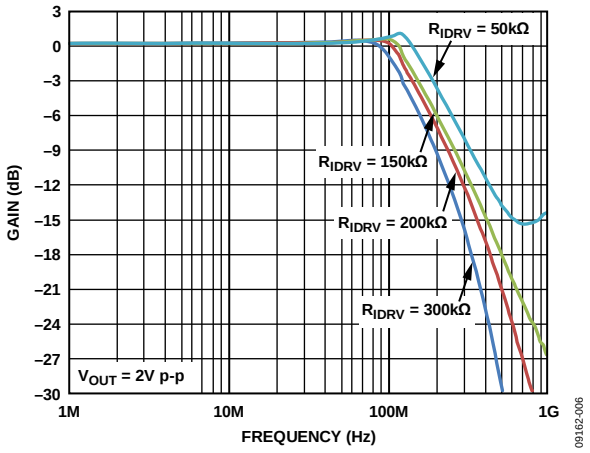

Figure 7. Large Signal Frequency Response with Various IDRV Resistances

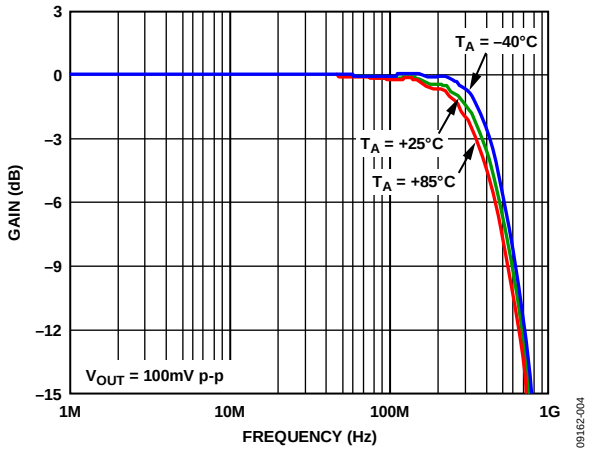

Figure 5. Small Signal Frequency Response at Various Temperatures

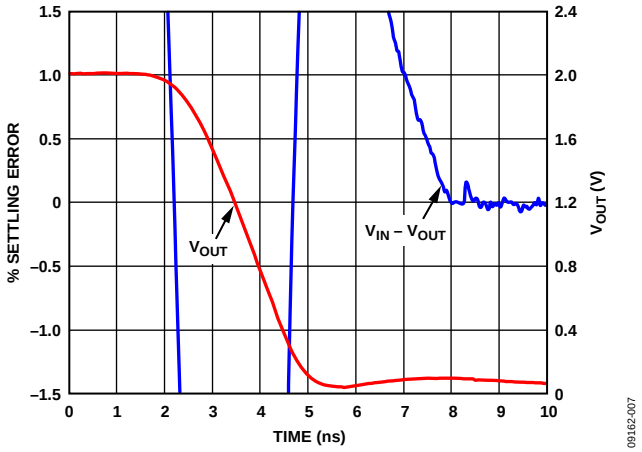

Figure 8. Settling Time, 2 V to 0 V Output Transition

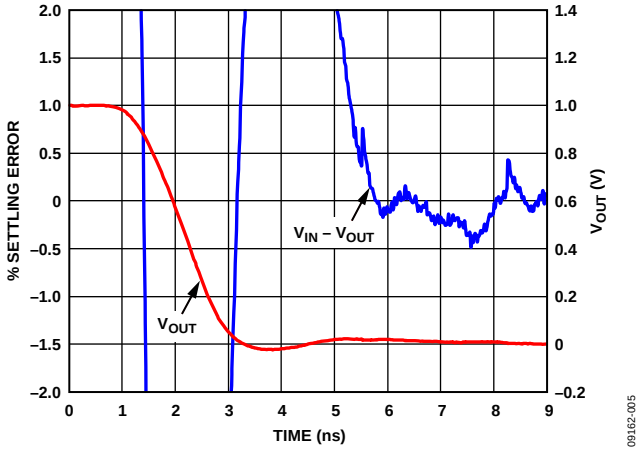

Figure 6. Settling Time, 1 V to 0 V Output Transition

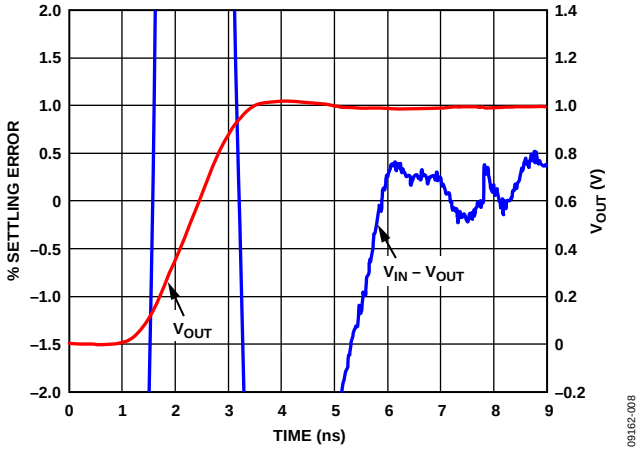

Figure 9. Settling Time, 0 V to 1 V Output Transition

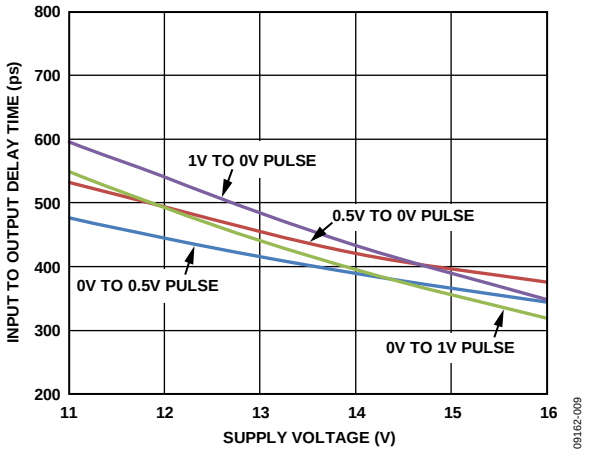

Figure 10. Input to Output Delay Time vs. Supply Voltage

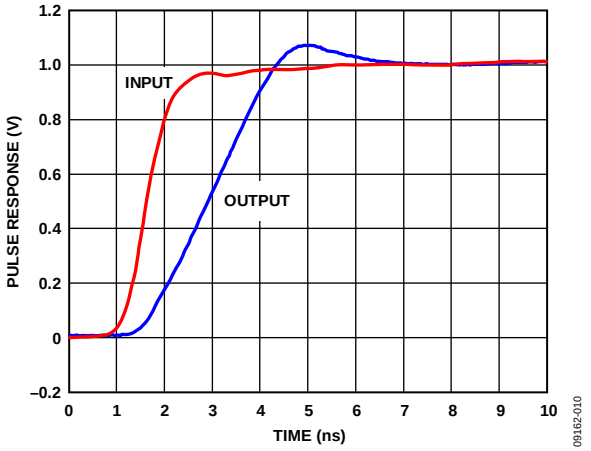

Figure 11. Positive Pulse Response, 0 V to 1 V

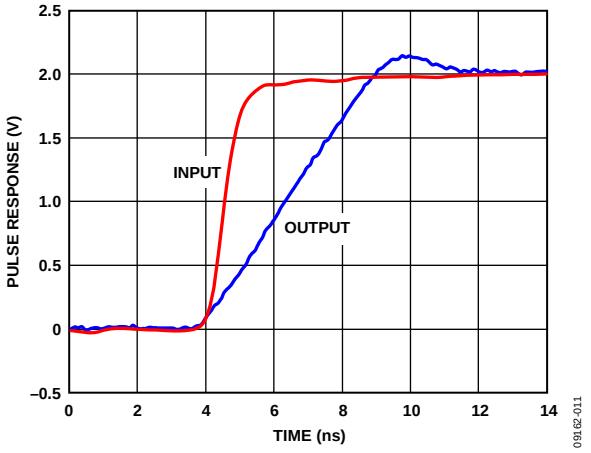

Figure 12. Positive Pulse Response, 0 V to 2 V

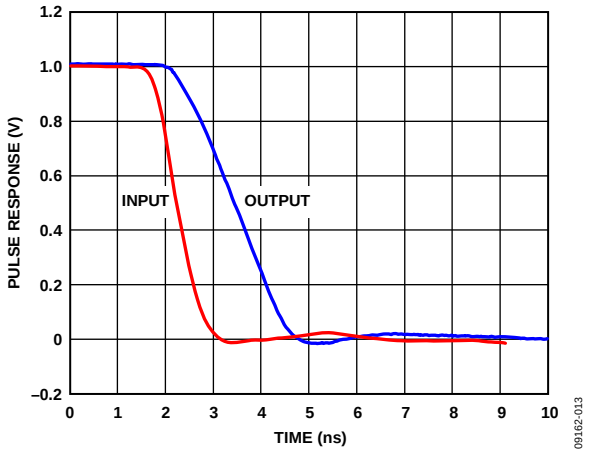

Figure 13. Negative Pulse Response, 1 V to 0 V

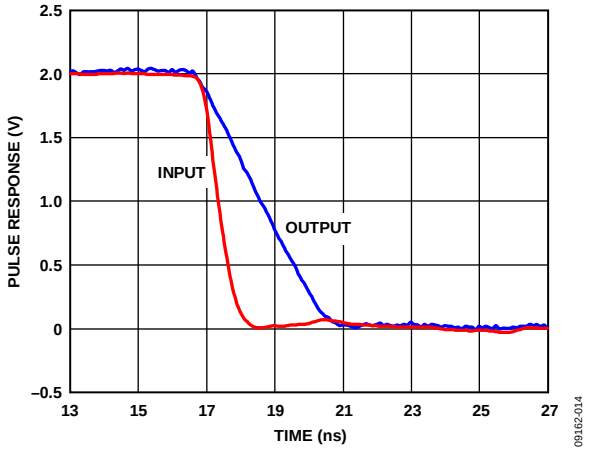

Figure 14. Negative Pulse Response, 2 V to 0 V

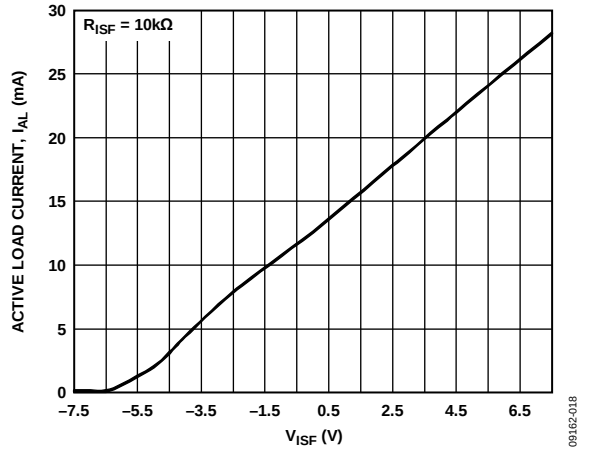

Figure 15. Input Current vs. Voltage on ISF Pin (V_{ISF})

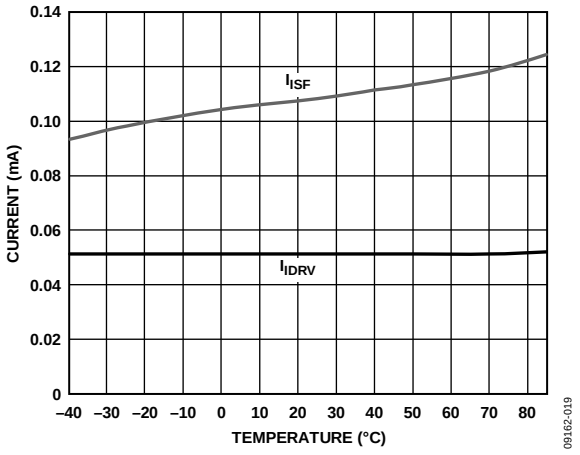

Figure 16. ISF and IDRV Currents vs. Temperature

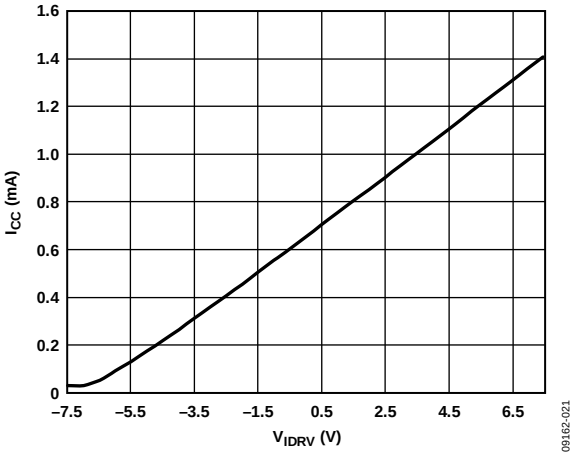

Figure 18. I_{CC} vs. Voltage on IDRV Pin (V_{IDRV})

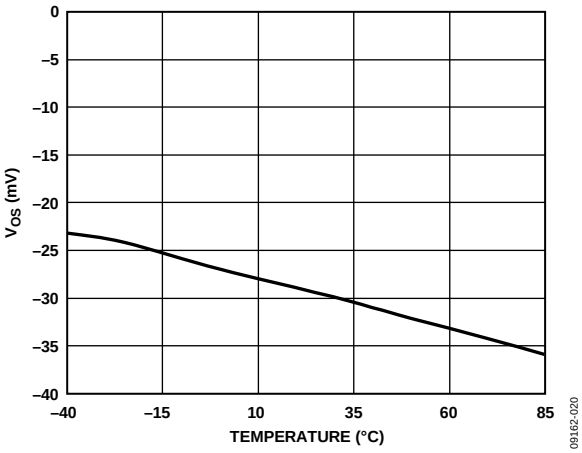

Figure 17. V_{OS} vs. Temperature

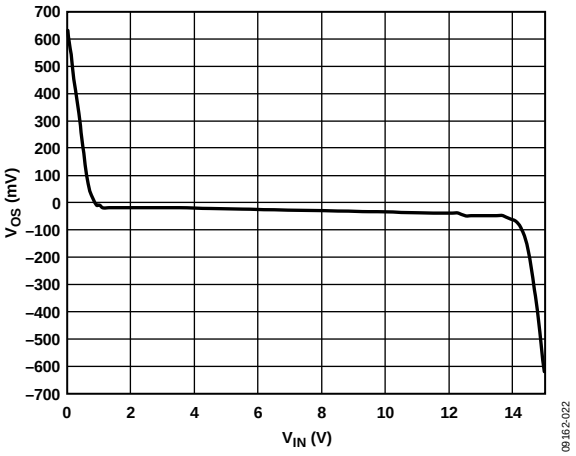

Figure 19. Output Offset Voltage vs. Input Voltage

TEST CIRCUIT

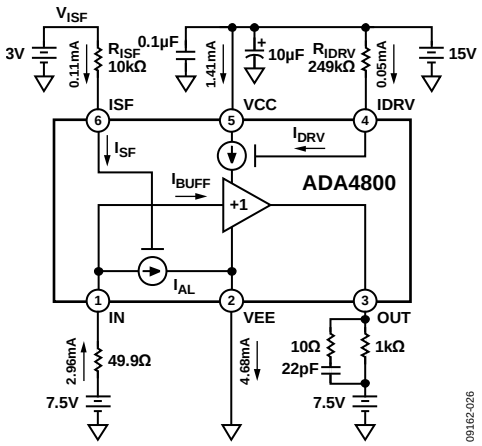

Figure 20. Typical Current Flow

THEORY OF OPERATION

The ADA4800 is a buffer integrated with an active load. Each element (the active load and the buffer) operates independently, as described in the following sections.

SETTING ACTIVE LOAD CURRENT WITH PIN 6 (ISF)

The ISF pin is used to establish the value of the active current load (I_{AL}). Set the ISF current using Equation 1.

$$I_{ISF} = \frac{V_{ISF} - 1.55\ \text{V}}{R_{ISF} + 3\ \text{k}\Omega} \quad (1)$$

where:
V_{ISF} is referenced to Pin 2. V_{ISF} can be an external voltage source, V_{CC}, or a GPO output as explained in the following paragraphs.
R_{ISF} is the external resistor between the ISF pin and V_{ISF}.

The active load current (into the IN pin) is directly proportional to I_{ISF} and can be calculated by Equation 2.

$$I_{AL} = I_{ISF} \times 27 \quad (2)$$

The ADA4800 allows for additional power savings by reducing the active load current. The active load current can be logically controlled by connecting the ISF pin to any general-purpose output (GPO) pin of a system microcontroller through an external resistor. A GPO logic high enables the flow of the active load current. Appling $-V_S$ or connecting a high-Z to the ISF pin places the ADA4800 into power save mode by shutting down the active load current.

Figure 22 illustrates an ADA4800 application configuration for using this power save feature.

An external resistor connected between the ISF and the microcontroller GPO pin determines the amount of current that flows into the input pin. This current can be calculated by using Equation 1 and Equation 2.

SETTING BANDWIDTH WITH PIN 4 (IDRV)

The IDRV pin establishes the buffer's I_{CC} quiescent current. As I_{CC} is increased, power dissipation and bandwidth both increase. Set the current using Equation 3.

$$I_{IDRV} = \frac{V_{IDRV} - 0.8\ \text{V}}{R_{IDRV} + 28\ \text{k}\Omega} \quad (3)$$

where:
V_{IDRV} is referenced to Pin 2. V_{IDRV} can be an external voltage source or V_{CC}.
R_{IDRV} is the external resistor between the IDRV pin and V_{IDRV}.

The I_{CC} current is directly proportional to I_{IDRV} and can be calculated by Equation 4.

$$I_{CC} = I_{IDRV} \times 26 \quad (4)$$

Applying $-V_S$ to the IDRV pin shuts down the buffer.

APPLICATIONS INFORMATION

OPEN SOURCE CCD OUTPUT BUFFER

With low power, high slew rate, and fast settling time, the ADA4800 is the ideal solution for an output buffer for CCD sensors with an open source output configuration. Figure 21 shows a typical application circuit for the ADA4800 as a CCD sensor output buffer.

The output of the CCD is connected directly to the IN pin of the ADA4800, whose OUT pin is then ac-coupled into the input of the analog front end.

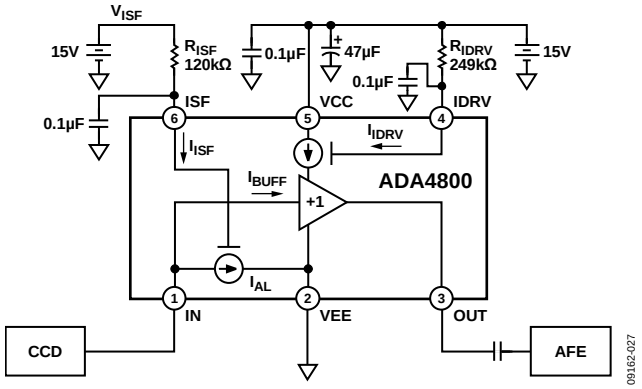

Figure 21. Typical Application Block Diagram

To help reduce the effects of power supply noise coupling into the ISF and IDRV pins, use 0.1 µF ceramic bypass decoupling capacitors. For best performance, place these capacitors as close to each of these pins as is physically possible.

POWER SAVE MODE

The buffer of the ADA4800 consumes only 20 mW of static power. To achieve even more power savings, the ADA4800 active load current can be switched off during standby mode or reduced during monitoring mode. Figure 22 illustrates the ADA4800 as an open source CCD buffer configured for using this power save feature. Power save mode allows I_{AL} current to be logically controlled by connecting the ISF pin to any general-purpose output (GPO) pin of the system microcontroller through an external resistor. A GPO logic high enables the flow of input sink current, while a logic low disables the input sink current and asserts the power save mode.

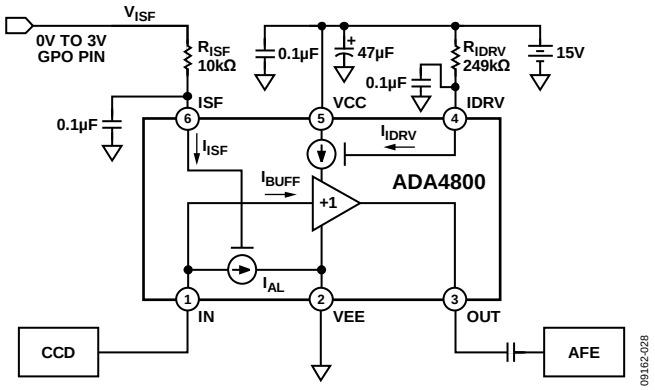

Figure 22. Using GPO to Drive ISF Voltage

Figure 23 shows an example of the ADA4800 power save feature.

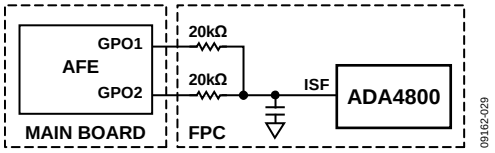

Figure 23. Example Block Diagram for Sink Current Selection

Three combinations of I_{AL} are provided with Figure 23. Selection of the I_{AL} is controlled by the logic signals applied to the GPO1 and GPO2 pins. Table 5 summarizes the I_{AL} selections.

Table 5. Input Sink Current Selection

Mode	GPO1	GPO2	Resistance (kΩ)	Active Load Current, I_{AL} (mA)
Standby	High-Z	High-Z	High-Z	0
	0	0	N/A	
Sleep	High-Z	1	20	1.90
	1	High-Z	20	
Active	1	1	10	3.36

POWER SUPPLY BYPASSING

Attention must be paid to bypassing the power supply pin of the ADA4800. Use high quality capacitors with low equivalent series resistance (ESR), such as multilayer ceramic capacitors (MLCCs), to minimize supply voltage ripple and power dissipation. A large, usually tantalum, 2.2 µF to 47 µF capacitor located in close proximity to the ADA4800 is required to provide good decoupling for lower frequency signals. The actual value is determined by the circuit transient and frequency requirements. In addition, 0.1 µF MLCC decoupling capacitors should be located as close to the power supply pin as is physically possible, no more than ⅛ inch away. The ground returns should terminate immediately into the ground plane. Locating the bypass capacitor return close to the load return minimizes ground loops and improves performance.

POWER SEQUENCING

All I/O pins are ESD protected with internal back-to-back diodes connected to VCC and GND as shown in Figure 24. With the ADA4800 supply turned off (V_{CC} = 0 V), a voltage on an I/O pin can turn on the protection diodes and cause permanent damage or destroy the IC. To prevent this condition during power-on, no voltages should be applied to any I/O pins until VCC is fully on and settled. During power-off, I/O pin voltages should be removed or reduced to 0 V before VCC is turned off.

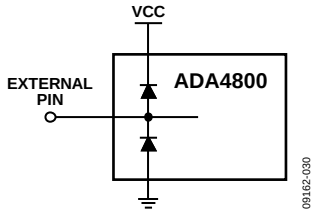

Figure 24. Simplified Input/Output Circuitry

In the presence of a voltage on an I/O pin with V_{CC} = 0 V, the current should be limited to 5 mA or less by the source or by adding a series resistor.

OUTLINE DIMENSIONS

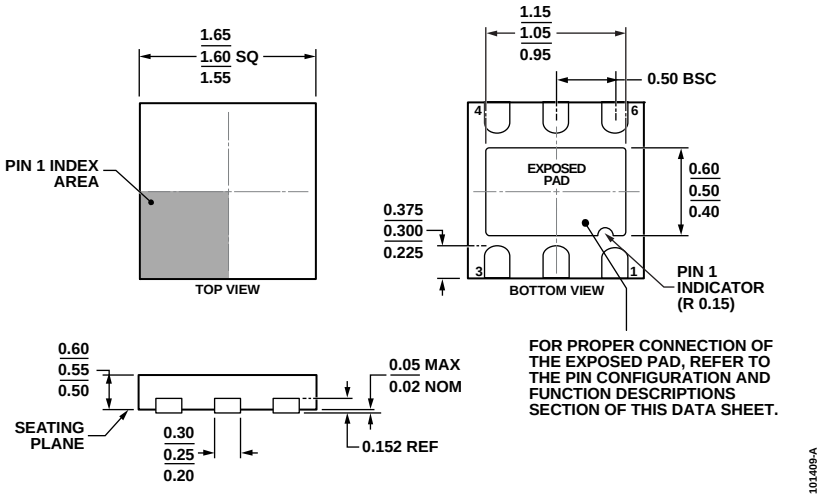

Figure 25. 6-Lead Lead Frame Chip Scale Package [LFCSP_UD]
1.60 mm × 1.60 mm Body, Ultra Thin, Dual Lead
(CP-6-4)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option	Branding
ADA4800ACPZ-R2	−40°C to +85°C	6-Lead Lead Frame Chip Scale Package [LFCSP_UD]	CP-6-4	H2E
ADA4800ACPZ-R7	−40°C to +85°C	6-Lead Lead Frame Chip Scale Package [LFCSP_UD]	CP-6-4	H2E
ADA4800ACPZ-RL	−40°C to +85°C	6-Lead Lead Frame Chip Scale Package [LFCSP_UD]	CP-6-4	H2E

[1] Z = RoHS Compliant Part.

NOTES

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D09162-0-7/10(A)