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REVISION HISTORY

7/15—Rev. G to Rev. H

Changed CP-16-4 to CP-16-23 and Changed LFCSP_VQ to LFCSP_WQ	Throughout
Changes to Figure 5.....	1
Changed Differential Input Voltage Parameter, Table 4.....	5
Updated Outline Dimensions	12
Changes to Ordering Guide	15

4/11—Rev. F to Rev. G

Changes to Figure 1.....	1
Updated Outline Dimensions	12

6/10—Rev. E to Rev. F

Added Differential Input Current to Table 4	5
Changes to Figure 14 and Figure 17.....	7

10/09—Rev. D to Rev. E

Changes to Product Title, General Description Section, and Figure 5	1
Updated Outline Dimensions (RM-8).....	13
Changes to Ordering Guide	14

6/09—Rev. C to Rev. D

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10/08—Rev. B to Rev. C

Added ADA4004-1 and ADA4004-2	Universal
Added 5-Lead SOT, 8-Lead SOIC, and 8-Lead MSOP	Universal
Changes to Features Section	1
Added Figure 1 to Figure 3; Renumbered Sequentially.....	1
Changes to General Description Section	1

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Added Phase Margin Parameter, Table 2.....	3
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11/07—Rev. A to Rev. B

Changed V_S to V_{SY}	Universal
Changes to General Description	1
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7/06—Rev. 0 to Rev. A

Changes to Table 4.....	5
Updated Outline Dimensions.....	12
Changes to Ordering Guide	12

1/06—Revision 0: Initial Version

SPECIFICATIONS

$V_{SY} = \pm 5\text{ V}$, $V_{CM} = 0\text{ V}$, $T_A = 25^\circ\text{C}$, unless otherwise specified.

Table 2.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}	$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$		40	140	μV
					300	μV
Input Bias Current	I_B	$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$		40	85	nA
					165	nA
Input Offset Current	I_{OS}	$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$		40	85	nA
					100	nA
Input Voltage Range	IVR		-3.5		+3.5	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = -3.0\text{ V to }+3.0\text{ V}$	105	111		dB
		$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$	95	110		dB
Open-Loop Gain	A_{VO}	$R_L = 2\text{ k}\Omega$, $V_{OUT} = -2.5\text{ V to }+2.5\text{ V}$	250	400		V/mV
		$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$	170			V/mV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$	$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$		0.7	1	$\mu\text{V}/^\circ\text{C}$
OUTPUT CHARACTERISTICS						
Output Voltage High	V_{OH}	$R_L = 2\text{ k}\Omega$ to ground	3.7	3.9		V
		$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$	3.4	3.6		V
Output Voltage Low	V_{OL}	$R_L = 2\text{ k}\Omega$ to ground		-3.6	-3.55	V
		$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$		-3.6	-3.4	V
Short-Circuit Limit	I_{SC}	$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$		25		mA
						mA
Output Current	I_O	$V_{OUT} = \pm 3.6\text{ V}$		± 10		mA
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	$V_{SY} = \pm 5\text{ V to } \pm 15\text{ V}$	110	118		dB
		$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$	110			dB
Supply Current per Amplifier	I_{SY}	$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$			2.0	mA
					2.2	mA
DYNAMIC PERFORMANCE						
Slew Rate	SR	$R_L = 2\text{ k}\Omega$ to ground		2.7		V/ μs
Gain Bandwidth Product	GBP			12		MHz
Phase Margin	Φ_M			48		Degrees
NOISE PERFORMANCE						
Voltage Noise	$e_{n\text{ p-p}}$	$f = 0.1\text{ Hz to }10\text{ Hz}$		0.1		$\mu\text{V p-p}$
Voltage Noise Density	e_n	$f = 1\text{ kHz}$		1.8		nV/ $\sqrt{\text{Hz}}$
Current Noise Density	i_n	$f = 10\text{ Hz}$		3.5		pA/ $\sqrt{\text{Hz}}$
Current Noise Density	i_n	$f = 200\text{ Hz}$		1.2		pA/ $\sqrt{\text{Hz}}$

$V_{SY} = \pm 15\text{ V}$, $V_{CM} = 0\text{ V}$, $T_A = 25^\circ\text{C}$, unless otherwise specified.

Table 3.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}	$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$		40	125	μV
Input Bias Current	I_B	$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$		40	270	μV
Input Offset Current	I_{OS}	$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$			90	nA
Input Voltage Range	IVR	$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$	-12.5		165	nA
Common-Mode Rejection Ratio	CMRR	$V_{CM} = -12.5\text{ V to } +12.5\text{ V}$	110	113	60	nA
Open-Loop Gain	A_{VO}	$R_L = 2\text{ k}\Omega$, $V_{OUT} = -12.0\text{ V to } +12.0\text{ V}$	500	1200	100	nA
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$	$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$	250	500	1	$\mu\text{V}/^\circ\text{C}$
OUTPUT CHARACTERISTICS						
Output Voltage High	V_{OH}	$R_L = 2\text{ k}\Omega$ to ground	13.4	13.6		V
Output Voltage Low	V_{OL}	$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$	13.1	13.3		V
Short-Circuit Limit	I_{SC}	$R_L = 2\text{ k}\Omega$ to ground		-13.3	-13.2	V
Output Current	I_O	$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$		-13.25	-13.15	V
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	$V_{SY} = \pm 5\text{ V to } \pm 15\text{ V}$	110	118		dB
Supply Current per Amplifier	I_{SY}	$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$	110		2.2	dB
		$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$			2.4	mA
DYNAMIC PERFORMANCE						
Slew Rate	SR	$R_L = 2\text{ k}\Omega$ to ground		2.7		$\text{V}/\mu\text{s}$
Gain Bandwidth Product	GBP			12		MHz
Phase Margin	Φ_M			48		Degrees
NOISE PERFORMANCE						
Voltage Noise	$e_{n\text{ p-p}}$	$f = 0.1\text{ Hz to } 10\text{ Hz}$		0.15		$\mu\text{V p-p}$
Voltage Noise Density	e_n	$f = 1\text{ kHz}$		1.8		$\text{nV}/\sqrt{\text{Hz}}$
Current Noise Density	i_n	$f = 10\text{ Hz}$		3.5		$\text{pA}/\sqrt{\text{Hz}}$
Current Noise Density	i_n	$f = 200\text{ Hz}$		1.2		$\text{pA}/\sqrt{\text{Hz}}$

ABSOLUTE MAXIMUM RATINGS

Table 4.

Parameter	Rating
Supply Voltage	$\pm 18\text{ V}$ or $+36\text{ V}$
Input Voltage	$V^- < V_{IN} < V^+$
Differential Input Voltage	$\pm 600\text{ mV}$
Differential Input Current	$\pm 5\text{ mA}$
Output Short-Circuit Duration to GND	Indefinite
Storage Temperature Range	-65°C to $+150^\circ\text{C}$
Operating Temperature Range	-40°C to $+125^\circ\text{C}$
Junction Temperature Range	-65°C to $+150^\circ\text{C}$
Lead Temperature (Soldering 60 sec)	300°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

θ_{JA} is specified with the device soldered on a circuit board with its exposed paddle soldered to a pad (if applicable) on a 4-layer JEDEC standard printed circuit board with zero airflow.

Table 5.

Package Type	θ_{JA}	θ_{JC}	Unit
5-Lead SOT (RJ-5)	230	92	$^\circ\text{C/W}$
8-Lead SOIC (R-8), ADA4004-1	177	53	$^\circ\text{C/W}$
8-Lead SOIC (R-8), ADA4004-2	155	45	$^\circ\text{C/W}$
8-Lead MSOP (RM-8)	186	52	$^\circ\text{C/W}$
14-Lead SOIC_N (R-14)	115	36	$^\circ\text{C/W}$
16-Lead LFCSP_VQ (CP-16-4)	44	31.5	$^\circ\text{C/W}$

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

TYPICAL PERFORMANCE CHARACTERISTICS

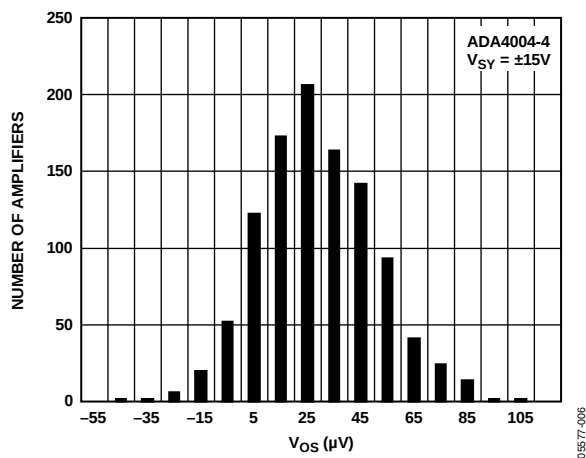


Figure 6. Number of Amplifiers vs. Input Offset Voltage

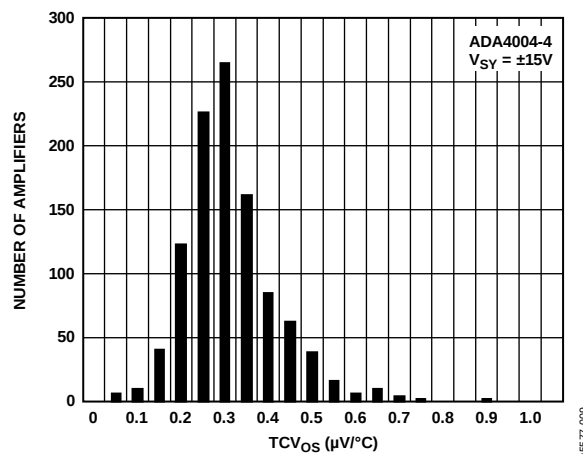


Figure 9. Number of Amplifiers vs. TCV_{OS}

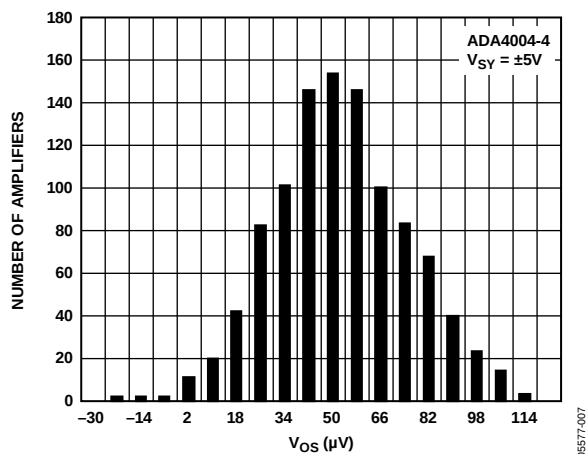


Figure 7. Number of Amplifiers vs. Input Offset Voltage

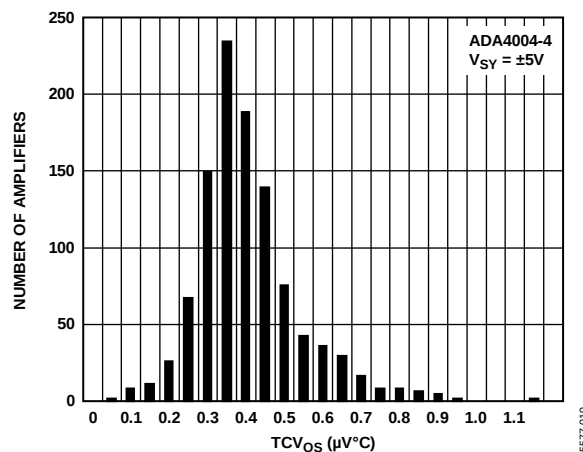


Figure 10. Number of Amplifiers vs. TCV_{OS}

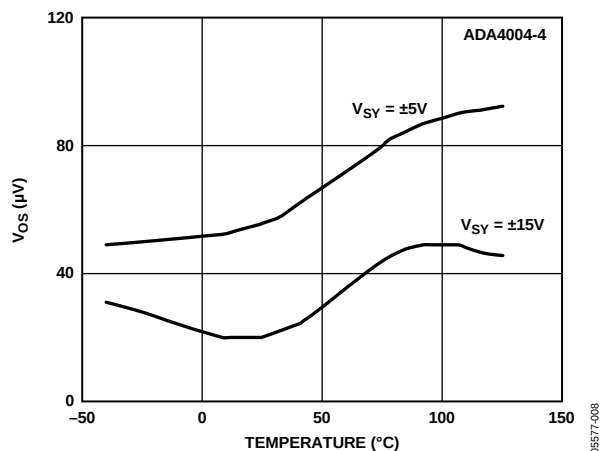


Figure 8. Input Offset Voltage vs. Temperature

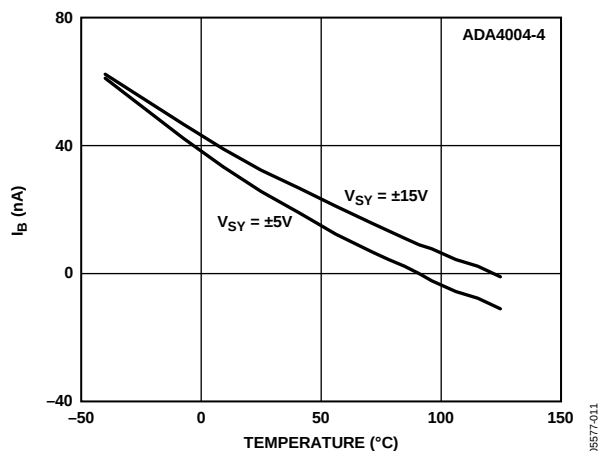


Figure 11. Input Bias Current vs. Temperature

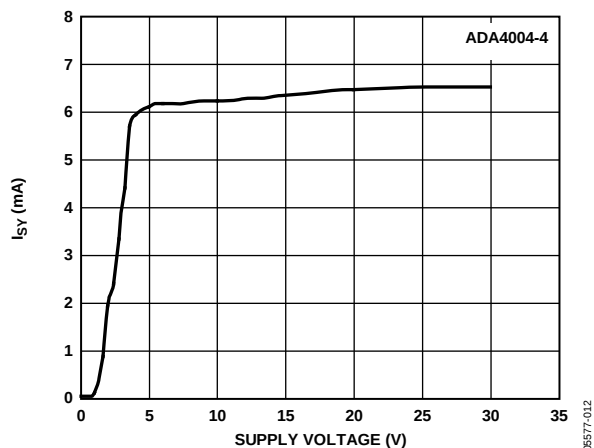


Figure 12. Supply Current vs. Total Supply Voltage

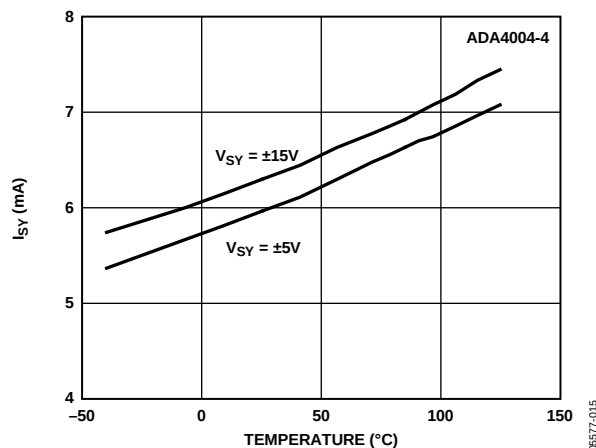


Figure 15. Supply Current vs. Temperature

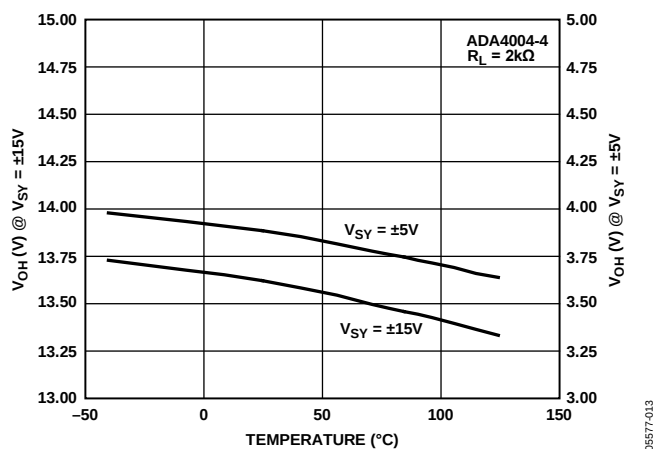
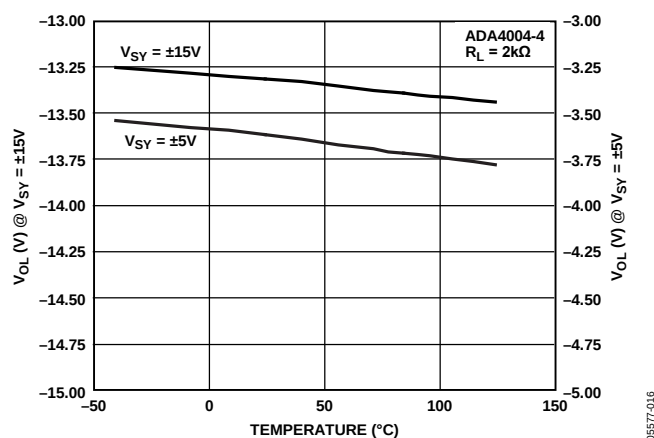
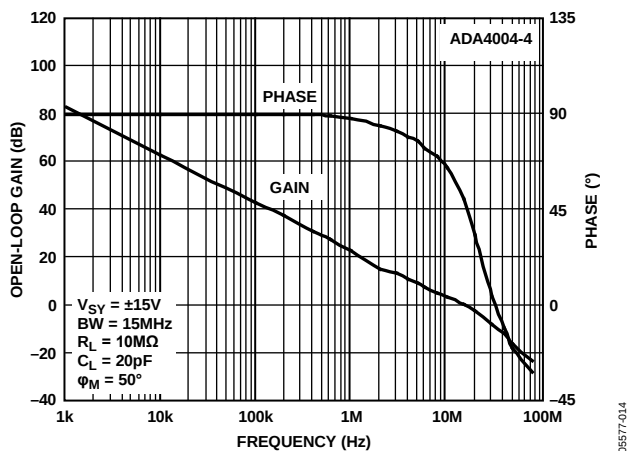
Figure 13. V_{OH} vs. TemperatureFigure 16. V_{OL} vs. Temperature

Figure 14. Open-Loop Gain and Phase vs. Frequency

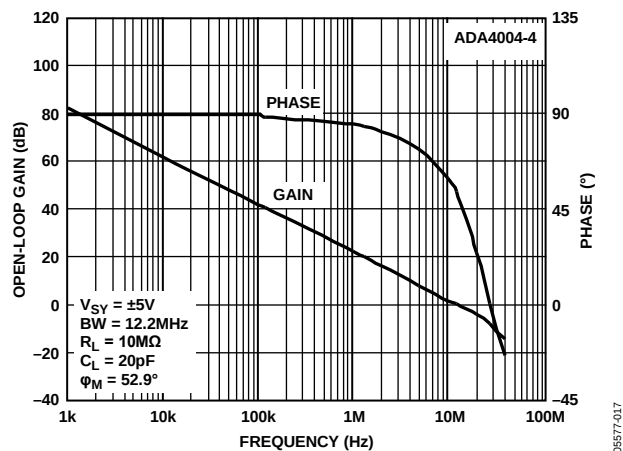


Figure 17. Open-Loop Gain and Phase vs. Frequency

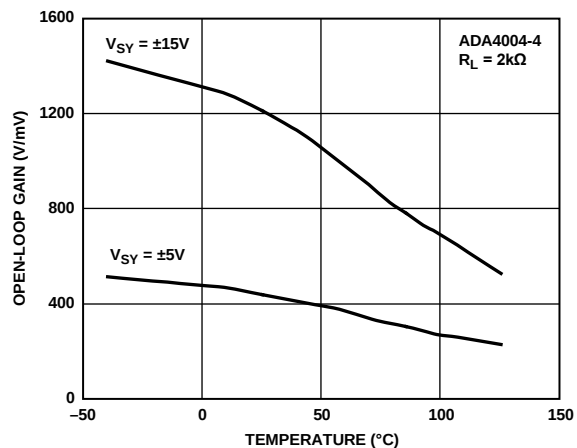


Figure 18. Open-Loop Gain vs. Temperature

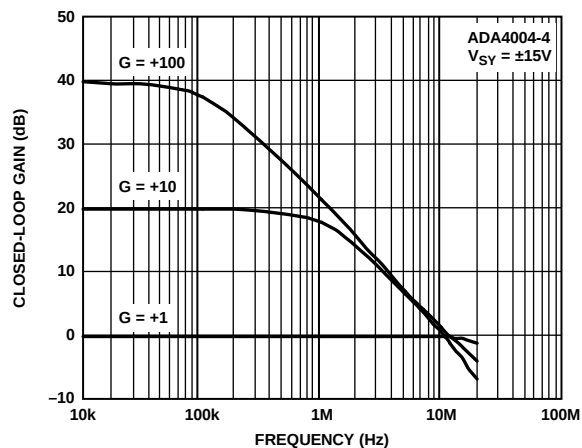


Figure 21. Closed-Loop Gain vs. Frequency

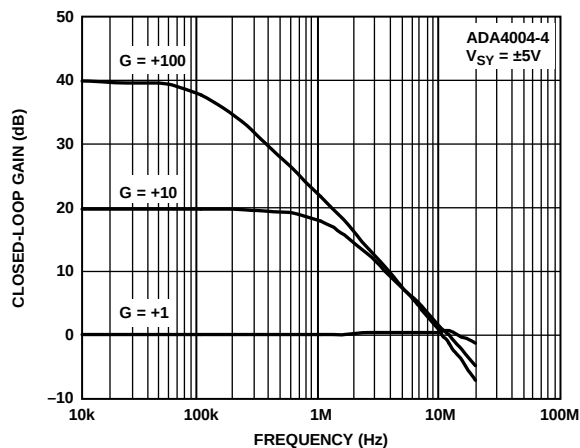


Figure 19. Closed-Loop Gain vs. Frequency

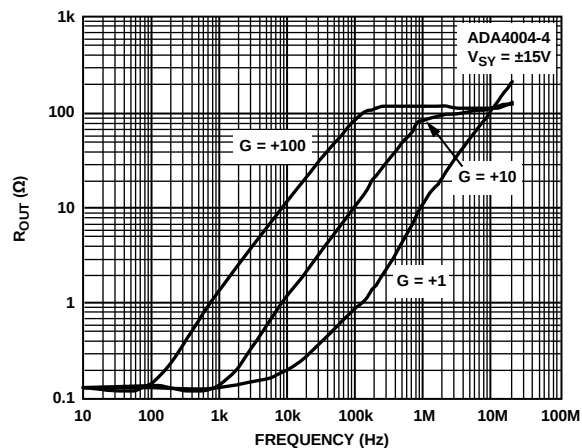


Figure 22. Output Impedance vs. Frequency

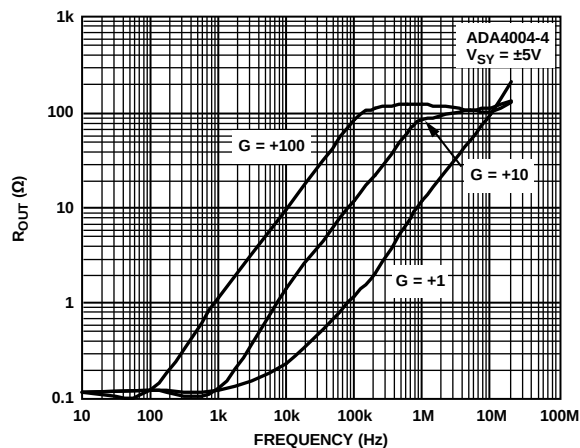


Figure 20. Output Impedance vs. Frequency

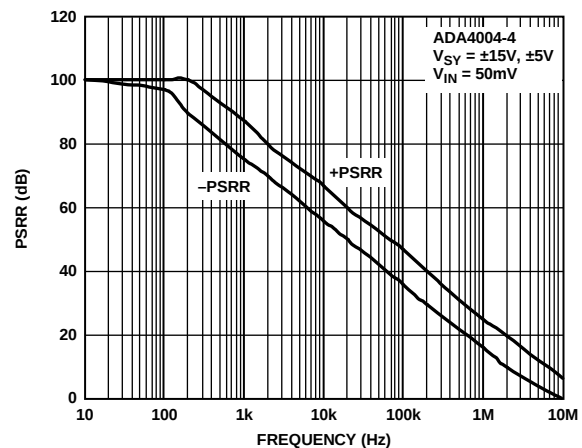


Figure 23. PSRR vs. Frequency

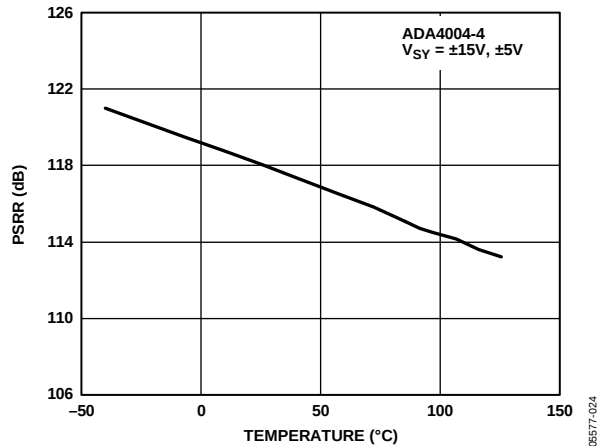


Figure 24. PSRR vs. Temperature

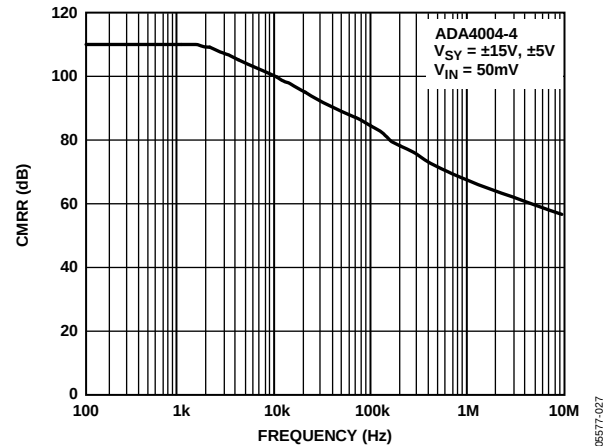


Figure 27. CMRR vs. Frequency

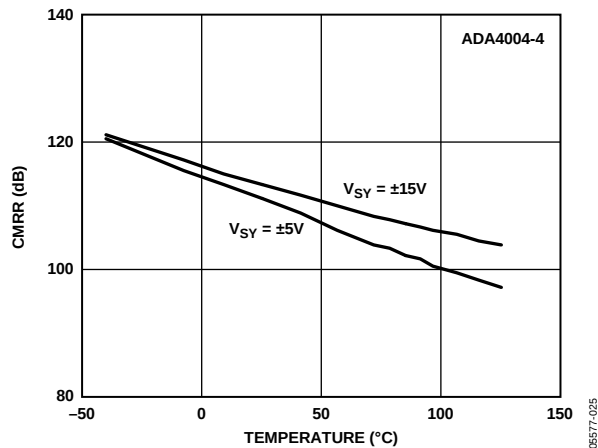


Figure 25. CMRR vs. Temperature

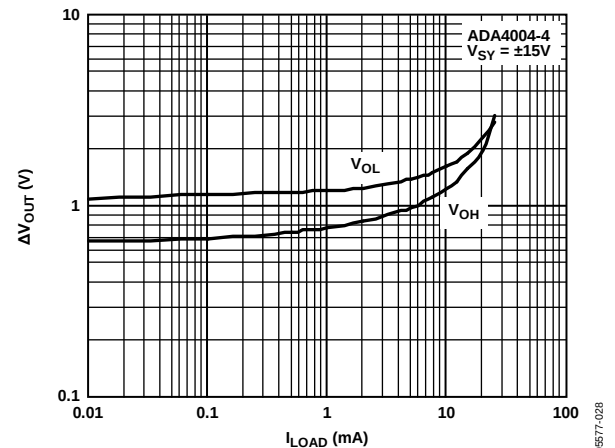


Figure 28. Output Voltage vs. Current Load

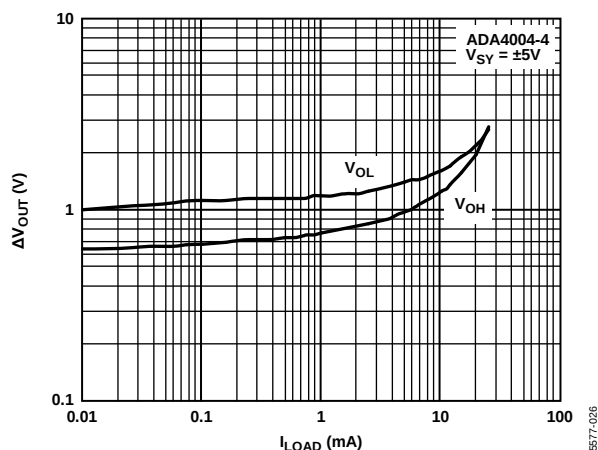


Figure 26. Output Voltage vs. Current Load

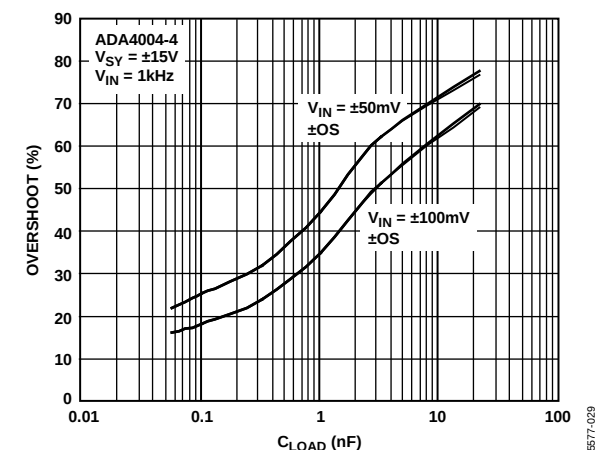


Figure 29. Small-Signal Overshoot vs. Capacitive Load

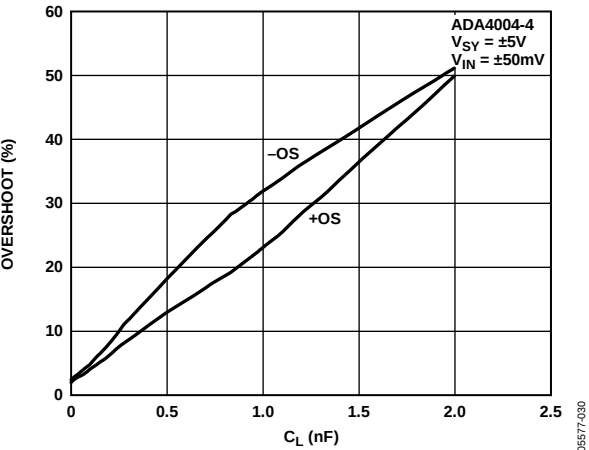


Figure 30. Small-Signal Overshoot vs. Capacitive Load

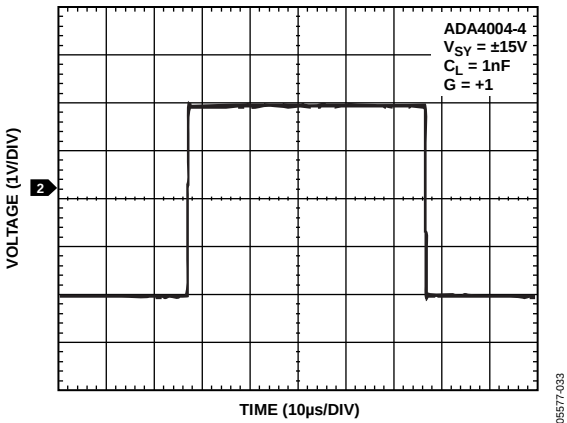


Figure 33. Large-Signal Transient Response

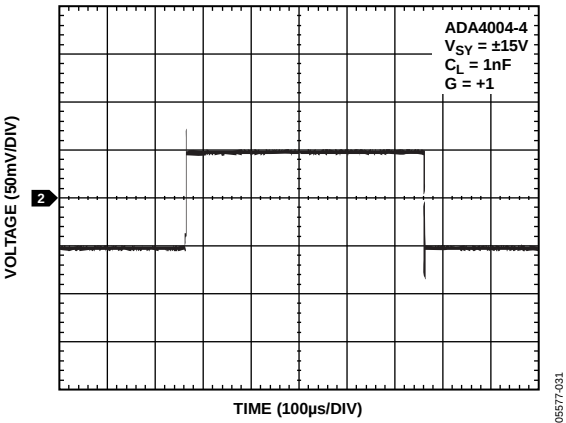


Figure 31. Small-Signal Transient Response

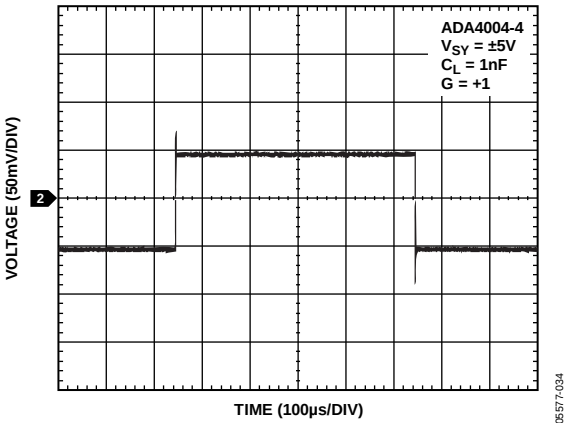


Figure 34. Small-Signal Transient Response

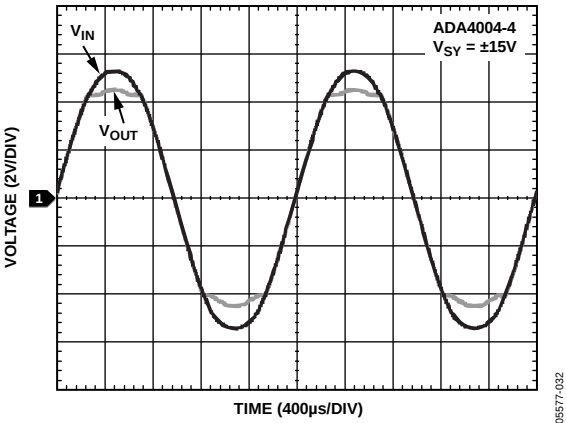


Figure 32. No Phase Reversal

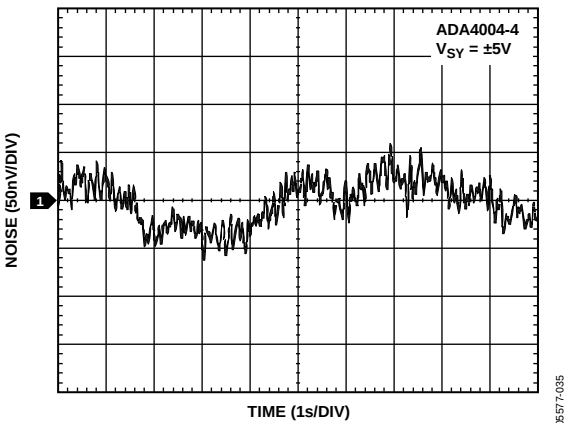


Figure 35. Voltage Noise (0.1 Hz to 10 Hz)

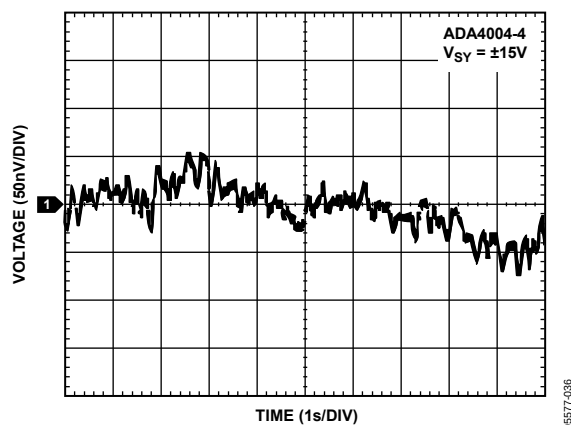


Figure 36. Voltage Noise (0.1 Hz to 10 Hz)

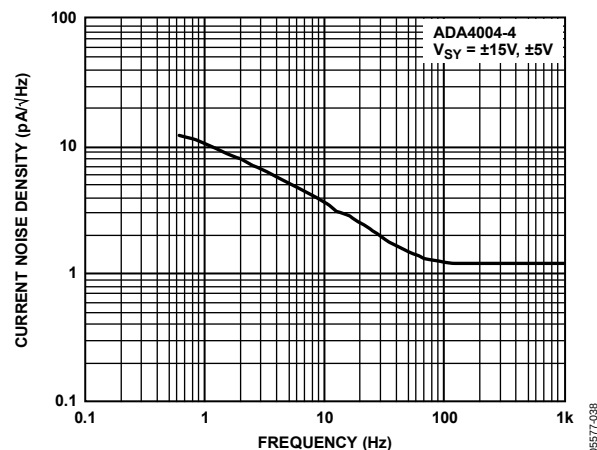


Figure 38. Current Noise Density vs. Frequency

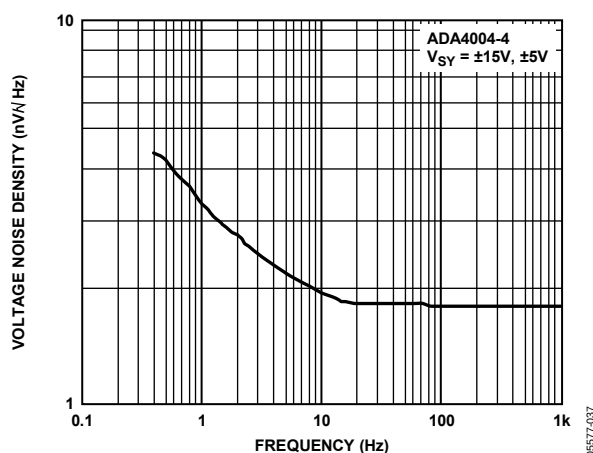


Figure 37. Voltage Noise Density vs. Frequency

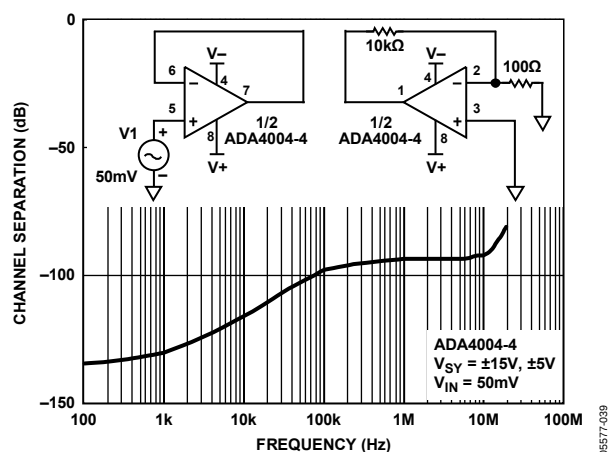
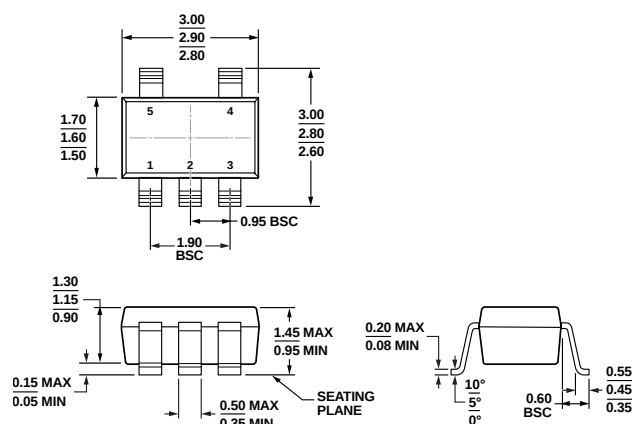


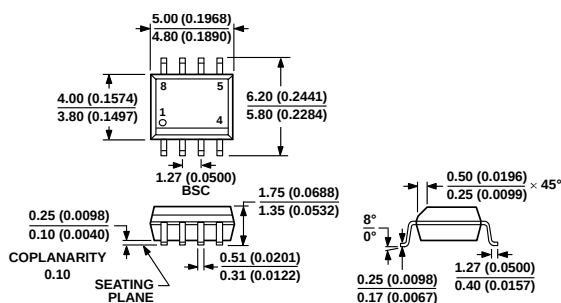
Figure 39. Channel Separation vs. Frequency

OUTLINE DIMENSIONS



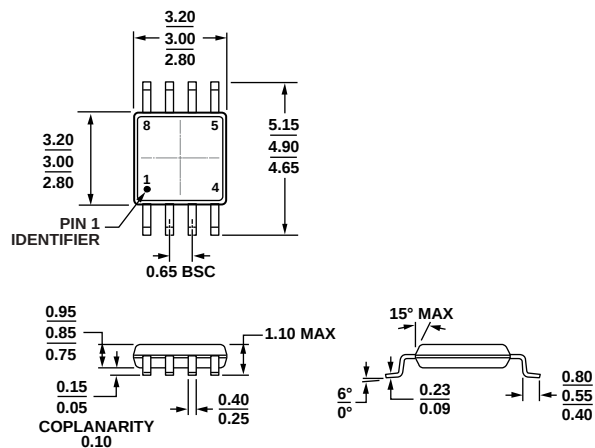
COMPLIANT TO JEDEC STANDARDS MO-178-AA

Figure 40. 5-Lead Small Outline Transistor Package [SOT-23]
(RJ-5)
Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MS-012-AA
CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS
(IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR
REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

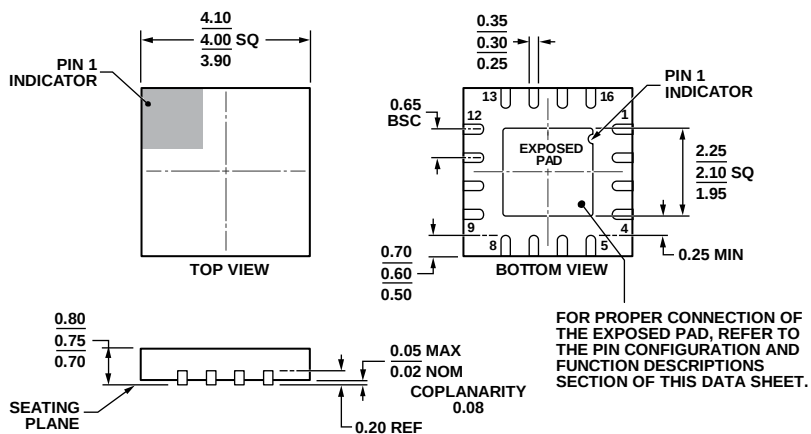
Figure 41. 8-Lead Standard Small Outline Package [SOIC_N]
Narrow Body (R-8)
Dimensions shown in millimeters and (inches)



COMPLIANT TO JEDEC STANDARDS MO-187-AA

Figure 42. 8-Lead Mini Small Outline Package [MSOP]
(RM-8)

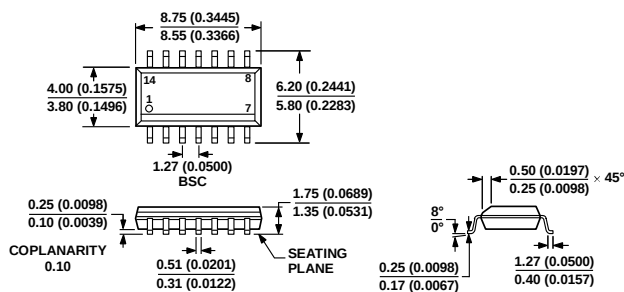
Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MO-220-WGGC.

Figure 43. 16-Lead Lead Frame Chip Scale Package [LFCSP_WQ]
4 mm × 4 mm Body, Very Very Thin Quad
(CP-16-23)

Dimensions shown in millimeters

COMPLIANT TO JEDEC STANDARDS MS-012-AB
CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS
(IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR
REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.Figure 44. 14-Lead Standard Small Outline Package [SOIC_N]
Narrow Body
(R-14)

Dimensions shown in millimeters and (inches)

ORDERING GUIDE

Model ¹	Temperature Range	Package Description	Package Option	Branding
ADA4004-1ARJZ-R2	–40°C to +125°C	5-Lead SOT-23	RJ-5	A1M
ADA4004-1ARJZ-R7	–40°C to +125°C	5-Lead SOT-23	RJ-5	A1M
ADA4004-1ARJZ-RL	–40°C to +125°C	5-Lead SOT-23	RJ-5	A1M
ADA4004-1ARZ	–40°C to +125°C	8-Lead SOIC_N	R-8	
ADA4004-1ARZ-R7	–40°C to +125°C	8-Lead SOIC_N	R-8	
ADA4004-1ARZ-RL	–40°C to +125°C	8-Lead SOIC_N	R-8	
ADA4004-2ARMZ	–40°C to +125°C	8-Lead MSOP	RM-8	A1N
ADA4004-2ARMZ-RL	–40°C to +125°C	8-Lead MSOP	RM-8	A1N
ADA4004-2ARMZ-R7	–40°C to +125°C	8-Lead MSOP	RM-8	A1N
ADA4004-2ARZ	–40°C to +125°C	8-Lead SOIC_N	R-8	
ADA4004-2ARZ-RL	–40°C to +125°C	8-Lead SOIC_N	R-8	
ADA4004-2ARZ-R7	–40°C to +125°C	8-Lead SOIC_N	R-8	
ADA4004-4ACPZ-R2	–40°C to +125°C	16-Lead LFCSP_WQ	CP-16-23	
ADA4004-4ACPZ-R7	–40°C to +125°C	16-Lead LFCSP_WQ	CP-16-23	
ADA4004-4ACPZ-RL	–40°C to +125°C	16-Lead LFCSP_WQ	CP-16-23	
ADA4004-4ARZ	–40°C to +125°C	14-Lead SOIC_N	R-14	
ADA4004-4ARZ-R7	–40°C to +125°C	14-Lead SOIC_N	R-14	
ADA4004-4ARZ-RL	–40°C to +125°C	14-Lead SOIC_N	R-14	

¹ Z = RoHS Compliant Part.

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