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FUNCTIONAL BLOCK DIAGRAM

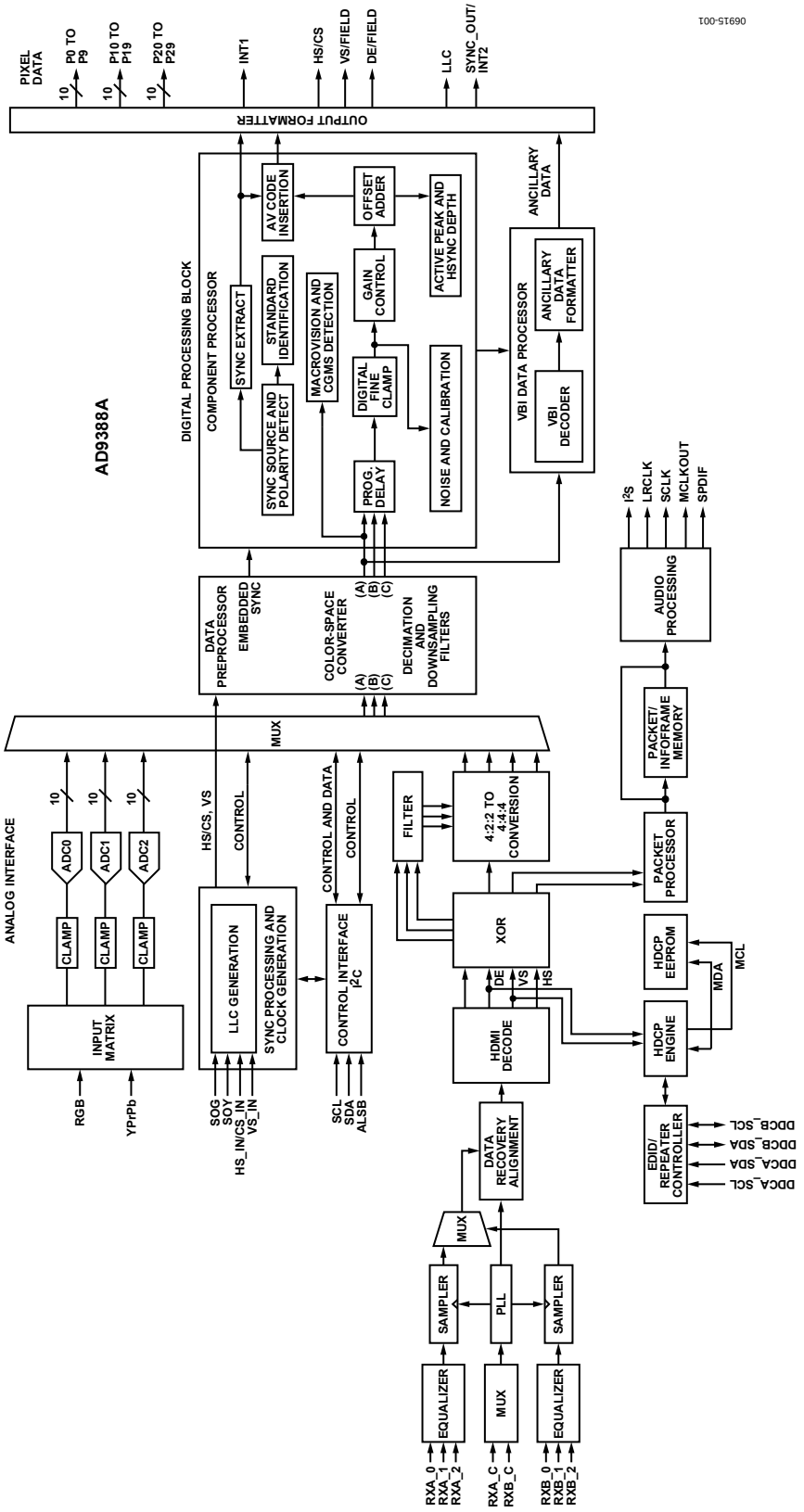


Figure 1.

SPECIFICATIONS

ELECTRICAL CHARACTERISTICS

AVDD = 1.71 V to 1.89 V, DVDD = 1.62 V to 1.98 V, DVDDIO = 2.97 V to 3.63 V, PVDD = 1.71 V to 1.89 V, TVDD = 3.135 V to 3.465 V, CVDD = 1.71 V to 1.89 V. Operating temperature range is −40°C to +85°C, unless otherwise noted.

Table 1.

Parameter[1]	Symbol	Test Conditions	Min	Typ	Max	Unit
STATIC PERFORMANCE[2]						
Resolution (Each ADC)	N				10	Bits
Integral Nonlinearity	INL	BSL at 27 MHz (@ a 10-bit level)		−0.5/+2		LSB
		BSL at 54 MHz (@ a 10-bit level)		−0.5/+2		LSB
		BSL at 74 MHz (@ a 10-bit level)		−0.5/+1.5		LSB
		BSL at 110 MHz (@ a 10-bit level)		−0.7/+2		LSB
		BSL at 170 MHz (@ an 8-bit level)		−0.25/+0.5		LSB
Differential Nonlinearity	DNL	At 27 MHz (@ a 10-bit level)		−0.5/+0.5		LSB
		At 54 MHz (@ a 10-bit level)		±0.5		LSB
		At 74 MHz (@ a 10-bit level)		±0.5		LSB
		At 110 MHz (@ a 10-bit level)		±0.5		LSB
		At 170 MHz (@ an 8-bit level)		−0.25/+0.2		LSB
DIGITAL INPUTS						
Input High Voltage[3]	V_{IH}		2			V
		HS_IN, VS_IN low trigger mode	0.7			V
Input Low Voltage[3]	V_{IL}				0.8	V
		HS_IN, VS_IN low trigger mode			0.3	V
Input Current	I_{IN}	Pin 21 ($\overline{\text{RESET}}$)	−60		+60	µA
		All input pins other than Pin 21	−10		+10	µA
Input Capacitance[4]	C_{IN}				10	pF
DIGITAL OUTPUTS						
Output High Voltage[5]	V_{OH}	I_{SOURCE} = 0.4 mA	2.4			V
Output Low Voltage[5]	V_{OL}	I_{SINK} = 3.2 mA			0.4	V
High Impedance Leakage Current	I_{LEAK}				10	µA
Output Capacitance[4]	C_{OUT}				20	pF
POWER REQUIREMENTS[4]						
Digital Core Power Supply	DVDD		1.62	1.8	1.98	V
Digital I/O Power Supply	DVDDIO		2.97	3.3	3.63	V
PLL Power Supply	PVDD		1.71	1.8	1.89	V
Analog Power Supply	AVDD		1.71	1.8	1.89	V
Terminator Power Supply	TVDD		3.135	3.3	3.465	V
Comparator Power Supply	CVDD		1.71	1.8	1.89	V
Digital Core Supply Current	I_{DVDD}	Graphics RGB sampling @ 108 MHz[6, 7]		141	290	mA
		YPrPb 1080p sampling @ 148.5 MHz[6, 7]		203	305	mA
		HDMI RGB sampling @ 165 MHz[7, 8, 9]		242	358	mA
		HDMI RGB sampling @ 225 MHz[7, 8, 9]		242	414	mA
Digital I/O Supply Current	I_{DVDDIO}	Graphics RGB sampling @ 108 MHz[6, 7]		17	80	mA
		YPrPb 1080p sampling @ 148.5 MHz[6, 7]		42	136	mA
		HDMI RGB sampling @ 165 MHz[7, 8, 9]		17	192	mA
		HDMI RGB sampling @ 225 MHz[7, 8, 9]		20	151	mA
HDMI Comparators	I_{CVDD}	Graphics RGB sampling @ 108 MHz[6, 7]		56	83	mA

Parameter[1]	Symbol	Test Conditions	Min	Typ	Max	Unit
TMDS PLL and Equalizer Supply Current		YPrPb 1080p sampling @ 148.5 MHz[6, 7]		56	83	mA
		HDMI RGB sampling @ 165 MHz[7, 8, 9]		86	111	mA
		HDMI RGB sampling @ 225 MHz[7, 8, 9]		95	125	mA
Analog Supply Current	I_{AVDD}	Graphics RGB sampling @ 108 MHz[6, 7]		174	312	mA
		YPrPb 1080p sampling @ 148.5 MHz[6, 7]		180	318	mA
		HDMI RGB sampling @ 165 MHz[7, 8, 9]		0	2	mA
		HDMI RGB sampling @ 225 MHz[7, 8, 9]		0	2	mA
Terminator Supply Current	I_{TVDD}	Graphics RGB sampling @ 108 MHz[6, 7]		12	20	mA
		YPrPb 1080p sampling @ 148.5 MHz[6, 7]		12	20	mA
		HDMI RGB sampling @ 165 MHz[7, 8, 9, 10]		42	97	mA
		HDMI RGB sampling @ 225 MHz[7, 8, 9, 10]		63	100	mA
Audio and Video Supply Current	I_{PVDD}	Graphics RGB sampling @ 108 MHz[6, 7]		14	22	mA
		YPrPb 1080p sampling @ 148.5 MHz[6, 7]		19	25	mA
		HDMI RGB sampling @ 165 MHz[7, 8, 9]		10	20	mA
		HDMI RGB sampling @ 225 MHz[7, 8, 9]		15	21	mA
Power-Down Current	I_{PWRDN}			11.6		mA
Power-Up Time	t_{PWRUP}			25		ms

[1] The minimum/maximum specifications are guaranteed over the −40°C to +85°C temperature range (T_{MIN} to T_{MAX}).
[2] All ADC linearity tests performed at input range of full scale − 12.5% and at zero scale + 12.5%.
[3] Pin 1, Pin 105, Pin 106, and Pin 144 are 5 V tolerant.
[4] Guaranteed by characterization.
[5] V_{OH} and V_{OL} levels obtained using default drive strength value (0x15) in User Map Register 0xF4.
[6] Current measurements for analog inputs were made with HDMI/analog simultaneous mode disabled (User Map Register 0xBA, Bit 7, programmed with Value 0) and no HDMI sources connected to the part.
[7] Typical current measurements were taken with nominal voltage supply levels and an SMPTE bar video pattern input. Maximum current measurements were taken with maximum rating voltage supply levels and a MoiréX video pattern input.
[8] Current measurements for HDMI inputs were made with a source connected to the active HDMI port and no source connected to the inactive HDMI port.
[9] Audio stream is an uncompressed stereo audio sampling frequency of f_S = 48 kHz and MCLKOUT = 256 f_S.
[10] The terminator supply current may vary with the HDMI source in use.

ANALOG AND HDMI SPECIFICATIONS

AVDD = 1.71 V to 1.89 V, DVDD = 1.62 V to 1.98 V, DVDDIO = 2.97 V to 3.63 V, PVDD = 1.71 V to 1.89 V, TVDD = 3.135 V to 3.465 V, CVDD = 1.71 V to 1.89 V. Operating temperature range is −40°C to +85°C, unless otherwise noted.

Table 2.

Parameter[1, 2]	Test Conditions	Min	Typ	Max	Unit
ANALOG					
Clamp Circuitry					
External Clamp Capacitor			0.1		µF
Input Impedance (Except Pin 74)	Clamps switched off		10		MΩ
Input Impedance of Pin 74			20		kΩ
CML			0.88		V
ADC Full-Scale Level			CML + 0.5		V
ADC Zero-Scale Level			CML − 0.5		V
ADC Dynamic Range			1		V
Clamp Level (When Locked)	Component input (Y signal)		CML − 0.120		V
	Component input (Pr signal)		CML		V
	Component input (Pb signal)		CML		V
	PC RGB input (R, G, B signals)		CML − 0.120		V
HDMI SPECIFICATIONS[3]					
Intrapair (Positive-to-Negative) Differential Input Skew[4, 5]				0.4 t_{bit}	
Channel-to-Channel Differential Input Skew[5, 6]				0.2 t_{pixel} + 1.78 ns	

[1] The minimum/maximum specifications are guaranteed over the −40°C to +85°C temperature range.
[2] Guaranteed by characterization.
[3] Guaranteed by design.
[4] t_{bit} is 1/10 the pixel period of the TMDS clock.
[5] The unit of measurement depends on the video applied and the TMDS clock frequency.
[6] t_{pixel} is the period of the TMDS clock.

DATA AND I²C TIMING CHARACTERISTICS

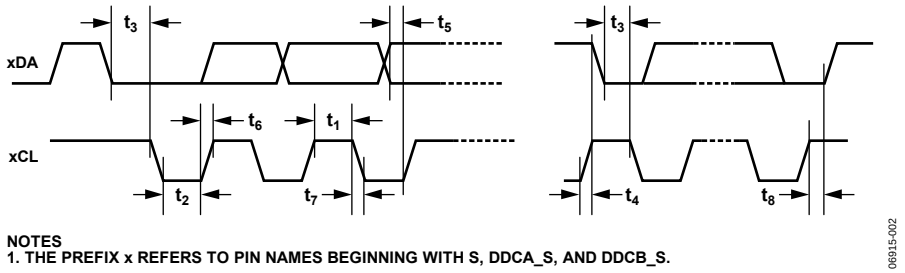
AVDD = 1.71 V to 1.89 V, DVDD = 1.62 V to 1.98 V, DVDDIO = 2.97 V to 3.63 V, PVDD = 1.71 V to 1.89 V, TVDD = 3.135 V to 3.465 V, CVDD = 1.71 V to 1.89 V. Operating temperature range is −40°C to +85°C, unless otherwise noted.

Table 3.

Parameter[1, 2]	Symbol	Test Conditions	Min	Typ	Max	Unit
SYSTEM CLOCK AND CRYSTAL						
Crystal Nominal Frequency				28.6363		MHz
Crystal Frequency Stability					±50	ppm
Horizontal Sync Input Frequency			14.8		110	kHz
LLC Frequency Range			12.825		170	MHz
I²C PORTS (FAST MODE)[3]						
xCL Frequency[4]					400	kHz
xCL Minimum Pulse Width High[4]	t_1		0.6			µs
xCL Minimum Pulse Width Low[4]	t_2		1.3			µs
Hold Time (Start Condition)	t_3		0.6			µs
Setup Time (Start Condition)	t_4		0.6			µs
xDA Setup Time[4]	t_5		100			ns
xCL and xDA Rise Times[4]	t_6				300	ns
xCL and xDA Fall Times[4]	t_7				300	ns
Setup Time (Stop Condition)	t_8		0.6			µs
I²C PORTS (NORMAL MODE)						
xCL Frequency[4]					100	kHz
xCL Minimum Pulse Width High[4]	t_1		4			µs
xCL Minimum Pulse Width Low[4]	t_2		4.7			µs
Hold Time (Start Condition)	t_3		4			µs
Setup Time (Start Condition)	t_4		4.7			µs
xDA Setup Time[4]	t_5		250			ns
xCL and xDA Rise Times[4]	t_6				1000	ns
xCL and xDA Fall Times[4]	t_7				300	ns
Setup Time (Stop Condition)	t_8		4			µs
RESET FEATURE						
Reset Pulse Width			5			ms
CLOCK OUTPUTS						
LLC Mark-Space Ratio	t_9:t_{10}		45:55		55:45	% duty cycle
DATA AND CONTROL OUTPUTS						
Data Output Transition Time SDR (CP)[5]	t_{11}	End of valid data to negative clock edge			2	ns
	t_{12}	Negative clock edge to start of valid data			0.5	ns
I²S PORT (MASTER MODE)						
SCLK Mark-Space Ratio	t_{13}:t_{14}		45:55		55:45	% duty cycle
LRCLK Data Transition Time	t_{15}	End of valid data to negative SCLK edge			10	ns
LRCLK Data Transition Time	t_{16}	Negative SCLK edge to start of valid data			10	ns
I2Sx Data Transition Time[6]	t_{17}	End of valid data to negative SCLK edge			5	ns
I2Sx Data Transition Time[6]	t_{18}	Negative SCLK edge to start of valid data			5	ns
MCLKOUT Frequency			4.096		24.576	MHz

[1] The minimum/maximum specifications are guaranteed over the −40°C to +85°C temperature range (T_{MIN} to T_{MAX}).
[2] Guaranteed by characterization.
[3] Refers to all I²C pins (DDC and control port).
[4] The prefix x refers to pin names beginning with S, DDCA_S, and DDCB_S.
[5] CP timing figures were obtained using the maximum drive strength value (0x3F) in User Map Register 0xF4.
[6] The suffix x refers to pin names ending with 0, 1, 2, and 3.

Timing Diagrams



NOTES
1. THE PREFIX x REFERS TO PIN NAMES BEGINNING WITH S, DDCA_S, AND DDCB_S.

Figure 2. I²C Timing

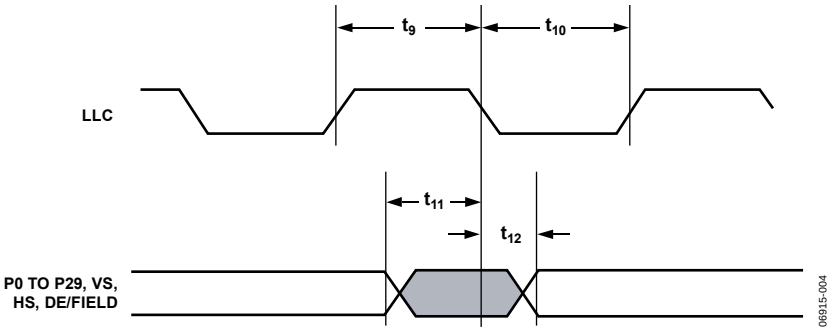
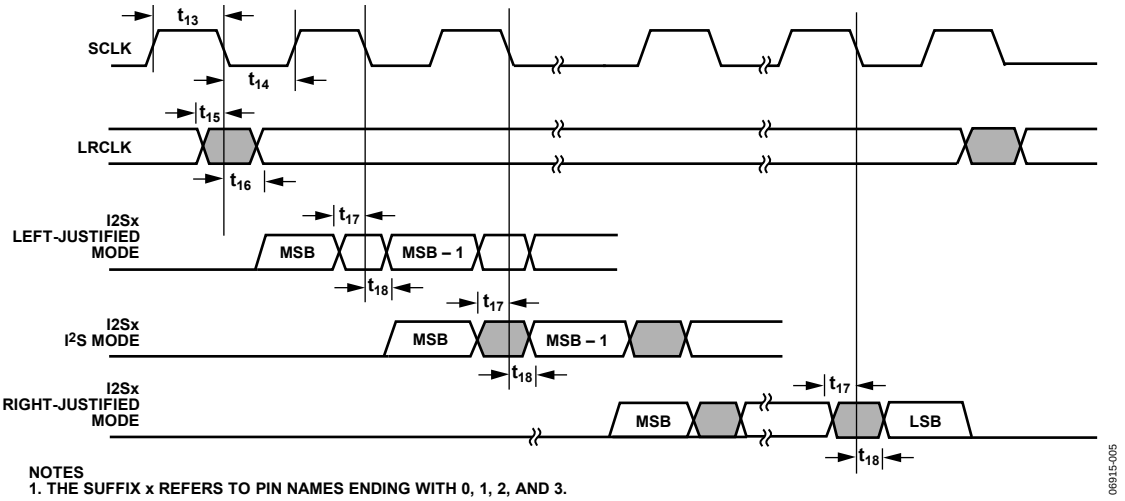


Figure 3. Pixel Port and Control CP Output Timing (CP Core)



NOTES
1. THE SUFFIX x REFERS TO PIN NAMES ENDING WITH 0, 1, 2, AND 3.

Figure 4. I²S Timing

ABSOLUTE MAXIMUM RATINGS

Table 4.

Parameter	Rating
AVDD to AGND	2.2 V
DVDD to DGND	2.2 V
PVDD to PGND	2.2 V
DVDDIO to DGND	4 V
CVDD to CGND	2.2 V
TVDD to TGND	4 V
DVDDIO to AVDD	−0.3 V to +3.6 V
DVDDIO to TVDD	−3.6 V to +3.6 V
DVDDIO to DVDD	−2 V to +2 V
CVDD to DVDD	−2 V to +0.3 V
PVDD to DVDD	−2 V to +0.3 V
AVDD to CVDD	−2 V to +2 V
AVDD to PVDD	−2 V to +2 V
AVDD to DVDD	−2 V to +2 V
AVDD to TVDD	−3.6 V to +0.3 V
TVDD to DVDD	−2 V to +2 V
Digital Inputs	
Voltage to DGND	DGND − 0.3 V to DVDDIO + 0.3 V
Digital Outputs	
Voltage to DGND	DGND − 0.3 V to DVDDIO + 0.3 V
Analog Inputs	
Voltage to AGND	AGND − 0.3 V to AVDD + 0.3 V
Maximum Junction Temperature (T_{J_MAX})	119°C
Storage Temperature Range	−65°C to +150°C
Infrared Reflow, Soldering (20 sec)	260°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

Table 5.

Package Type	Ψ_{JT}[1]	Unit
144-Lead LQFP (ST-144)	1.62	°C/W

[1] Junction-to-package surface thermal resistance.

PACKAGE THERMAL PERFORMANCE

To reduce power consumption during AD9388A operation, turn off unused ADCs.

On a 4-layer PCB that includes a solid ground plane, the θ_{JA} value is 25.3°C/W. However, due to variations within the PCB metal and, therefore, variations in PCB heat conductivity, the value of θ_{JA} may differ for various PCBs.

The most efficient measurement technique is to use the surface temperature of the package to estimate the die temperature because it is not affected by the variance associated with the θ_{JA} value.

The maximum junction temperature (T_{J_MAX}) of 119°C must not be exceeded. The following equation calculates the junction temperature using the measured surface temperature of the package and applies only when no heat sink is used on the device under test:

$$T_{J\_MAX} = T_S + (\Psi_{JT} \times W_{TOTAL})$$

where:
T_S is the surface temperature of the package expressed in degrees Celsius.
Ψ_{JT} is the junction-to-package surface thermal resistance.
$W_{TOTAL} = \{(AVDD \times I_{AVDD}) + (DVDD \times I_{DVDD}) + (DVDDIO \times I_{DVDDIO}) + (PVDD \times I_{PVDD}) + (CVDD \times I_{CVDD}) + (TVDD \times I_{TVDD})\}$

The AD9388A can be operated in ambient temperatures up to +85°C. However, in video modes where highest power is consumed and there is higher than nominal power supply voltages and worst-case video data, operation at these ambient temperatures may cause the junction temperature to exceed its maximum allowed value (119°C). One way to avoid this is to restrict the ambient temperature to be below +79°C. However, even if the ambient temperature is kept below +79°C, the user still needs to observe the thermally efficient PCB design recommendations outlined in this section to ensure that the maximum allowed junction temperature is not exceeded in any video mode.

Contact an Analog Devices, Inc., representative or field applications engineer (FAE) for more details on package thermal performance.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

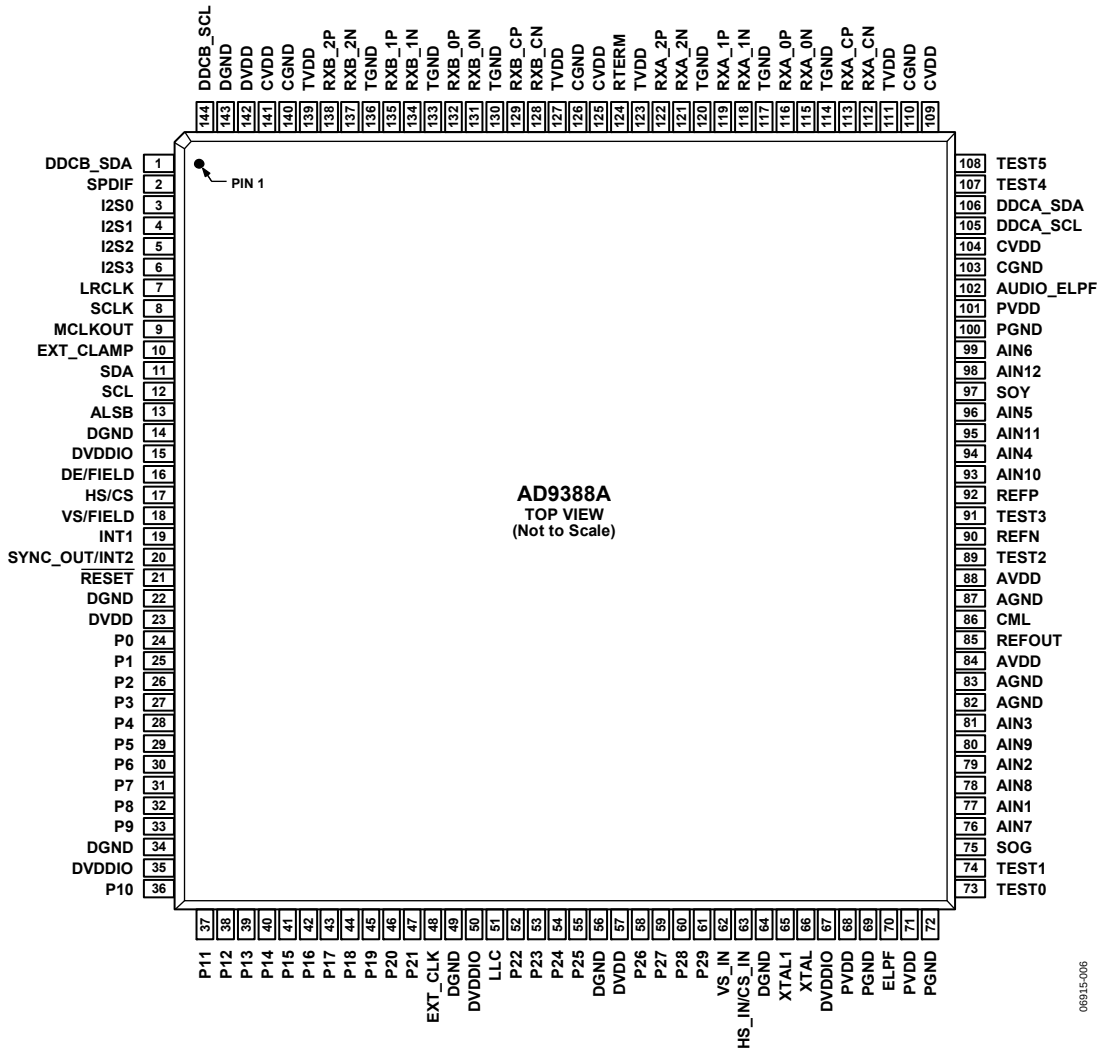


Figure 5. AD9388ABSTZ-170, AD9388ABSTZ-110, and AD9388ABSTZ-5P Pin Configuration

Table 6. Pin Function Descriptions

Pin No.	Mnemonic	Type[1]	Description
14, 22, 34, 49, 56, 64, 143	DGND	G	Digital Ground.
82, 83, 87	AGND	G	Analog Ground.
69, 72, 100	PGND	G	PLL Ground.
103, 110, 126, 140	CGND	G	Comparator Ground.
114, 117, 120, 130, 133, 136	TGND	G	Terminator Ground.
15, 35, 50, 67	DVDDIO	P	Digital I/O Supply Voltage (3.3 V).
23, 57, 142	DVDD	P	Digital Core Supply Voltage (1.8 V).
84, 88	AVDD	P	Analog Supply Voltage (1.8 V).
68, 71, 101	PVDD	P	Audio and Video PLL Supply Voltage (1.8 V).
104, 109, 125, 141	CVDD	P	HDMI Comparator, TMDS PLL, and Equalizer Supply Voltage (1.8 V).
111, 123, 127, 139	TVDD	P	Terminator Supply Voltage (3.3 V).
73, 74, 91, 108	TEST0, TEST1, TEST3, TEST5	I	Test Pins. Do not connect.
89	TEST2	O	Test Pin. Do not connect.
107	TEST4	I/O	Test Pin. Do not connect.
77, 79, 81, 94, 96, 99, 76, 78, 80, 93, 95, 98	AIN1 to AIN12	I	Analog Video Input Channels.

Pin No.	Mnemonic	Type[1]	Description
24 to 33, 36 to 47, 52 to 55, 58 to 61	P0 to P29	O	Video Pixel Output Port.
19	INT1	O	Interrupt. Can be active low or active high. The set of events that triggers an interrupt is under user control.
20	SYNC_OUT/INT2	O	Sliced Synchronization Output Signal (SYNC_OUT). Interrupt Signal (INT2).
17	HS/CS	O	Horizontal Synchronization Output Signal (HS). Composite Synchronization (CS). A single signal containing both horizontal and vertical synchronization pulses.
18	VS/FIELD	O	Vertical Synchronization Output Signal (VS). Field Synchronization (FIELD). Field synchronization output signal in all interlaced video modes.
16	DE/FIELD	O	Data Enable Signal (DE). Indicates active pixel data. Field Synchronization (FIELD). Field synchronization output signal in all interlaced video modes.
11	SDA	I/O	I^2C Port Serial Data Input/Output. SDA is the data line for the control port.
12	SCL	I	I^2C Port Serial Clock Input. (Maximum clock rate of 400 kHz.) SCL is the clock line for the control port.
13	ALSB	I	This pin sets the second LSB of each AD9388A register map.
21	$\overline{\text{RESET}}$	I	System Reset Input. Active low. A minimum low reset pulse width of 5 ms is required to reset the AD9388A circuitry.
51	LLC	O	Line-Locked Output Clock for Pixel Data. Range is 13.5 MHz to 170 MHz.
65	XTAL1	O	This pin should be connected to the 28.63636 MHz crystal or left as a no connect if an external 3.3 V, 28.63636 MHz clock oscillator source is used to clock the AD9388A. In crystal mode, the crystal must be a fundamental crystal.
66	XTAL	I	Input Pin for the 28.63636 MHz Crystal. This pin can be overdriven by an external 3.3 V, 28.63636 MHz clock oscillator source to clock the AD9388A.
70	ELPF	O	The recommended external loop filter must be connected to this ELPF pin.
102	AUDIO_ELPF	O	The recommended external loop filter must be connected to this AUDIO_ELPF pin.
85	REFOUT	O	Internal Voltage Reference Output.
86	CML	O	Common-Mode Level for the Internal ADCs.
90	REFN	I	Internal Voltage Output.
92	REFP	I	Internal Voltage Output.
63	HS_IN/CS_IN	I	HS Input Signal. Used in analog mode for 5-wire timing mode. CS Input Signal. Used in analog mode for 4-wire timing mode. For optimal performance, a 100 Ω series resistor is recommended on the HS_IN/CS_IN pin.
62	VS_IN	I	VS Input Signal. This pin is used in analog mode for 5-wire timing mode. For optimal performance, a 100 Ω series resistor is recommended on the VS_IN pin.
75	SOG	I	Synchronization-on-Green Input. This pin is used in embedded synchronization mode.
97	SOY	I	Synchronization-on-Luma Input. This pin is used in embedded synchronization mode.
112	RXA_CN	I	Digital Input Clock Complement of Port A in the HDMI Interface.
113	RXA_CP	I	Digital Input Clock True of Port A in the HDMI Interface.
115	RXA_0N	I	Digital Input Channel 0 Complement of Port A in the HDMI Interface.
116	RXA_0P	I	Digital Input Channel 0 True of Port A in the HDMI Interface.
118	RXA_1N	I	Digital Input Channel 1 Complement of Port A in the HDMI Interface.
119	RXA_1P	I	Digital Input Channel 1 True of Port A in the HDMI Interface.

Pin No.	Mnemonic	Type[1]	Description
121	RXA_2N	I	Digital Input Channel 2 Complement of Port A in the HDMI Interface.
122	RXA_2P	I	Digital Input Channel 2 True of Port A in the HDMI Interface.
128	RXB_CN	I	Digital Input Clock Complement of Port B in the HDMI Interface.
129	RXB_CP	I	Digital Input Clock True of Port B in the HDMI Interface.
131	RXB_0N	I	Digital Input Channel 0 Complement of Port B in the HDMI Interface.
132	RXB_0P	I	Digital Input Channel 0 True of Port B in the HDMI Interface.
134	RXB_1N	I	Digital Input Channel 1 Complement of Port B in the HDMI Interface.
135	RXB_1P	I	Digital Input Channel 1 True of Port B in the HDMI Interface.
137	RXB_2N	I	Digital Input Channel 2 Complement of Port B in the HDMI Interface.
138	RXB_2P	I	Digital Input Channel 2 True of Port B in the HDMI Interface.
106	DDCA_SDA	I/O	HDCP Slave Serial Data Port A.
1	DDCB_SDA	I/O	HDCP Slave Serial Data Port B.
105	DDCA_SCL	I	HDCP Slave Serial Clock Port A.
144	DDCB_SCL	I	HDCP Slave Serial Clock Port B.
2	SPDIF	O	SPDIF Digital Audio Output.
3	I2S0	O	I^2S Audio for Channel 1 and Channel 2.
4	I2S1	O	I^2S Audio for Channel 3 and Channel 4.
5	I2S2	O	I^2S Audio for Channel 5 and Channel 6.
6	I2S3	O	I^2S Audio for Channel 7 and Channel 8.
7	LRCLK	O	Data Output Clock for Left and Right Audio Channels.
8	SCLK	O	Audio Serial Clock Output.
9	MCLKOUT	O	Audio Master Clock Output.
10	EXT_CLAMP	I	External Clamp Signal. This is an optional mode of operation for the AD9388A.
48	EXT_CLK	I	Clock Input for External Clock and Clamp Mode. This is an optional mode of operation for the AD9388A.
124	RTERM	I	Sets Internal Termination Resistance. Connect this pin to TGND using a 500 Ω resistor.

[1] G = ground, P = power, I = input, and O = output.

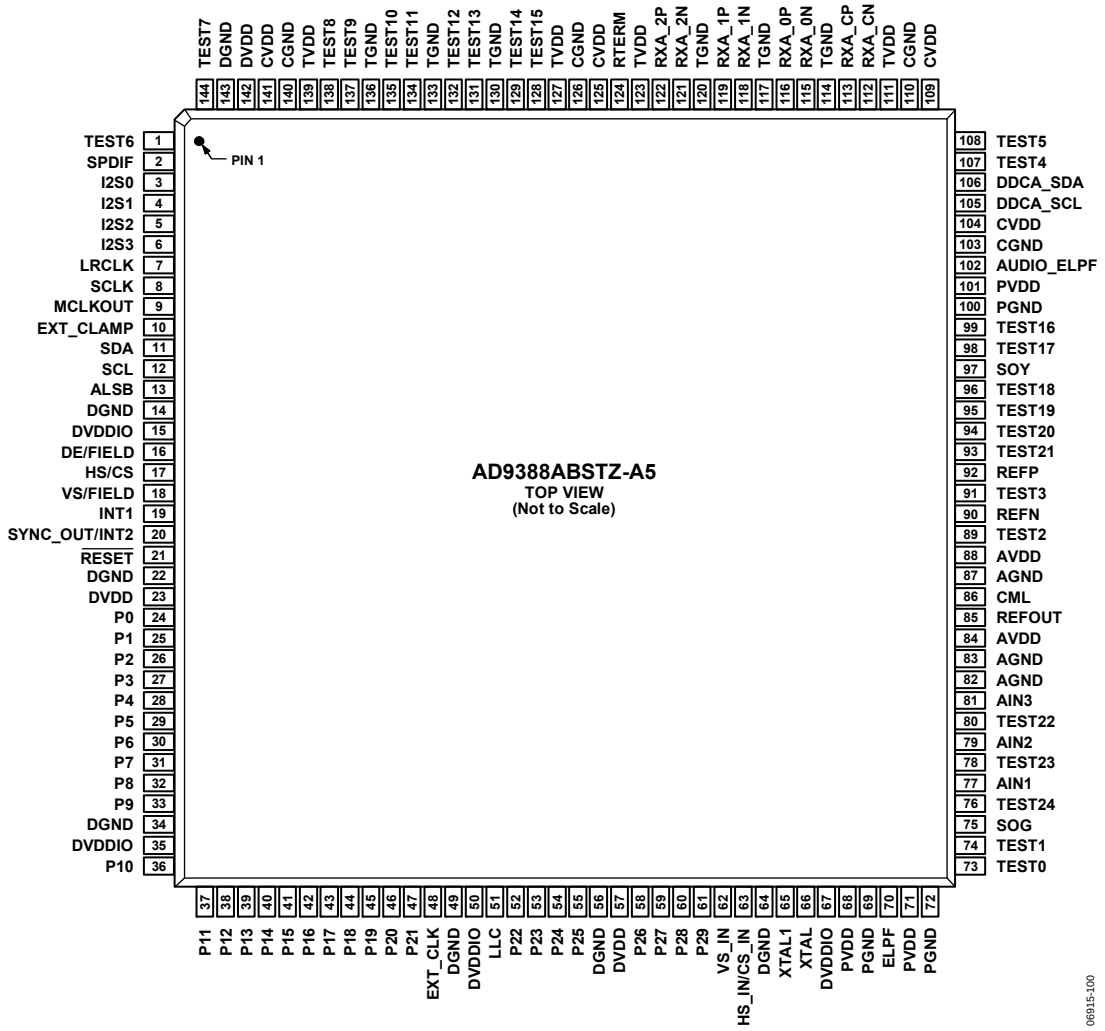


Figure 6. AD9388ABSTZ-A5 Pin Configuration

Table 7. Pin Function Descriptions

Pin No.	Mnemonic	Type[1]	Description
14, 22, 34, 49, 56, 64, 143	DGND	G	Digital Ground.
82, 83, 87	AGND	G	Analog Ground.
69, 72, 100	PGND	G	PLL Ground.
103, 110, 126, 140	CGND	G	Comparator Ground.
114, 117, 120, 130, 133, 136	TGND	G	Terminator Ground.
15, 35, 50, 67	DVDDIO	P	Digital I/O Supply Voltage (3.3 V).
23, 57, 142	DVDD	P	Digital Core Supply Voltage (1.8 V).
84, 88	AVDD	P	Analog Supply Voltage (1.8 V).
68, 71, 101	PVDD	P	Audio and Video PLL Supply Voltage (1.8 V).
104, 109, 125, 141	CVDD	P	HDMI Comparator, TMDS PLL, and Equalizer Supply Voltage (1.8 V).
111, 123, 127, 139	TVDD	P	Terminator Supply Voltage (3.3 V).
128, 129, 131, 132, 134, 135, 137, 138, 108, 91, 74, 73	TEST15 to TEST8, TEST5, TEST3, TEST1, TEST0	I	Test Pins. Do not connect.
76, 78, 80, 93 to 96, 98, 99	Test24 to Test16	I	Test Pins. Connect to AGND through a 10 kΩ resistor.
89	TEST2	O	Test Pin. Do not connect.
107	TEST4	I/O	Test Pin. Do not connect.
77, 79, 81	AIN1 to AIN3	I	Analog Video Input Channels.

Pin No.	Mnemonic	Type[1]	Description
24 to 33, 36 to 47, 52 to 55, 58 to 61	P0 to P29	O	Video Pixel Output Port.
19	INT1	O	Interrupt. Can be active low or active high. The set of events that triggers an interrupt is under user control.
20	SYNC_OUT/INT2	O	Sliced Synchronization Output Signal (SYNC_OUT). Interrupt Signal (INT2).
17	HS/CS	O	Horizontal Synchronization Output Signal (HS). Composite Synchronization (CS). A single signal containing both horizontal and vertical synchronization pulses.
18	VS/FIELD	O	Vertical Synchronization Output Signal (VS). Field Synchronization (FIELD). Field synchronization output signal in all interlaced video modes.
16	DE/FIELD	O	Data Enable Signal (DE). Indicates active pixel data. Field Synchronization (FIELD). Field synchronization output signal in all interlaced video modes.
11	SDA	I/O	I^2C Port Serial Data Input/Output. SDA is the data line for the control port.
12	SCL	I	I^2C Port Serial Clock Input. (Maximum clock rate of 400 kHz.) SCL is the clock line for the control port.
13	ALSB	I	This pin sets the second LSB of each AD9388A register map.
21	$\overline{\text{RESET}}$	I	System Reset Input. Active low. A minimum low reset pulse width of 5 ms is required to reset the AD9388A circuitry.
51	LLC	O	Line-Locked Output Clock for Pixel Data. Range is 13.5 MHz to 170 MHz.
65	XTAL1	O	This pin should be connected to the 28.63636 MHz crystal or left as a no connect if an external 3.3 V, 28.63636 MHz clock oscillator source is used to clock the AD9388A. In crystal mode, the crystal must be a fundamental crystal.
66	XTAL	I	Input Pin for the 28.63636 MHz Crystal. This pin can be overdriven by an external 3.3 V, 28.63636 MHz clock oscillator source to clock the AD9388A.
70	ELPF	O	The recommended external loop filter must be connected to this ELPF pin.
102	AUDIO_ELPF	O	The recommended external loop filter must be connected to AUDIO_ELPF.
85	REFOUT	O	Internal Voltage Reference Output.
86	CML	O	Common-Mode Level for the Internal ADCs.
90	REFN	I	Internal Voltage Output.
92	REFP	I	Internal Voltage Output.
63	HS_IN/CS_IN	I	HS Input Signal. Used in analog mode for 5-wire timing mode. CS Input Signal. Used in analog mode for 4-wire timing mode. For optimal performance, a 100 Ω series resistor is recommended on the HS_IN/CS_IN pin.
62	VS_IN	I	VS Input Signal. This pin is used in analog mode for 5-wire timing mode. For optimal performance, a 100 Ω series resistor is recommended on the VS_IN pin.
75	SOG	I	Synchronization-on-Green Input. This pin is used in embedded synchronization mode.
97	SOY	I	Synchronization-on-Luma Input. This pin is used in embedded synchronization mode.
112	RXA_CN	I	Digital Input Clock Complement of Port A in the HDMI Interface.
113	RXA_CP	I	Digital Input Clock True of Port A in the HDMI Interface.
115	RXA_0N	I	Digital Input Channel 0 Complement of Port A in the HDMI Interface.
116	RXA_0P	I	Digital Input Channel 0 True of Port A in the HDMI Interface.
118	RXA_1N	I	Digital Input Channel 1 Complement of Port A in the HDMI Interface.
119	RXA_1P	I	Digital Input Channel 1 True of Port A in the HDMI Interface.
121	RXA_2N	I	Digital Input Channel 2 Complement of Port A in the HDMI Interface.
122	RXA_2P	I	Digital Input Channel 2 True of Port A in the HDMI Interface.
106	DDCA_SDA	I/O	HDCP Slave Serial Data Port A.
1	TEST6	I/O	Test Pin. Do not connect.
105	DDCA_SCL	I	HDCP Slave Serial Clock Port A.
144	TEST7	I	Test Pin. Connect this pin to DGND using a 10 kΩ resistor.

Pin No.	Mnemonic	Type [1]	Description
2	SPDIF	O	SPDIF Digital Audio Output.
3	I2S0	O	I^2S Audio for Channel 1 and Channel 2.
4	I2S1	O	I^2S Audio for Channel 3 and Channel 4.
5	I2S2	O	I^2S Audio for Channel 5 and Channel 6.
6	I2S3	O	I^2S Audio for Channel 7 and Channel 8.
7	LRCLK	O	Data Output Clock for Left and Right Audio Channels.
8	SCLK	O	Audio Serial Clock Output.
9	MCLKOUT	O	Audio Master Clock Output.
10	EXT_CLAMP	I	External Clamp Signal. This is an optional mode of operation for the AD9388A.
48	EXT_CLK	I	Clock Input for External Clock and Clamp Mode. This is an optional mode of operation for the AD9388A.
124	RTERM	I	Sets Internal Termination Resistance. Connect this pin to TGND using a 500 Ω resistor.

[1] G = ground, P = power, I = input, and O = output.

FUNCTIONAL OVERVIEW

The following overview provides a brief description of the functionality of the AD9388A. More details are available in the Theory of Operation section.

ANALOG FRONT END

The analog front end of the AD9388A provides three high quality 10-bit ADCs to enable true 10-bit video decoding, a multiplexer with 12 analog input channels to enable a multisource connection without the requirement of an external multiplexer, and three current and voltage clamp control loops to ensure that dc offsets are removed from the video signal.

HDMI RECEIVER

The AD9388A is compatible with the HDMI specification. The AD9388A supports all HDTV formats up to 1080p in non–Deep Color mode and 1080p in 36-bit Deep Color mode. Furthermore, it supports all display resolutions up to UXGA (1600 × 1200 at 60 Hz).

This device includes the following features:

- Adaptive front-end equalization for HDMI operation over cable lengths of up to 30 meters
- Synchronization conditioning for higher performance in strenuous conditions
- Audio mute for removing extraneous noises
- Programmable data island packet interrupt generator

COMPONENT PROCESSOR PIXEL DATA OUTPUT MODES

The AD9388A features single data rate outputs as follows:

- 8-/10-bit 4:2:2 YCrCb for 525i, 625i
- 16-/20-bit 4:2:2 YCrCb for all standards
- 24-/30-bit 4:4:4 YCrCb/RGB for all standards

COMPONENT VIDEO PROCESSING

The AD9388A supports 525i, 625i, 525p, 625p, 720p, 1080i, 1080p, and many other HDTV formats. It provides automatic adjustment of gain (contrast) and offset (brightness), as well as manual adjustment controls. Furthermore, the AD9388A not only supports analog component YPrPb/RGB video formats with embedded synchronization or with separate HS, VS, and CS, but also supports YCrCb-to-RGB and RGB-to-YCrCb conversions by any-to-any, 3 × 3 color-space conversion matrices and user-defined pixel sampling for nonstandard video sources.

In addition, the AD9388A features brightness, saturation, and hue controls. Standard identification (STDI) enables detection of the component format at the system level, and a synchronization source polarity detector (SSPD) determines the source and polarity of the synchronization signals that accompany the input video.

Certified Macrovision® copy protection detection is available on component formats (525i, 625i, 525p, and 625p).

When no video input is present, stable timing is provided by the free run output mode.

RGB GRAPHICS PROCESSING

The AD9388A provides 170 MSPS conversion rate support of RGB input resolutions up to 1600 × 1200 at 60 Hz (UXGA).

The AD9388A offers automatic or manual clamp and gain controls for graphics modes.

Similar to the component video processing features, the RGB graphics processing for the AD9388A features contrast and brightness controls, automatic detection of synchronization source and polarity by the SSPD block, standard identification enabled by the STDI block, and user-defined pixel sampling support for nonstandard video sources.

Additional RGB graphics processing features of the AD9388A include the following:

- Sampling PLL clock with 500 ps p-p jitter at 150 MSPS
- 32-phase DLL support of optimum pixel clock sampling
- Color-space conversion of RGB to YCrCb and decimation to a 4:2:2 format for videocentric, back-end IC interfacing
- Data enable (DE) output signal supplied for direct connection to HDMI/DVI transmitter IC

GENERAL FEATURES

The AD9388A offers a high quality multiformat video decoder and digitizer that feature HS, VS, and FIELD output signals with programmable position, polarity, and width. It also includes programmable interrupt request output pins (INT1 and INT2).

The part offers low power consumption—1.8 V digital core and analog input, and 3.3 V digital input/output—and a low power power-down mode.

The AD9388A operates over a temperature range of −40°C to +85°C and is available in a 144-lead, 20 mm × 20 mm, RoHS-compliant LQFP.

THEORY OF OPERATION

ANALOG FRONT END

The AD9388A analog front end comprises three 10-bit ADCs that digitize the analog video signal before applying it to the CP. The analog front end uses differential channels to each ADC to ensure high performance in mixed-signal applications.

The front end also includes a 12-channel input multiplexer that enables multiple video signals to be applied to the AD9388A. Current and voltage clamps are positioned in front of each ADC to ensure that the video signal remains within the range of the converter. Fine clamping of the video signals is performed downstream by digital fine clamping in the CP.

For component 525i, 625i, 525p, and 625p sources, 2× oversampling is performed, but 4× oversampling is available for component 525i and 625i. All other video standards are 1× oversampled. Oversampling the video signals reduces the cost and complexity of external antialiasing (AA) filters, with the additional benefit of increasing the signal-to-noise ratio (SNR).

HDMI RECEIVER

The HDMI receiver on the AD9388A incorporates active equalization of the HDMI data signals. This equalization compensates for the high frequency losses inherent in HDMI and DVI cables, especially those with long lengths and high frequencies. Because the AD9338A can provide equalization compensation for cable lengths up to 30 meters, it is capable of achieving robust receiver performance at even the highest HDMI data rates.

With the inclusion of HDCP, displays can receive encrypted video content. The HDMI interface of the AD9388A allows for authentication of a video receiver, decryption of encoded data at the receiver, and renewability of that authentication during transmission as specified by the HDCP 1.3 protocol.

The HDMI receiver also offers advanced audio functionality. The receiver contains an audio mute controller that can detect a variety of selectable conditions that may result in audible extraneous noise in the audio output. Upon detection of these conditions, the audio data can be ramped to prevent audio clicks and pops.

COMPONENT PROCESSOR (CP)

The CP is capable of decoding and digitizing a wide range of component video formats in any color space. Component video standards supported by the CP include 525i, 625i, 525p, 625p, 720p, 1080i, 1080p, 1250i, VGA up to UXGA at 60 Hz, and many other standards.

The CP section of the AD9388A contains an AGC block. This block is followed by a digital clamp circuit that ensures that the video signal is clamped to the correct blanking level. Automatic adjustments within the CP include gain (contrast) and offset (brightness); however, manual adjustment controls are also supported. If no embedded synchronization is present, the video gain can be set manually.

A fully programmable, any-to-any, 3 × 3 color-space converter is placed before the CP section. This enables YPrPb-to-RGB and RGB-to-YCrCb conversions. Many other standards of color space can be implemented using the color-space converter.

A second fully programmable, any-to-any, 3 × 3 color-space converter is placed in the back end of the CP core. This color-space converter features advanced color controls, such as contrast, saturation, brightness, and hue controls.

The output section of the CP can be configured in single data rate (SDR) mode with one data packet per clock cycle. In SDR mode, a 16-/20-bit 4:2:2 or 24-/30-bit 4:4:4 output is possible. In these modes, HS/CS, VS/FIELD, and DE/FIELD (where applicable) timing reference signals are provided.

The CP section contains circuitry to enable the detection of Macrovision-encoded YPrPb signals for 525i, 625i, 525p, and 625p. It is designed to be fully robust when decoding these types of signals.

VBI DATA PROCESSOR

VBI extraction of CGMS data is performed by the VBI data processor (VDP) section of the AD9388A for interlaced, progressive, and high definition scanning rates. The data extracted is read back over the I^2C interface.

For more detailed product information about the AD9388A, contact a local Analog Devices sales representative or field applications engineer (FAE).

PIXEL OUTPUT FORMATTING

Note that unused pins of the pixel output port are driven with a low voltage.

Table 8. Component Processor Pixel Output Pin Map (P19 to P0)

Processor[1]	Mode	Format	Output of Data Port Pins P[19:0]																			
			19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CP	Mode 1	Video output 8-bit 4:2:2[2]	YCrCb[7:0]																			
CP	Mode 2	Video output 10-bit 4:2:2[2]	YCrCb[9:0]																			
CP	Mode 3	Video output 12-bit 4:2:2[2]	YCrCb[11:2]																			
CP	Mode 4	Video output 12-bit 4:2:2[2]	YCrCb[11:4]																			
CP	Mode 5	Video output 12-bit 4:2:2[2]	YCrCb[11:4]										YCrCb[3:0]									
CP	Mode 6	Video output 16-bit 4:2:2[3, 4]	CHA[7:0] (default data is Y[7:0])										CHB/CHC[7:0] (default data is Cr/Cb[7:0])									
CP	Mode 7	Video output 20-bit 4:2:2[3, 4]	CHA[9:0] (default data is Y[9:0])										CHB/CHC[9:0] (default data is Cr/Cb[9:0])									
CP	Mode 8	Video output 20-bit 4:2:2[3, 4]	CHA[9:2] (default data is Y[9:2])										CHB/CHC[9:2] (default data is Cr/Cb[9:2])									
CP	Mode 9	Video output 24-bit 4:2:2[3, 4]	Y[11:2]										CrCb[11:2]									
CP	Mode 10	Video output 24-bit 4:2:2[3, 4]	Y[11:4]										CrCb[11:4]									
CP	Mode 11	Video output 24-bit 4:2:2[3, 4]	Y[11:4]										Y[3:0]				CrCb[3:0]					
CP	Mode 12	Video output 24-bit 4:4:4[3, 4]	CHA[7:0] (default data is G[7:0] or Y[7:0])										CHB[7:0] (default data is R[7:0] or Cr[7:0])									
CP	Mode 13	Video output 24-bit 4:4:4[3, 4]	CHA[7:0] (default data is G[7:0] or Y[7:0])										CHC[7:0] (default data is B[7:0] or Cb[7:0])									
CP	Mode 14	Video output 24-bit 4:4:4[3, 4]	CHC[7:0] (default data is B[7:0] or Cb[7:0])										CHA[7:0] (default data is G[7:0] or Y[7:0])									
CP	Mode 15	Video output 24-bit 4:4:4[3, 4]	CHC[7:0] (default data is B[7:0] or Cb[7:0])										CHB[7:0] (default data is R[7:0] or Cr[7:0])									
CP	Mode 16	Video output 30-bit 4:4:4[3, 4]	CHA[9:0] (default data is G[9:0] or Y[9:0])										CHB[9:0] (default data is R[9:0] or Cr[9:0])									
CP	Mode 17	Video output 30-bit 4:4:4	CHA[9:0] (default data is G[9:0] or Y[9:0])										CHC[9:0] (default data is B[9:0] or Cb[9:0])									
CP	Mode 18	Video output 30-bit 4:4:4	CHC[9:0] (default data is B[9:0] or Cb[9:0])										CHA[9:0] (default data is G[9:0] or Y[9:0])									
CP	Mode 19	Video output 30-bit 4:2:2	CHC[9:0] (default data is B[9:0] or Cb[9:0])										CHB[9:0] (default data is R[9:0] or Cr[9:0])									

[1] The CP processor uses the digitizer or HDMI as input.
[2] Maximum pixel clock rate of 54 MHz.
[3] Maximum pixel clock rate of 170 MHz for the analog digitizer.
[4] Maximum pixel clock rate of 165 MHz for HDMI.

Table 9. Component Processor Pixel Output Pin Map (P29 to P20)

Processor [1]	Mode	Format	Output of Data Port Pins P[29:20]									
			29	28	27	26	25	24	23	22	21	20
CP	Mode 1	Video output 8-bit 4:2:2 [2]										
CP	Mode 2	Video output 10-bit 4:2:2[2]										
CP	Mode 3	Video output 12-bit 4:2:2[2]							YCrCb[1:0]			
CP	Mode 4	Video output 12-bit 4:2:2 [2]					YCrCb[3:0]					
CP	Mode 5	Video output 12-bit 4:2:2 [2]										
CP	Mode 6	Video output 16-bit 4:2:2 [3, 4]										
CP	Mode 7	Video output 20-bit 4:2:2[3, 4]										
CP	Mode 8	Video output 20-bit 4:2:2[3, 4]	Y[1:0]		CrCb[1:0]							
CP	Mode 9	Video output 24-bit 4:2:2 [3, 4]			CrCb[1:0]				Y[1:0]			
CP	Mode 10	Video output 24-bit 4:2:2[3, 4]	CrCb[3:0]				Y[3:0]					
CP	Mode 11	Video output 24-bit 4:2:2[3, 4]	CrCb[11:4]									
CP	Mode 12	Video output 24-bit 4:4:4[3, 4]	CHC[7:0] (for example, B[7:0] or Cb[7:0])									
CP	Mode 13	Video output 24-bit 4:4:4[3, 4]	CHB[7:0] (for example, R[7:0] or Cr[7:0])									
CP	Mode 14	Video output 24-bit 4:4:4[3, 4]	CHB[7:0] (for example, R[7:0] or Cr[7:0])									
CP	Mode 15	Video output 24-bit 4:4:4[3, 4]	CHA[7:0] (for example, G[7:0] or Y[7:0])									
CP	Mode 16	Video output 30-bit 4:4:4[3, 4]	CHC[9:0] (for example, B[9:0] or Cb[9:0])									
CP	Mode 17	Video output 30-bit 4:4:4[3, 4]	CHB[9:0] (for example, R[9:0] or Cr[9:0])									
CP	Mode 18	Video output 30-bit 4:4:4[3, 4]	CHB[9:0] (for example, R[9:0] or Cr[9:0])									
CP	Mode 19	Video output 30-bit 4:2:2[3, 4]	CHA[9:0] (for example, G[9:0] or Y[9:0])									

[1] The CP processor uses the digitizer or HDMI as input.
[2] Maximum pixel clock rate of 54 MHz.
[3] Maximum pixel clock rate of 170 MHz for the analog digitizer.
[4] Maximum pixel clock rate of 165 MHz for HDMI.

REGISTER MAP ARCHITECTURE

The AD9388A registers are controlled via a 2-wire serial (I^2C-compatible) interface. The AD9388A has eight maps, each with a unique I^2C address. The state of the ALSB pin (Pin 13) sets Bit 2 of each register map address in Table 10.

Table 10. AD9388A Map Addresses

Register Map	Address with ALSB = Low	Address with ALSB = High	Programmable Address	Location at Which Address Can Be Programmed
User Map	0x40	0x42	Not programmable	N/A
User Map 1	0x44	0x46	Programmable	User Map 2, Register 0xEB
User Map 2	0x60	0x62	Programmable	User Map, Register 0x0E
VDP Map	0x48	0x4A	Programmable	User Map 2, Register 0xEC
Reserved Map	0x4C	0x4E	Programmable	User Map 2, Register 0xEA
HDMI Map	0x68	0x6A	Programmable	User Map 2, Register 0xEF
Repeater/KSV Map	0x64	0x66	Programmable	User Map 2, Register 0xED
EDID Map	0x6C	0x6E	Programmable	User Map 2, Register 0xEE

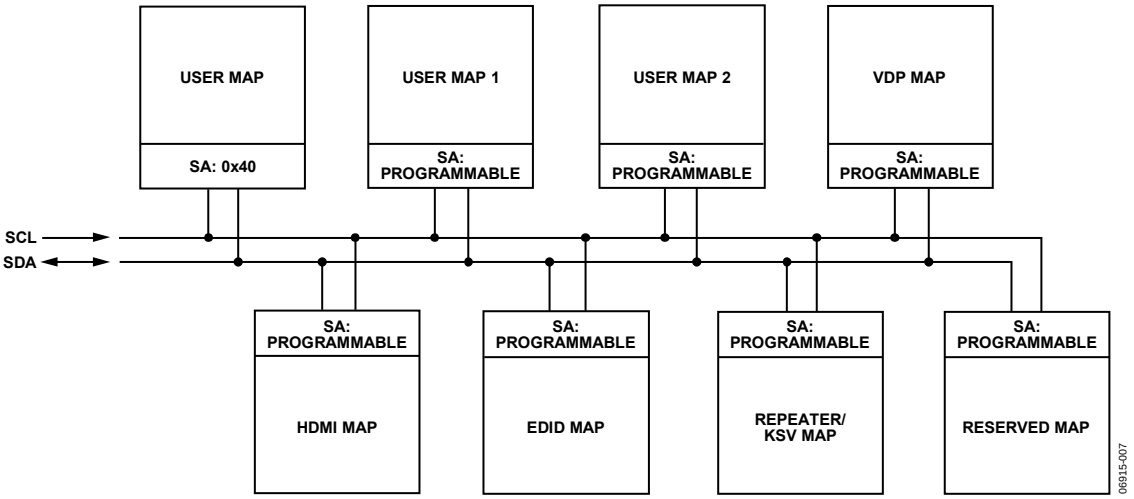


Figure 7. Register Map Access Through the Main I^2C Port

TYPICAL CONNECTION DIAGRAM

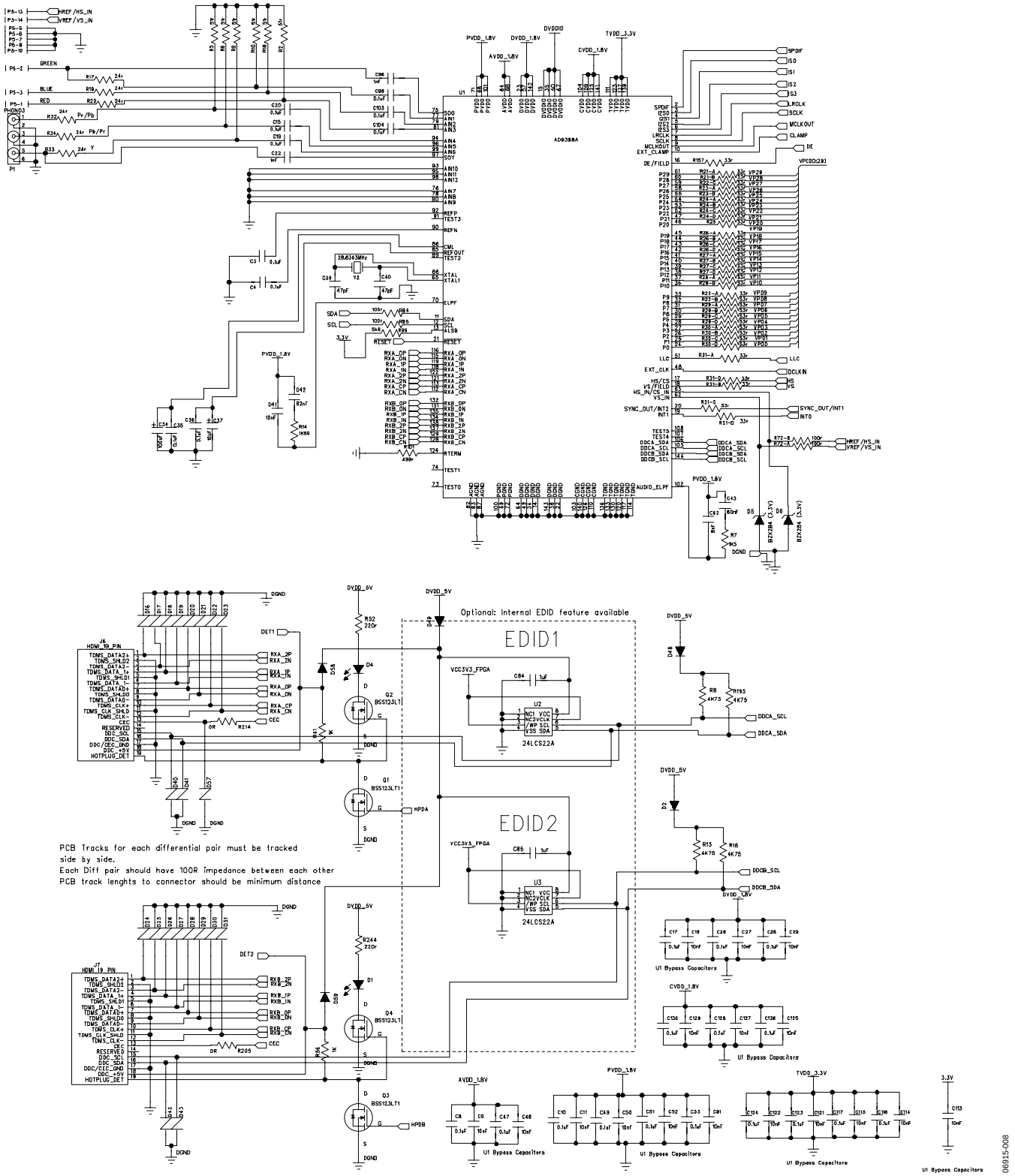


Figure 8. Typical Connection Diagram

RECOMMENDED EXTERNAL LOOP FILTER COMPONENTS

Note that the external loop filter components for the ELPF and AUDIO_ELPF pins should be placed as close as possible to the respective pins. The recommended component values are specified in Figure 9 and Figure 10.

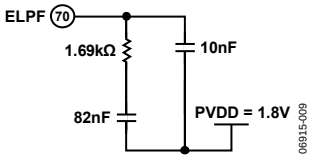


Figure 9. ELPF Components

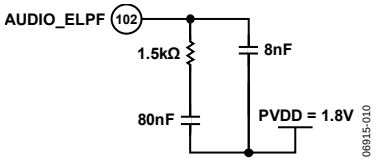


Figure 10. AUDIO_ELPF Components

AD9388A EVALUATION PLATFORM

Analog Devices has developed an advanced TV (ATV) evaluation platform for the AD9388A decoder. The evaluation platform consists of a motherboard and two daughterboards. The motherboard features a Xilinx FPGA for digital processing and muxing functions. The motherboard also features three AD9742 devices (12-bit DACs) from Analog Devices. This allows the user to drive a VGA monitor with just the motherboard and front-end board.

The back end of the platform can be connected to a specially developed video output board from Analog Devices. This modular board features an Analog Devices encoder and an Analog Devices HDMI transmitter.

The front end of the platform consists of an AD9388A evaluation board (EVAL-AD9388AFEZ_x). This board feeds the digital outputs from the decoder to the FPGA on the motherboard. The evaluation board comes with one of the pin-compatible decoders listed in Table 11.

Table 11. Front-End Modular Board Details

Front-End Modular Board Model	On-Board Decoder	HDCP License Required
EVAL-AD9388AFEZ_1	AD9388ABSTZ-170	Yes
EVAL-AD9388AFEZ_2	AD9388ABSTZ-5P	No
EVAL-AD9388AFEZ_3	AD9388ABSTZ-A5	Yes

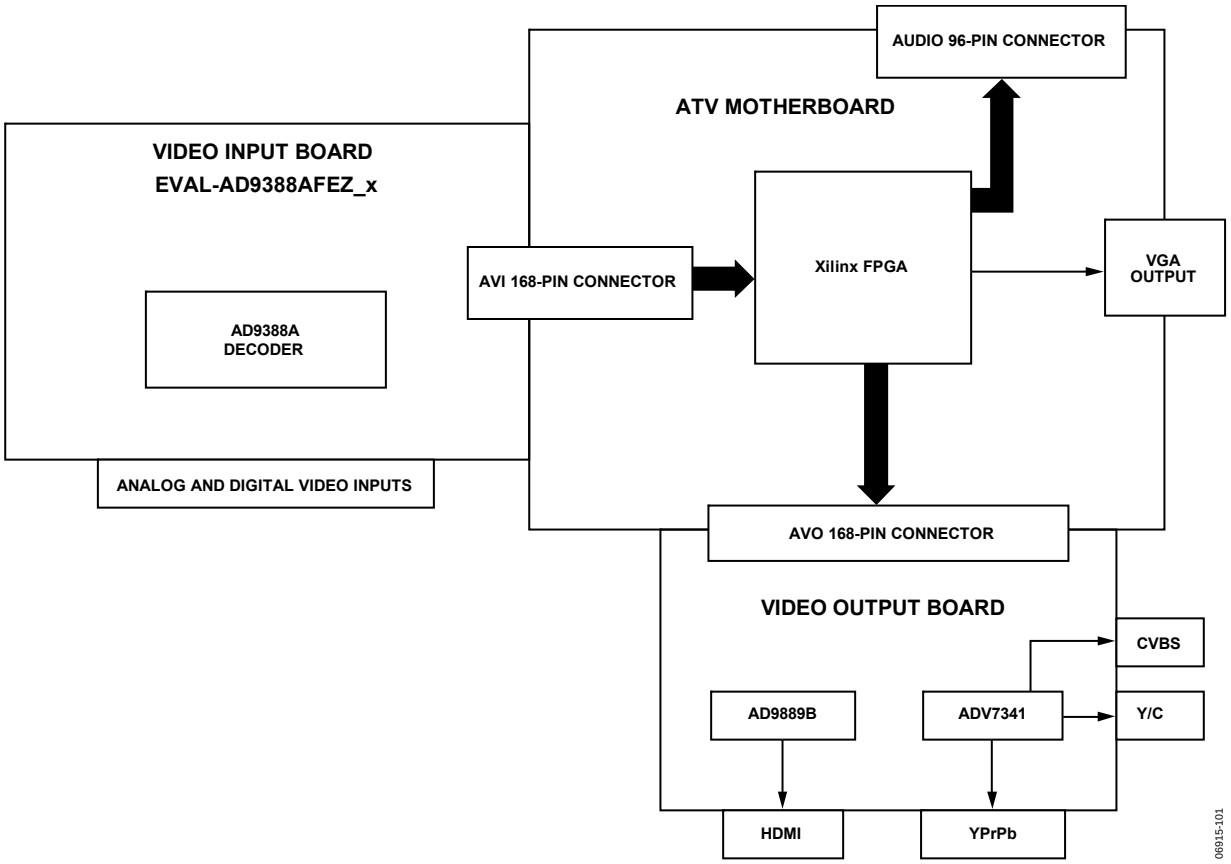
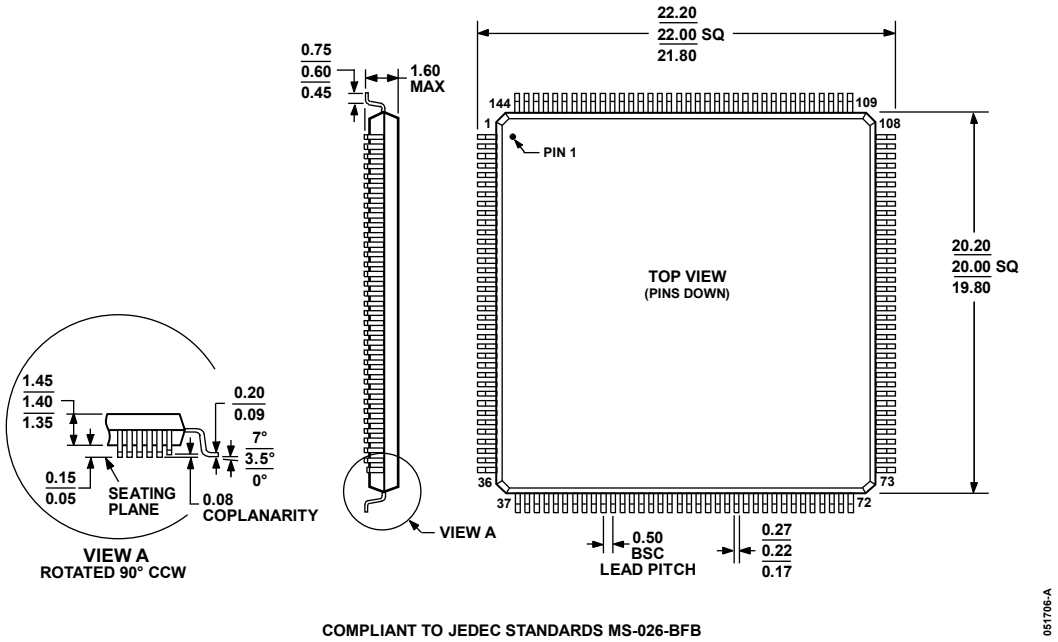


Figure 11. Functional Block Diagram of Evaluation Platform

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MS-026-BFB

Figure 12. 144-Lead Low Profile Quad Flat Package [LQFP]
(ST-144)
Dimensions shown in millimeters

ORDERING GUIDE

Model [1, 2, 3, 4, 5]	Temperature Range	Package Description	Package Option
AD9388ABSTZ-170	–40°C to +85°C	144-Lead Low Profile Quad Flat Package [LQFP]	ST-144
AD9388ABSTZ-110	–40°C to +85°C	144-Lead Low Profile Quad Flat Package [LQFP]	ST-144
AD9388ABSTZ-5P	–40°C to +85°C	144-Lead Low Profile Quad Flat Package [LQFP]	ST-144
AD9388ABSTZ-A5	–40°C to +85°C	144-Lead Low Profile Quad Flat Package [LQFP]	ST-144

[1] Z = RoHS Compliant Part.
[2] The AD9388ABSTZ-170, AD9388ABSTZ-110, and AD9833ABSTZ-A5 are programmed with internal HDCP keys. Customers must have HDCP adopter status (consult Digital Content Protection, LLC, for licensing requirements) to purchase any components with internal HDCP keys.
[3] The AD9388ABSTZ-5P speed grade: 5 = 170 MHz; HDCP functionality: P = no HDCP functionality (professional version).
[4] The AD9388ABSTZ-5P professional version for non-HDCP encrypted applications. User is not required to be an HDCP adopter.
[5] The AD9388ABSTZ-A5 speed grade: 5 = 170 MHz; input configuration: A = 1 analog (AIN1, AIN2, AIN3, HS_IN/CS_IN, VS_IN, SOG, and SOY), 1 digital (1 HDMI port).

I²C refers to a communications protocol originally developed by Phillips Semiconductors (now NXP Semiconductors).

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D06915-0-10/10(F)