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DC SPECIFICATIONS

AVDD = 3 V, DRVDD = 2.5 V, sample rate = 80 MSPS, 2 V p-p differential input, 1.0 V external reference, unless otherwise noted.

Table 1.

			AD9236BRU/AD9236BCP			
Parameter	**Temp**	**Test Level**	**Min**	**Typ**	**Max**	**Unit**
RESOLUTION	Full	VI	12			Bits
ACCURACY						
No Missing Codes	Full	VI		Guaranteed		
Offset Error[1]	Full	VI		±0.30	±1.30	% FSR
Gain Error	25°C	V		±0.10		% FSR
Gain Error[1]	Full	VI		±0.30	±4.34	% FSR
Differential Nonlinearity (DNL)[2]	Full	VI		±0.40	±0.65	LSB
Integral Nonlinearity (INL)[2]	Full	VI		±0.35	±1.20	LSB
TEMPERATURE DRIFT						
Offset Error[1]	Full	V		±6		ppm/°C
Gain Error	Full	V		±12		ppm/°C
Gain Error[1]	Full	V		±18		ppm/°C
INTERNAL VOLTAGE REFERENCE						
Output Voltage Error (1 V)	Full	VI		±2	±35	mV
Load Regulation @ 1.0 mA	25°C	V		0.8		mV
Output Voltage Error (0.5 V)	25°C	V		±1		mV
Load Regulation @ 0.5 mA	25°C	V		0.1		mV
INPUT REFERRED NOISE						
VREF = 0.5 V	25°C	V		0.55		LSB rms
VREF = 1.0 V	25°C	V		0.28		LSB rms
ANALOG INPUT						
Input Span, VREF = 0.5 V	Full	IV		1		V p-p
Input Span, VREF = 1.0 V	Full	IV		2		V p-p
Input Capacitance[3]	Full	V		7		pF
REFERENCE INPUT RESISTANCE	Full	V		7		kΩ
POWER SUPPLIES						
Supply Voltage						
AVDD	Full	IV	2.7	3.0	3.6	V
DRVDD	Full	IV	2.25	2.5	3.6	V
Supply Current						
IAVDD[4]	Full	VI		122	137	mA
IDRVDD[4]	25°C	V		8		mA
PSRR	25°C	V		±0.01		% FSR
POWER CONSUMPTION						
Low Frequency Input[4]	25°C	V		366		mW
Standby Power[5]	25°C	V		1.0		mW

[1] With a 1.0 V internal reference.
[2] Measured at low input frequency, full-scale sine wave, with approximately 5 pF loading on each output bit.
[3] Input capacitance refers to the effective capacitance between one differential input pin and AGND. Refer to Figure 5 for the equivalent analog input structure.
[4] Measured at AC Specifications conditions without output drivers.
[5] Measured with a dc input, CLK pin inactive (that is, set to AVDD or AGND).

AC SPECIFICATIONS

AVDD = 3 V, DRVDD = 2.5 V, sample rate = 80 MSPS, 2 V p-p differential input, 1.0 V external reference, AIN = –0.5 dBFS, DCS off, unless otherwise noted.

Table 2.

			AD9236BRU/AD9236BCP			
Parameter	**Temp**	**Test Level**	**Min**	**Typ**	**Max**	**Unit**
SIGNAL-TO-NOISE-RATIO (SNR)						
f_{IN} = 2.4 MHz	Full	VI	68.6			dB
	25°C	V		70.9		dB
f_{IN} = 40 MHz	25°C	V		70.4		dB
f_{IN} = 70 MHz	Full	IV	67.8			dB
	25°C	V		70.1		dB
f_{IN} = 100 MHz	25°C	V		69.0		dB
SIGNAL-TO-NOISE AND DISTORTION (SINAD)						
f_{IN} = 2.4 MHz	Full	VI	68.4			dB
	25°C	V		70.8		dB
f_{IN} = 40 MHz	25°C	V		70.2		dB
f_{IN} = 70 MHz	Full	IV	67.4			dB
	25°C	V		69.8		dB
f_{IN} = 100 MHz	25°C	V		68.0		dB
EFFECTIVE NUMBER OF BITS (ENOB)						
f_{IN} = 2.4 MHz	Full	VI	11.1			Bits
	25°C	V		11.5		Bits
f_{IN} = 40 MHz	25°C	V		11.4		Bits
f_{IN} = 70 MHz	Full	IV	10.9			Bits
	25°C	V		11.3		Bits
f_{IN} = 100 MHz	25°C	V		11.0		Bits
WORST SECOND OR THIRD						
f_{IN} = 2.4 MHz	Full	VI			–75.6	dBc
	25°C	V		–91.3		dBc
f_{IN} = 40 MHz	25°C	V		–87.8		dBc
f_{IN} = 70 MHz	Full	VI			–73.2	dBc
	25°C	V		–81.4		dBc
f_{IN} = 100 MHz	25°C	V		–76.4		dBc
SPURIOUS FREE DYNAMIC RANGE (SFDR)						
f_{IN} = 2.4 MHz	Full	VI	75.6			dBc
	25°C	V		91.3		dBc
f_{IN} = 40 MHz	25°C	V		87.8		dBc
f_{IN} = 70 MHz	Full	IV	73.2			dBc
	25°C	V		81.4		dBc
f_{IN} = 100 MHz	25°C	V		76.4		dBc

DIGITAL SPECIFICATIONS

AVDD = 3 V, DRVDD = 2.5 V, 1.0 V external reference, unless otherwise noted.

Table 3.

Parameter	Temp	Test Level	AD9236BRU/AD9236BCP Min	Typ	Max	Unit
LOGIC INPUTS (CLK, PDWN)						
High Level Input Voltage	Full	IV	2.0			V
Low Level Input Voltage	Full	IV			0.8	V
High Level Input Current	Full	IV	−10		+10	µA
Low Level Input Current	Full	IV	−10		+10	µA
Input Capacitance	Full	V		2		pF
DIGITAL OUTPUTS (D0–D11, OTR)[1]						
DRVDD = 3.3 V						
High Level Output Voltage (IOH = 50 µA)	Full	IV	3.29			V
High Level Output Voltage (IOH = 0.5 mA)	Full	IV	3.25			V
Low Level Output Voltage (IOH = 1.6 mA)	Full	IV			0.2	V
Low Level Output Voltage (IOH = 50 µA)	Full	IV			0.05	V
DRVDD = 2.5 V						
High Level Output Voltage (IOH = 50 µA)	Full	IV	2.49			V
High Level Output Voltage (IOH = 0.5 mA)	Full	IV	2.45			V
Low Level Output Voltage (IOH = 1.6 mA)	Full	IV			0.2	V
Low Level Output Voltage (IOH = 50 µA)	Full	IV			0.05	V

[1] Output voltage levels measured with 5 pF load on each output.

SWITCHING SPECIFICATIONS

AVDD = 3 V, DRVDD = 2.5 V, unless otherwise noted.

Table 4.

Parameter	Temp	Test Level	AD9236BRU/AD9236BCP Min	Typ	Max	Unit
CLOCK INPUT PARAMETERS						
Maximum Conversion Rate	Full	VI	80			MSPS
Minimum Conversion Rate	Full	V			1	MSPS
CLK Period	Full	V	12.5			ns
CLK Pulse Width High[1]	Full	V	4.0			ns
CLK Pulse Width Low[1]	Full	V	4.0			ns
DATA OUTPUT PARAMETERS						
Output Propagation Delay (t_{PD})[2]	Full	V		3.5		ns
Pipeline Delay (Latency)	Full	V		7		Cycles
Aperture Delay (t_A)	Full	V		1.0		ns
Aperture Uncertainty (Jitter, t_J)	Full	V		0.3		ps rms
Wake-Up Time[3]	Full	V		7		ms
OUT OF RANGE RECOVERY TIME	Full	V		2		Cycles

[1] With duty cycle stabilizer (DCS) enabled.
[2] Output propagation delay is measured from CLK 50% transition to DATA 50% transition, with 5 pF load.
[3] Wake-up time is dependant on the value of the decoupling capacitors; typical values shown with 0.1 µF and 10 µF capacitors on REFT and REFB.

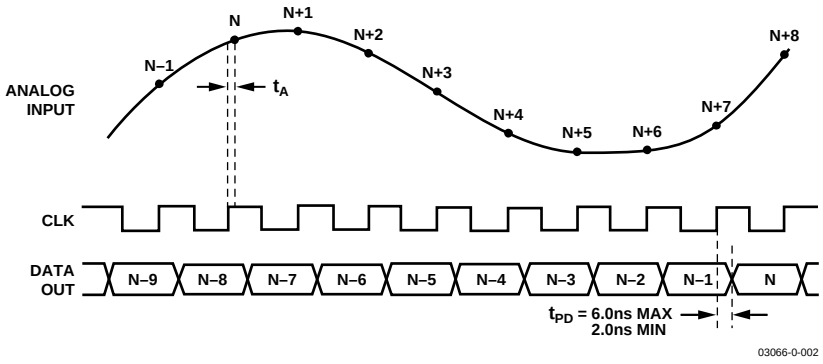

Figure 2. Timing Diagram

Table 5. Explanation of Test Levels

Test Level	Definitions
I	100% production tested.
II	100% production tested at 25°C and guaranteed by design and characterization at specified temperatures.
III	Sample tested only.
IV	Parameter is guaranteed by design and characterization testing.
V	Parameter is a typical value only.
VI	100% production tested at 25°C and guaranteed by design and characterization for industrial temperature range.

ABSOLUTE MAXIMUM RATINGS

Table 6.

Parameter	With Respect to	Min	Max	Unit
ELECTRICAL				
AVDD	AGND	–0.3	+3.9	V
DRVDD	DGND	–0.3	+3.9	V
AGND	DGND	–0.3	+0.3	V
AVDD	DRVDD	–3.9	+3.9	V
D0 to D11	DGND	–0.3	DRVDD + 0.3	V
CLK, MODE	AGND	–0.3	AVDD + 0.3	V
VIN+, VIN–	AGND	–0.3	AVDD + 0.3	V
VREF	AGND	–0.3	AVDD + 0.3	V
SENSE	AGND	–0.3	AVDD + 0.3	V
REFT, REFB	AGND	–0.3	AVDD + 0.3	V
PDWN	AGND	–0.3	AVDD + 0.3	V
ENVIRONMENTAL				
Storage Temperature		–65	+125	°C
Operating Temperature Range		–40	+85	°C
Lead Temperature (Soldering 10 sec)			300	°C
Junction Temperature			150	°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions on a 4-layer board in still air, in accordance with EIA/JESD51-1.

Table 7.

Package Type	θ_{JA}	θ_{JC}	Unit
RU-28	67.7		°C/W
CP-32-7	32.5	32.71	°C/W

Airflow increases heat dissipation effectively, reducing θ_{JA}. In addition, more metal directly in contact with the package leads from metal traces, through holes, ground, and power planes reduces the θ_{JA}. It is recommended that the exposed paddle be soldered to the ground plane for the LFCSP package. There is an increased reliability of the solder joints, and maximum thermal capability of the package is achieved with the exposed paddle soldered to the customer board.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

TERMINOLOGY

Analog Bandwidth (Full Power Bandwidth)
The analog input frequency at which the spectral power of the fundamental frequency (as determined by the FFT analysis) is reduced by 3 dB.

Aperture Delay (t_A)
The delay between the 50% point of the rising edge of the clock and the instant at which the analog input is sampled.

Aperture Uncertainty (Jitter, t_J)
The sample-to-sample variation in aperture delay.

Integral Nonlinearity (INL)
The deviation of each individual code from a line drawn from negative full scale through positive full scale. The point used as negative full scale occurs ½ LSB before the first code transition. Positive full scale is defined as a level 1½ LSB beyond the last code transition. The deviation is measured from the middle of each particular code to the true straight line.

Differential Nonlinearity (DNL, No Missing Codes)
An ideal ADC exhibits code transitions that are exactly 1 LSB apart. DNL is the deviation from this ideal value. Guaranteed no missing codes to 12-bit resolution indicates that all 4096 codes must be present over all operating ranges.

Offset Error
The major carry transition should occur for an analog value ½ LSB below VIN+ = VIN–. Offset error is defined as the deviation of the actual transition from that point.

Gain Error
The first code transition should occur at an analog value ½ LSB above negative full scale. The last transition should occur at an analog value 1½ LSB below positive full scale. Gain error is the deviation of the actual difference between first and last code transitions and the ideal difference between first and last code transitions.

Temperature Drift
The temperature drift for offset error and gain error specifies the maximum change from the initial (25°C) value to the value at T_{MIN} or T_{MAX}.

Power Supply Rejection Ratio
The change in full scale from the value with the supply at the minimum limit to the value with the supply at its maximum limit.

Total Harmonic Distortion (THD)[1]
The ratio of the rms input signal amplitude to the rms value of the sum of the first six harmonic components.

Signal-to-Noise and Distortion (SINAD)[1]
The ratio of the rms input signal amplitude to the rms value of the sum of all other spectral components below the Nyquist frequency, including harmonics but excluding dc.

Effective Number of Bits (ENOB)
The effective number of bits for a sine wave input at a given input frequency can be calculated directly from its measured *SINAD* using the following formula

$$ENOB = \frac{(SINAD - 1.76)}{6.02}$$

Signal-to-Noise Ratio (SNR)[1]
The ratio of the rms input signal amplitude to the rms value of the sum of all other spectral components below the Nyquist frequency, excluding the first six harmonics and dc.

Spurious Free Dynamic Range (SFDR)[1]
The difference in dB between the rms input signal amplitude and the peak spurious signal. The peak spurious component may or may not be a harmonic.

Two-Tone SFDR[1]
The ratio of the rms value of either input tone to the rms value of the peak spurious component. The peak spurious component may or may not be an IMD product.

Clock Pulse Width and Duty Cycle
Pulse width high is the minimum amount of time that the clock pulse should be left in the Logic 1 state to achieve rated performance. Pulse width low is the minimum time the clock pulse should be left in the low state. At a given clock rate, these specifications define an acceptable clock duty cycle.

Minimum Conversion Rate
The clock rate at which the SNR of the lowest analog signal frequency drops by no more than 3 dB below the guaranteed limit.

Maximum Conversion Rate
The clock rate at which parametric testing is performed.

Output Propagation Delay (t_{PD})
The delay between the clock rising edge and the time when all bits are within valid logic levels.

Out-of-Range Recovery Time
The time it takes for the ADC to reacquire the analog input after a transition from 10% above positive full scale to 10% above negative full scale, or from 10% below negative full scale to 10% below positive full scale.

[1] AC specifications may be reported in dBc (degrades as signal levels are lowered) or in dBFS (always related back to converter full scale).

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

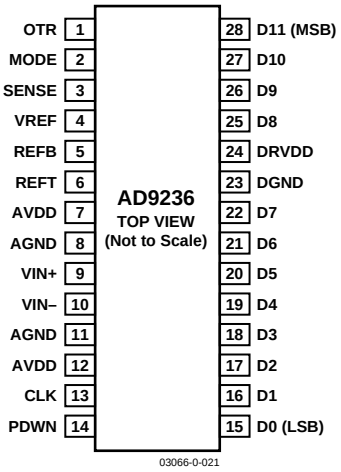

Figure 3. 28-Lead TSSOP

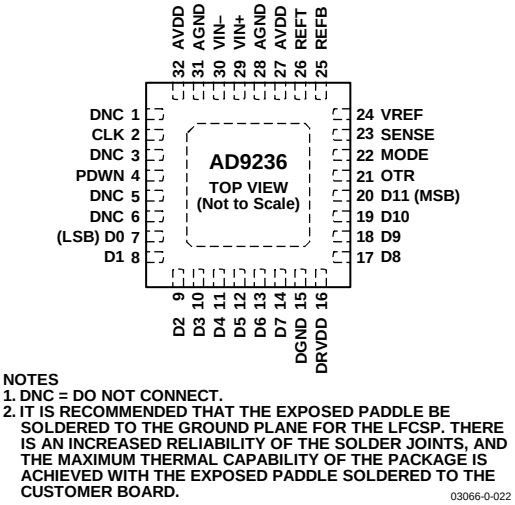

Figure 4. 32-Lead LFCSP

Table 8. Pin Function Descriptions—28-Lead TSSOP

Pin No.	Mnemonic	Description
1	OTR	Out-of-Range Indicator
2	MODE	Data Format Select and DCS Mode Selection
3	SENSE	Reference Mode Selection
4	VREF	Voltage Reference Input/Output
5	REFB	Differential Reference (–)
6	REFT	Differential Reference (+)
7, 12	AVDD	Analog Power Supply
8, 11	AGND	Analog Ground
9	VIN+	Analog Input Pin (+)
10	VIN–	Analog Input Pin (–)
13	CLK	Clock Input Pin
14	PDWN	Power-Down Function Select
15 to 22, 25 to 28	D0 (LSB) to D11 (MSB)	Data Output Bits
23	DGND	Digital Output Ground
24	DRVDD	Digital Output Driver Supply

Table 9. Pin Function Descriptions—32-Lead LFCSP

Pin No.	Mnemonic	Description
1, 3, 5, 6	DNC	Do Not Connect
2	CLK	Clock Input Pin
4	PDWN	Power-Down Function Select
7 to 14, 17 to 20	D0 (LSB) to D11 (MSB)	Data Output Bits
15	DGND	Digital Output Ground
16	DRVDD	Digital Output Driver Supply
21	OTR	Out-of-Range Indicator
22	MODE	Data Format Select and DCS Mode Selection
23	SENSE	Reference Mode Selection
24	VREF	Voltage Reference Input/Output
25	REFB	Differential Reference (–)
26	REFT	Differential Reference (+)
27, 32	AVDD	Analog Power Supply
28, 31	AGND	Analog Ground
29	VIN+	Analog Input Pin (+)
30	VIN–	Analog Input Pin (–)
	EP	Exposed Pad. It is recommended that the exposed paddle be soldered to the ground plane for the LFCSP. There is an increased reliability of the solder joints, and the maximum thermal capability of the package is achieved with the exposed paddle soldered to the customer board.

EQUIVALENT CIRCUITS

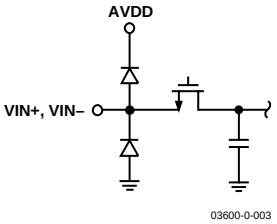

Figure 5. Equivalent Analog Input Circuit

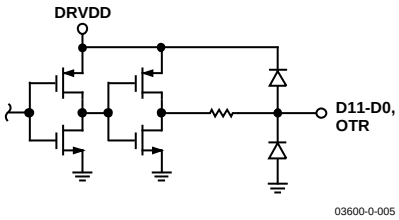

Figure 7. Equivalent Digital Output Circuit

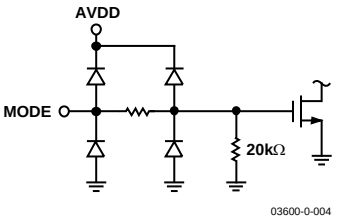

Figure 6. Equivalent MODE Input Circuit

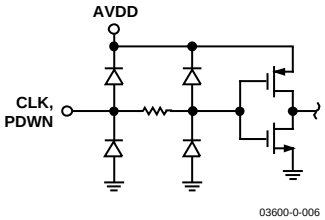

Figure 8. Equivalent Digital Input Circuit

TYPICAL PERFORMANCE CHARACTERISTICS

AVDD = 3.0 V, DRVDD = 2.5 V, sample rate = 80 MSPS, DCS disabled, T_A = 25°C, 2 V p-p differential input, AIN = −0.5 dBFS, VREF = 1.0 V external, unless otherwise noted.

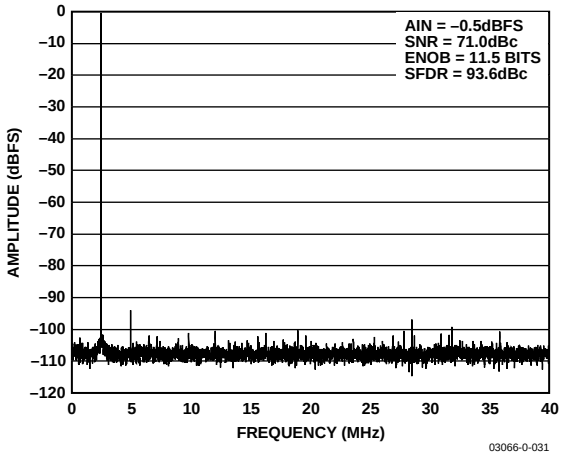

Figure 9. Single Tone 8K FFT @ 2.5 MHz

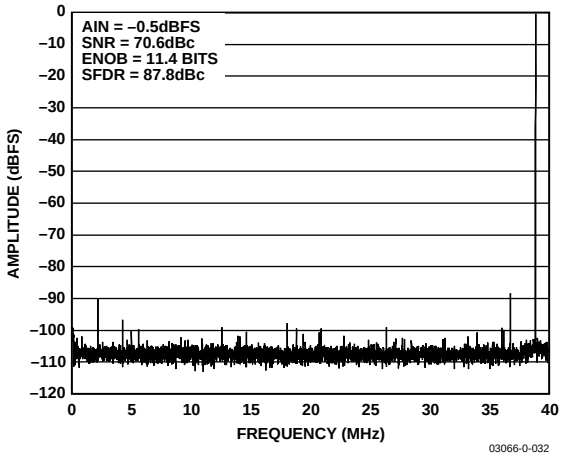

Figure 10. Single Tone 8K FFT @ 39 MHz

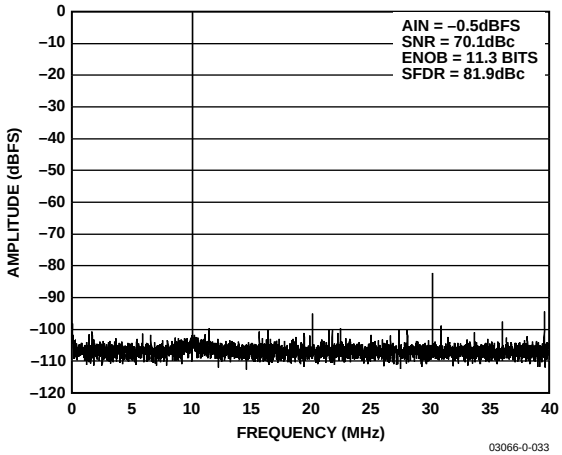

Figure 11. Single Tone 8K FFT @ 70 MHz

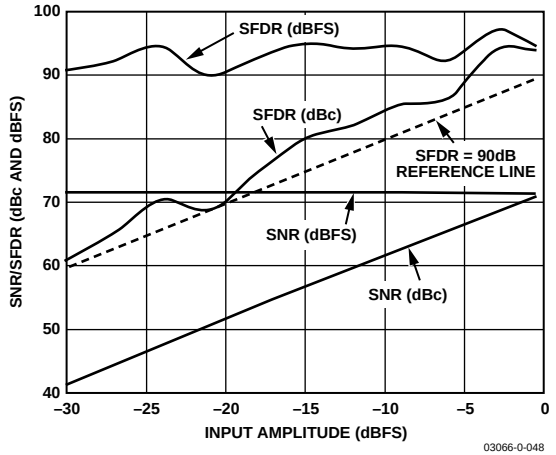

Figure 12. Single Tone SNR/SFDR vs. Input Amplitude (AIN) @ 2.5 MHz

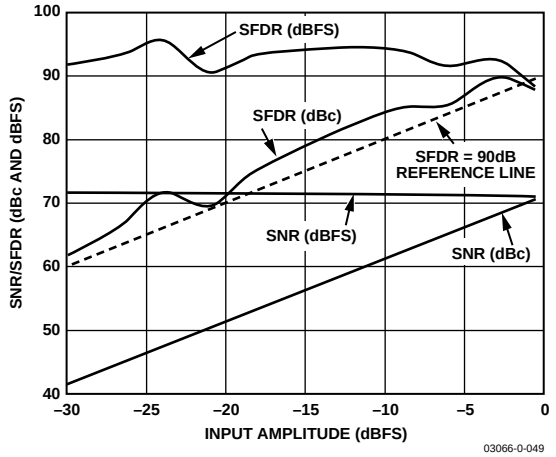

Figure 13. Single Tone SNR/SFDR vs. Input Amplitude (AIN) @ 39 MHz

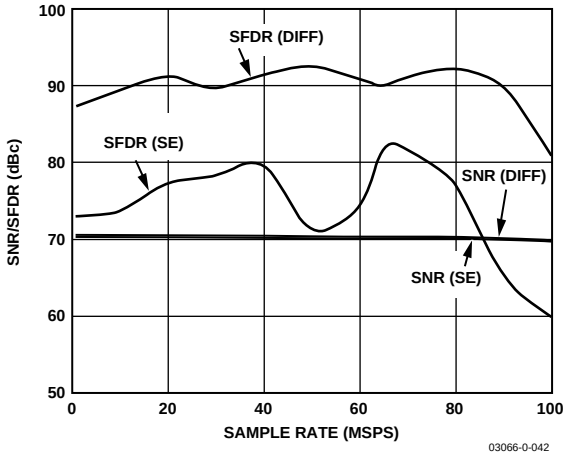

Figure 14. SNR/SFDR vs. Sample Rate @ 10 MHz

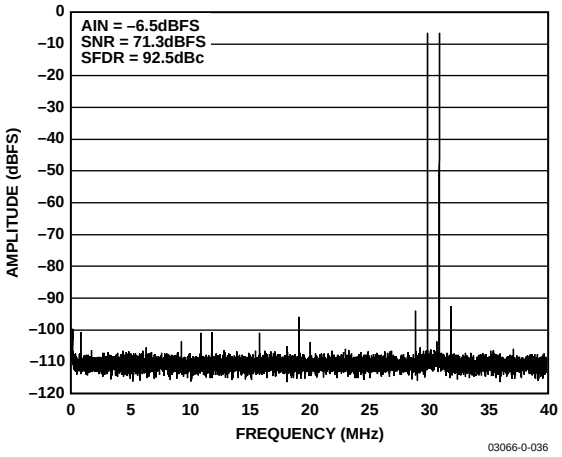

Figure 15. Two-Tone 8K FFT @ 30 MHz and 31 MHz

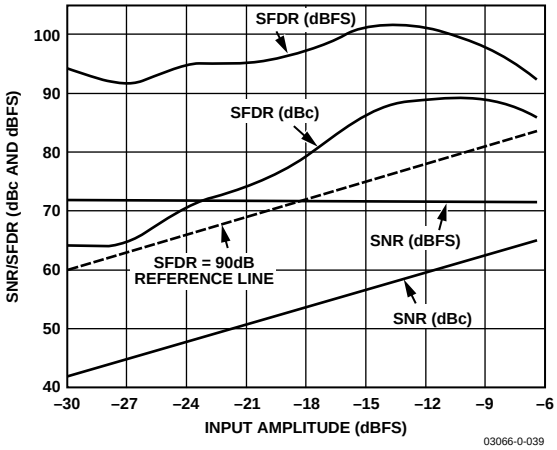

Figure 18. Two-Tone SNR/SFDR vs. Input Amplitude @ 30 MHz and 31 MHz

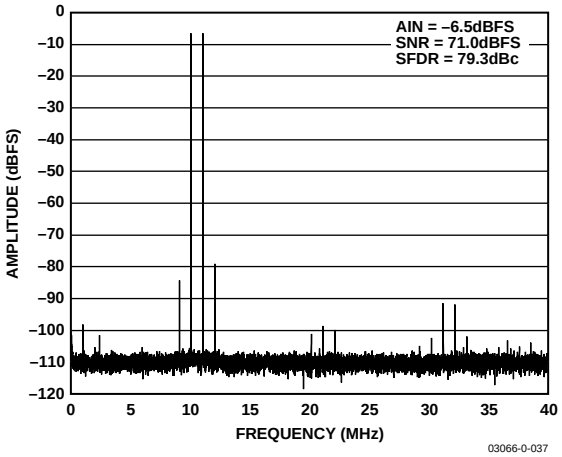

Figure 16. Two-Tone 8K FFT @ 69 MHz and 70 MHz

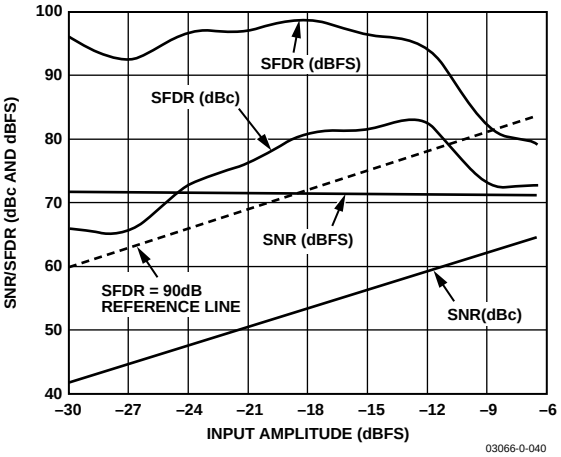

Figure 19. Two-Tone SNR/SFDR vs. Input Amplitude @ 69 MHz and 70 MHz

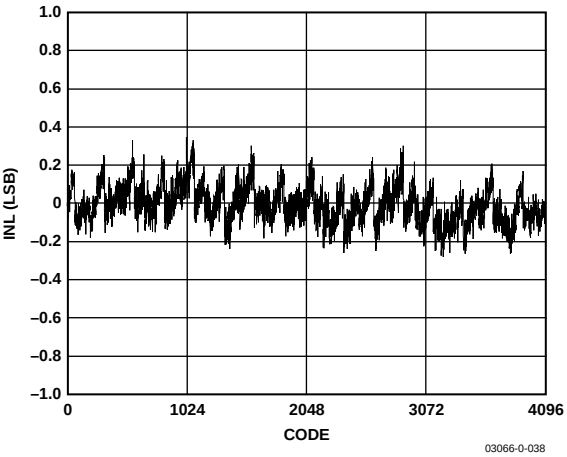

Figure 17. Typical INL

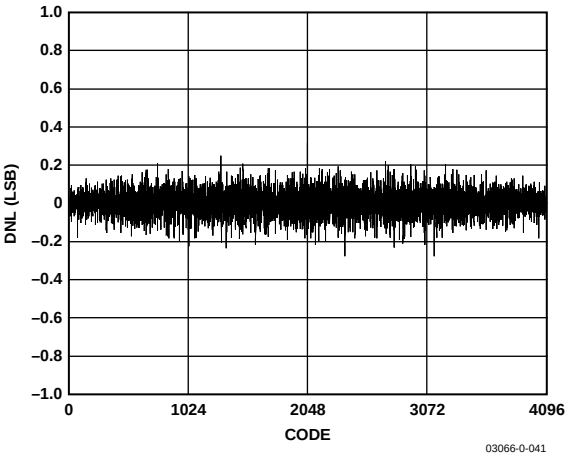

Figure 20. Typical DNL

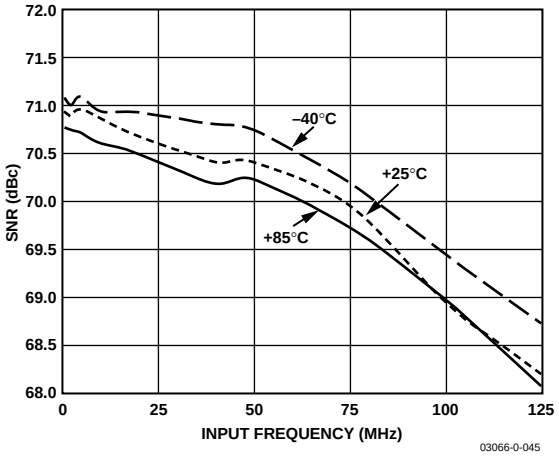

Figure 21. SNR vs. Input Frequency

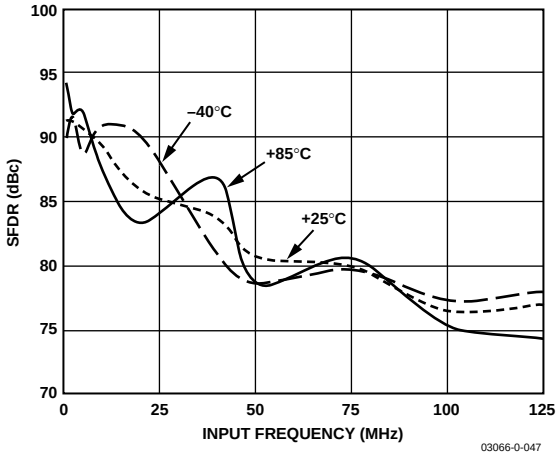

Figure 24. SFDR vs. Input Frequency

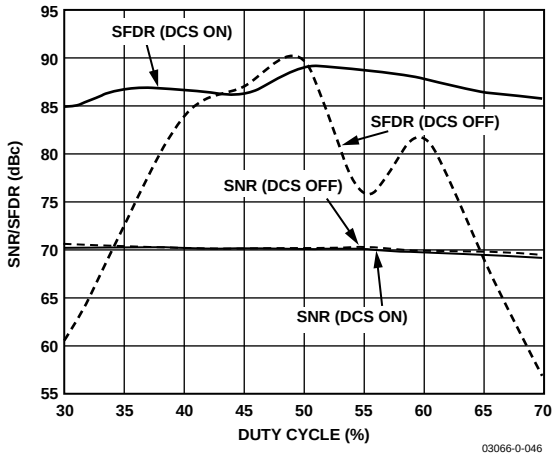

Figure 22. SNR/SFDR vs. Clock Duty Cycle

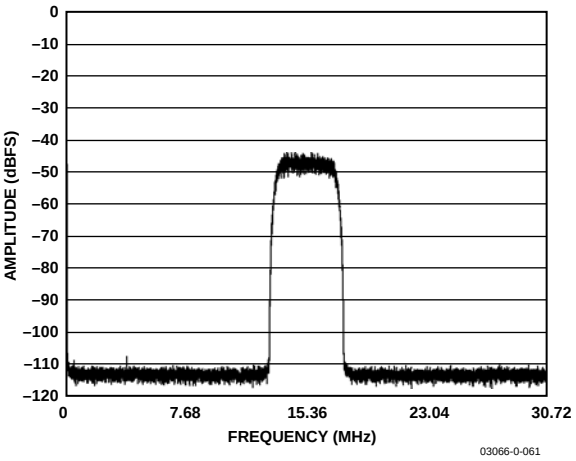

Figure 25. 32K FFT WCDMA Carrier @ F_{IN} =76.8 MHz, Sample Rate = 61.44 MSPS

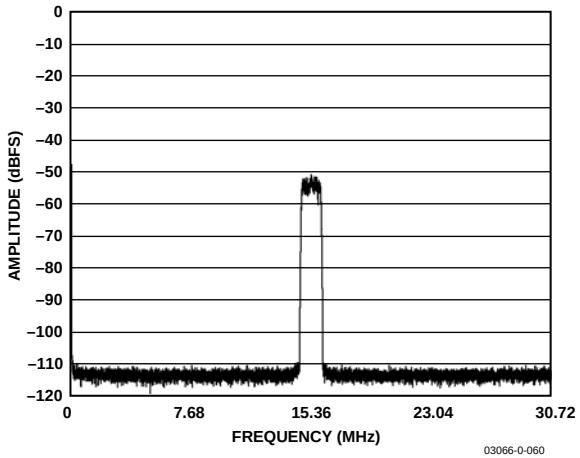

Figure 23. 32K FFT CDMA-2000 Carrier @ F_{IN} = 46.08 MHz, Sample Rate = 61.44 MSPS

THEORY OF OPERATION

The AD9236 architecture consists of a front-end sample-and-hold amplifier (SHA) followed by a pipelined switched capacitor ADC. The pipelined ADC is divided into three sections, consisting of a 4-bit first stage followed by eight 1.5-bit stages and a final 3-bit flash. Each stage provides sufficient overlap to correct for flash errors in the preceding stages. The quantized outputs from each stage are combined into a final 12-bit result in the digital correction logic. The pipelined architecture permits the first stage to operate on a new input sample, while the remaining stages operate on preceding samples. Sampling occurs on the rising edge of the clock.

Each stage of the pipeline, excluding the last, consists of a low resolution flash ADC connected to a switched capacitor DAC and interstage residue amplifier (MDAC). The residue amplifier magnifies the difference between the reconstructed DAC output and the flash input for the next stage in the pipeline. One bit of redundancy is used in each stage to facilitate digital correction of flash errors. The last stage simply consists of a flash ADC.

The input stage contains a differential SHA that can be ac- or dc-coupled in differential or single-ended modes. The output-staging block aligns the data, carries out the error correction, and passes the data to the output buffers. The output buffers are powered from a separate supply, allowing adjustment of the output voltage swing. During power-down, the output buffers go into a high impedance state.

ANALOG INPUT AND REFERENCE OVERVIEW

The analog input to the AD9236 is a differential switched capacitor SHA that has been designed for optimum performance while processing a differential input signal. The SHA input can support a wide common-mode range (VCM) and maintain excellent performance, as shown in Figure 26. An input common-mode voltage of midsupply minimizes signal-dependant errors and provides optimum performance.

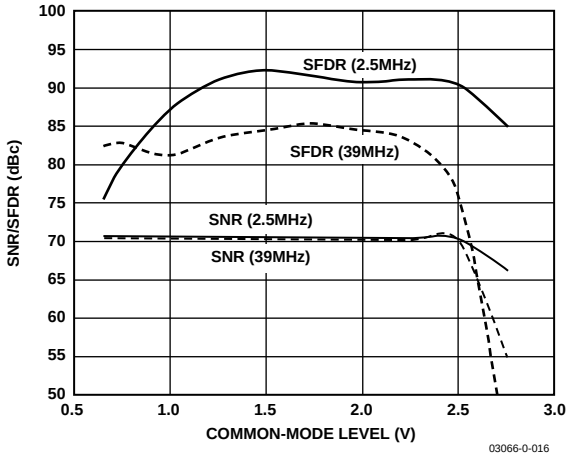

Figure 26. SNR, SFDR vs. Common-Mode Level

Referring to Figure 27, the clock signal alternately switches the SHA between sample mode and hold mode. When the SHA is switched into sample mode, the signal source must be capable of charging the sample capacitors and settling within one-half of a clock cycle. A small resistor in series with each input can help reduce the peak transient current required from the output stage of the driving source. In addition, a small shunt capacitor can be placed across the inputs to provide dynamic charging currents. This passive network creates a low-pass filter at the ADC's input; therefore, the precise values are dependant upon the application. In IF undersampling applications, any shunt capacitors should be reduced or removed. In combination with the driving source impedance, they would limit the input bandwidth.

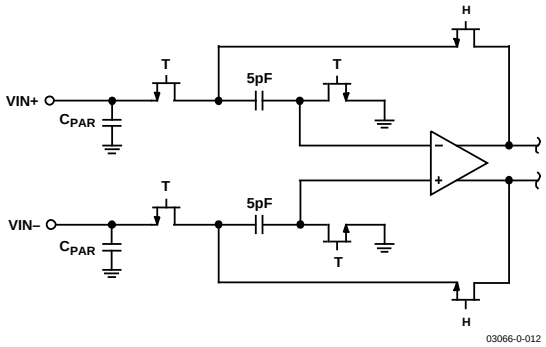

Figure 27. Switched-Capacitor SHA Input

For best dynamic performance, the source impedances driving VIN+ and VIN– should be matched such that common-mode settling errors are symmetrical. These errors are reduced by the common-mode rejection of the ADC.

An internal differential reference buffer creates positive and negative reference voltages, REFT and REFB, that define the span of the ADC core. The output common mode of the reference buffer is set to midsupply, and the REFT and REFB voltages and span are defined as follows:

$$REFT = ½(AVDD + VREF)$$

$$REFB = ½(AVDD + VREF)$$

$$Span = 2 \times (REFT - REFB) = 2 \times VREF$$

It can be seen from the previous equations that the REFT and REFB voltages are symmetrical about the midsupply voltage and, by definition, the input span is twice the value of the VREF voltage.

The internal voltage reference can be pin strapped to fixed values of 0.5 V or 1.0 V, or adjusted within the same range as discussed in the Internal Reference Connection section. Maximum SNR performance is achieved with the AD9236 set to the largest input span of 2 V p-p. The relative SNR degradation is 3 dB when changing from 2 V p-p mode to 1 V p-p mode.

The SHA can be driven from a source that keeps the signal peaks within the allowable range for the selected reference voltage. The minimum and maximum common-mode input levels are defined as:

$$VCM_{MIN} = \frac{VREF}{2}$$

$$VCM_{MAX} = \frac{(AVDD + VREF)}{2}$$

The minimum common-mode input level allows the AD9236 to accommodate ground referenced inputs.

Although optimum performance is achieved with a differential input, a single-ended source can be applied to VIN+ or VIN–. In this configuration, one input accepts the signal, while the opposite input should be set to midscale by connecting it to an appropriate reference. For example, a 2 V p-p signal can be applied to VIN+ while a 1 V reference is applied to VIN–. The AD9236 then accepts an input signal varying between 2 V and 0 V. In the single-ended configuration, distortion performance can degrade significantly as compared to the differential case. However, the effect is less noticeable at lower input frequencies.

Differential Input Configurations

As previously detailed, optimum performance is achieved while driving the AD9236 in a differential input configuration. For baseband applications, the AD8138 differential driver provides excellent performance and a flexible interface to the ADC. The output common-mode voltage of the AD8138 is easily set to AVDD/2, and the driver can be configured in a Sallen-Key filter topology to provide band limiting of the input signal.

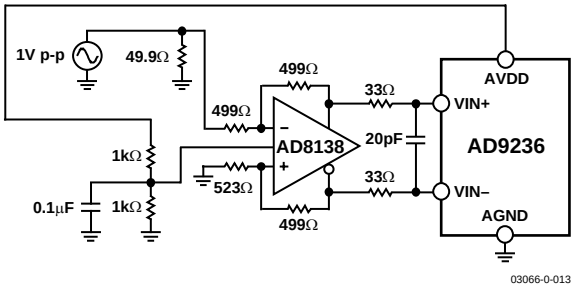

Figure 28. Differential Input Configuration Using the AD8138

At input frequencies in the second Nyquist zone and above, the performance of most amplifiers is not adequate to achieve the true performance of the AD9236. This is especially true in IF undersampling applications where frequencies in the 70 MHz to 100 MHz range are being sampled. For these applications, differential transformer coupling is the recommended input configuration. The value of the shunt capacitor is dependent on the input frequency and source impedance and should be reduced or removed. An example is shown in Figure 29.

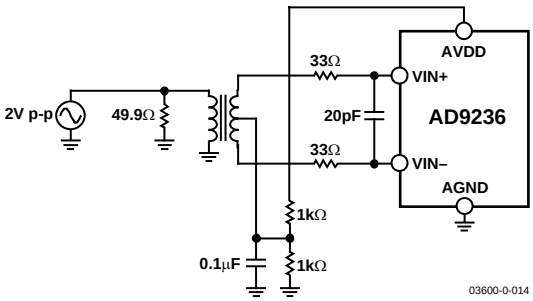

Figure 29. Differential Transformer-Coupled Configuration

The signal characteristics must be considered when selecting a transformer. Most RF transformers saturate at frequencies below a few MHz, and excessive signal power can also cause core saturation, which leads to distortion.

Single-Ended Input Configuration

A single-ended input can provide adequate performance in cost-sensitive applications. In this configuration, there is a degradation in SFDR and distortion performance due to the large input common-mode swing (see Figure 14). However, if the source impedances on each input are matched, there should be little effect on SNR performance. Figure 30 details a typical single-ended input configuration.

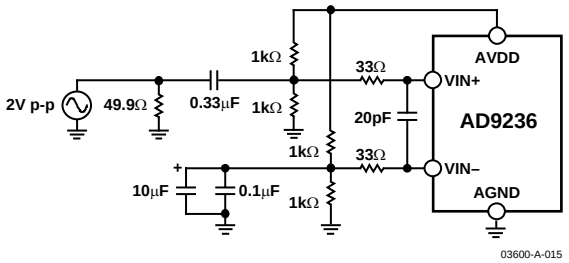

Figure 30. Single-Ended Input Configuration

CLOCK INPUT CONSIDERATIONS

Typical high speed ADCs use both clock edges to generate a variety of internal timing signals, and as a result can be sensitive to clock duty cycle. Commonly a 5% tolerance is required on the clock duty cycle to maintain dynamic performance characteristics. The AD9236 contains a clock duty cycle stabilizer (DCS) that retimes the nonsampling edge, providing an internal clock signal with a nominal 50% duty cycle. This allows a wide range of clock input duty cycles without affecting the performance of the AD9236. As shown in Figure 22, noise and distortion performance is nearly flat for a 30% to 70% duty cycle with the DCS on.

The duty cycle stabilizer uses a delay-locked loop (DLL) to create the nonsampling edge. As a result, any changes to the sampling frequency require approximately 100 clock cycles to allow the DLL to acquire and lock to the new rate.

Jitter Considerations

High speed, high resolution ADCs are sensitive to the quality of the clock input. The degradation in SNR at a given input frequency (f_{INPUT}) due only to aperture jitter (t_J) can be calculated with the following equation:

$$SNR = 20\log_{10}\left[\frac{1}{2\pi f_{INPUT} \times t_J}\right]$$

In the equation, the rms aperture jitter represents the root-mean square of all jitter sources, which include the clock input, analog input signal, and ADC aperture jitter specification. IF undersampling applications are particularly sensitive to jitter (see Figure 31).

The clock input should be treated as an analog signal in cases where aperture jitter can affect the dynamic range of the AD9236. Power supplies for clock drivers should be separated from the ADC output driver supplies to avoid modulating the clock signal with digital noise. Low jitter, crystal controlled oscillators make the best clock sources. If the clock is generated from another type of source (by gating, dividing, or other methods), it should be retimed by the original clock at the last step.

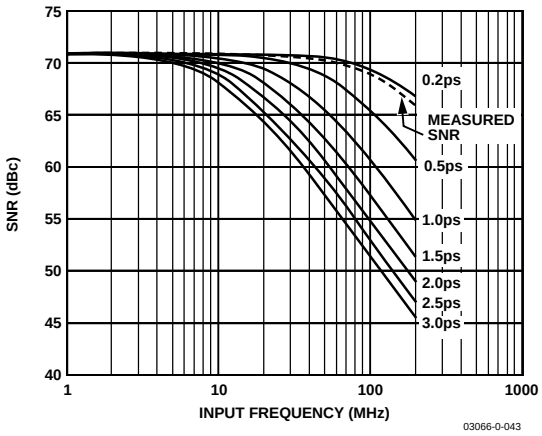

Figure 31. SNR vs. Input Frequency and Jitter

POWER DISSIPATION AND STANDBY MODE

As shown in Figure 32, the power dissipated by the AD9236 is proportional to its sample rate. The digital power dissipation is determined primarily by the strength of the digital drivers and the load on each output bit. The maximum DRVDD current (I_{DRVDD}) can be calculated as

$$I_{DRVDD} = V_{DRVDD} \times C_{LOAD} \times f_{CLK} \times N$$

$$I_{DRVDD} = V_{DRVDD} \times C_{LOAD} \times f_{CLK} \times N$$

where N is the number of output bits, 12 in the case of the AD9236. This maximum current occurs when every output bit switches on every clock cycle, that is, a full-scale square wave at the Nyquist frequency, $f_{CLK}/2$. In practice, the DRVDD current is established by the average number of output bits switching, which is determined by the sample rate and the characteristics of the analog input signal.

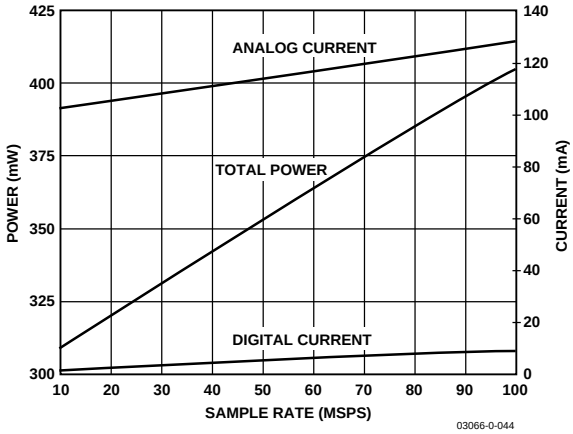

Figure 32. Power and Current vs. Sample Rate @ 2.5 MHz

Reducing the capacitive load presented to the output drivers can minimize digital power consumption. The data in Figure 32 was taken with the same operating conditions as the Typical Performance Characteristics, and with a 5 pF load on each output driver.

By asserting the PDWN pin high, the AD9236 is placed in standby mode. In this state, the ADC typically dissipates 1 mW if the CLK and analog inputs are static. During standby, the output drivers are placed in a high impedance state. Reasserting the PDWN pin low returns the AD9236 to its normal operational mode.

Low power dissipation in standby mode is achieved by shutting down the reference, reference buffer, and biasing networks. The decoupling capacitors on REFT and REFB are discharged when entering standby mode and then must be recharged when returning to normal operation. As a result, the wake-up time is related to the time spent in standby mode, and shorter standby cycles result in proportionally shorter wake-up times. With the recommended 0.1 µF and 10 µF decoupling capacitors on REFT and REFB, it takes approximately 1 second to fully discharge the reference buffer decoupling capacitors and 7 ms to restore full operation.

DIGITAL OUTPUTS

The AD9236 output drivers can be configured to interface with 2.5 V or 3.3 V logic families by matching DRVDD to the digital supply of the interfaced logic. The output drivers are sized to provide sufficient output current to drive a wide variety of logic families. However, large drive currents tend to cause current glitches on the supplies, which can affect converter performance. Applications requiring the ADC to drive large capacitive loads or large fanouts can require external buffers or latches.

As detailed in Table 11, the data format can be selected for either offset binary or twos complement.

TIMING

The AD9236 provides latched data outputs with a pipeline delay of seven clock cycles. Data outputs are available one propagation delay (t_{PD}) after the rising edge of the clock signal. Refer to Figure 2 for a detailed timing diagram.

The length of the output data lines and the loads placed on them should be minimized to reduce transients within the AD9236. These transients can degrade the converter's dynamic performance.

The lowest typical conversion rate of the AD9236 is 1 MSPS. At clock rates below 1 MSPS, dynamic performance can degrade.

VOLTAGE REFERENCE

A stable and accurate 0.5 V voltage reference is built into the AD9236. The input range can be adjusted by varying the reference voltage applied to the AD9236 using either the internal reference or an externally applied reference voltage. The input span of the ADC tracks reference voltage changes linearly. The various reference modes are summarized in Table 10 and described in the following sections.

If the ADC is being driven differentially through a transformer, the reference voltage can be used to bias the center tap (common-mode voltage).

Internal Reference Connection

A comparator within the AD9236 detects the potential at the SENSE pin and configures the reference into four possible states, which are summarized in Table 10. If SENSE is grounded, the reference amplifier switch is connected to the internal resistor divider (see Figure 33), setting VREF to 1 V. Connecting the SENSE pin to VREF switches the reference amplifier output to the SENSE pin, completing the loop and providing a 0.5 V reference output. If a resistor divider is connected as shown in Figure 34, the switch is again set to the SENSE pin. This puts the reference amplifier in a noninverting mode with the VREF output defined as follows:

$$VREF = 0.5 \times \left(1 + \frac{R2}{R1}\right)$$

In all reference configurations, REFT and REFB drive the A/D conversion core and establish its input span. The input range of the ADC always equals twice the voltage at the reference pin for either an internal or an external reference.

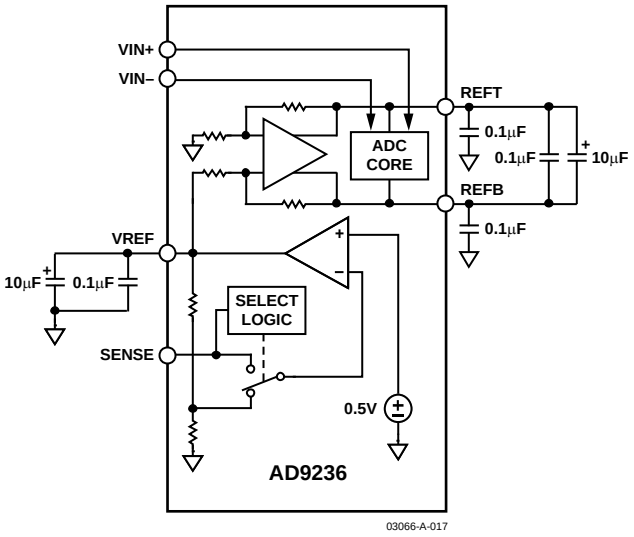

Figure 33. Internal Reference Configuration

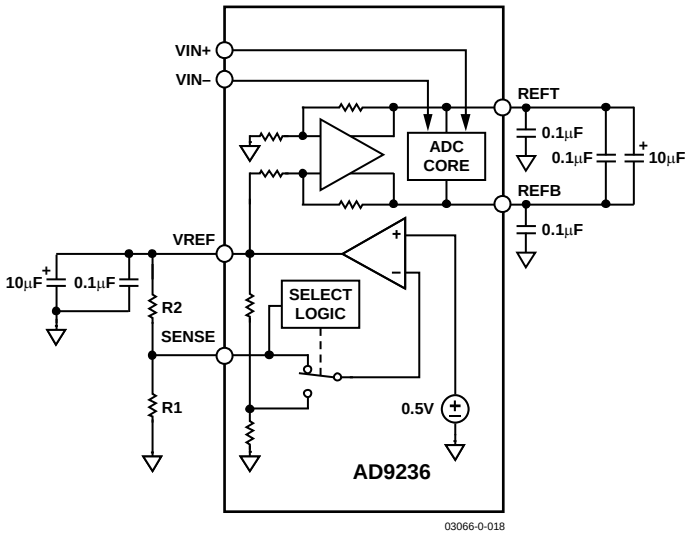

Figure 34. Programmable Reference Configuration

Table 10. Reference Configuration Summary

Selected Mode	SENSE Voltage	Resulting VREF (V)	Resulting Differential Span (V p-p)
External Reference	AVDD	N/A	2 × External Reference
Internal Fixed Reference	VREF	0.5	1.0
Programmable Reference	0.2 V to VREF	$0.5 \times \left(1 + \frac{R2}{R1}\right)$ (See Figure 34)	2 × VREF
Internal Fixed Reference	AGND to 0.2 V	1.0	2.0

If the internal reference of the AD9236 is used to drive multiple converters to improve gain matching, the loading of the reference by the other converters must be considered. Figure 35 depicts how the internal reference voltage is affected by loading. A 2 mA load is the maximum recommended load.

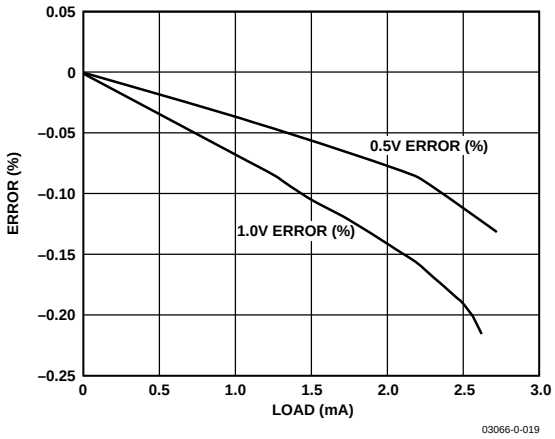

Figure 35. VREF Accuracy vs. Load

External Reference Operation

The use of an external reference can be necessary to enhance the gain accuracy of the ADC or to improve thermal drift characteristics. When multiple ADCs track one another, a single reference (internal or external) can be necessary to reduce gain matching errors to an acceptable level. Figure 36 shows the typical drift characteristics of the internal reference in both 1.0 V and 0.5 V modes.

When the SENSE pin is tied to AVDD, the internal reference is disabled, allowing the use of an external reference. An internal reference buffer loads the external reference with an equivalent 7 kΩ load. The internal buffer still generates the positive and negative full-scale references, REFT and REFB, for the ADC core. The input span is always twice the value of the reference voltage; therefore, the external reference must be limited to a maximum of 1.0 V.

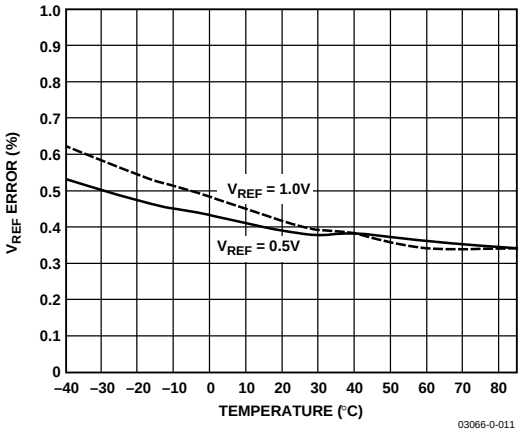

Figure 36. Typical VREF Drift

OPERATIONAL MODE SELECTION

As discussed in the Digital Outputs section, the AD9236 can output data in either offset binary or twos complement format. There is also a provision for enabling or disabling the clock duty cycle stabilizer (DCS). The MODE pin is a multilevel input that controls the data format and DCS state. The input threshold values and corresponding mode selections are outlined in Table 11.

Table 11. Mode Selection

MODE Voltage	Data Format	Duty Cycle Stabilizer
AVDD	Twos Complement	Disabled
2/3 AVDD	Twos Complement	Enabled
1/3 AVDD	Offset Binary	Enabled
AGND (Default)	Offset Binary	Disabled

EVALUATION BOARD

The AD9236 evaluation board provides all of the support circuitry required to operate the ADC in its various modes and configurations. Complete schematics and layout plots follow and demonstrate the proper routing and grounding techniques that should be applied at the system level.

It is critical that signal sources with very low phase noise (< 1 ps rms jitter) be used to realize the ultimate performance of the converter. Proper filtering of the input signal, to remove harmonics and lower the integrated noise at the input, is also necessary to achieve the specified noise performance.

TSSOP Evaluation Board

Figure 37 shows the typical bench setup used to evaluate the ac performance of the AD9236. The AD9236 can be driven single-ended or differentially through an AD8138 driver or a transformer. Separate power pins are provided to isolate the DUT from the support circuitry. Each input configuration can be selected by proper connection of various jumpers (refer to the schematics).

The AUXCLK input should be selected in applications requiring the lowest jitter and SNR performance (that is, IF undersampling characterization). It allows the user to apply a clock input signal that is 4× the target sample rate of the AD9236. A low jitter, differential divide-by-4 counter, the MC100LVEL33D, provides a 1× clock output that is subsequently returned back to the CLK input via JP9. For example, a 260 MHz signal (sinusoid) is divided down to a 65 MHz signal for clocking the ADC. Note that R1 must be removed with the AUXCLK interface. Lower jitter is often achieved with this interface since many RF signal generators display improved phase noise at higher output frequencies and the slew rate of the sinusoidal output signal is 4× that of a 1× signal of equal amplitude.

LFCSP Evaluation Board

The typical bench setup used to evaluate the ac performance of the AD9236 is similar to the TSSOP evaluation board connections. The AD9236 can be driven single-ended or differentially through a transformer. Separate power pins are provided to isolate the DUT from the support circuitry. Each input configuration can be selected by proper connection of various jumpers (see Figure 48).

An alternative differential analog input path using an AD8351 op amp is included in the layout but is not populated in production. Designers interested in evaluating the op amp with the ADC should remove C15, R12, and R3 and populate the op amp circuit. The passive network between the AD8351 outputs and the AD9236 allows the user to optimize the frequency response of the op amp for their application.

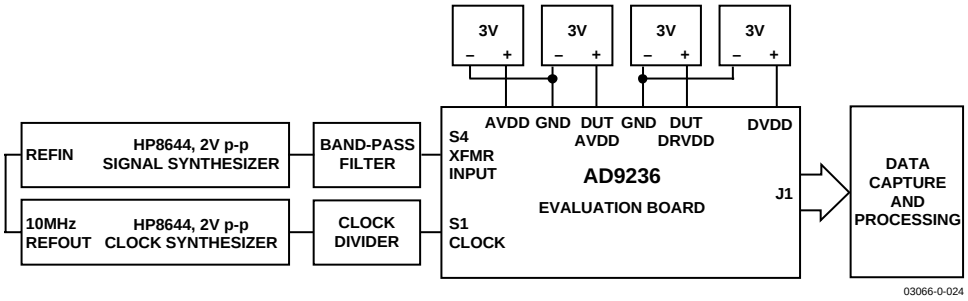

Figure 37. TSSOP Evaluation Board Connections

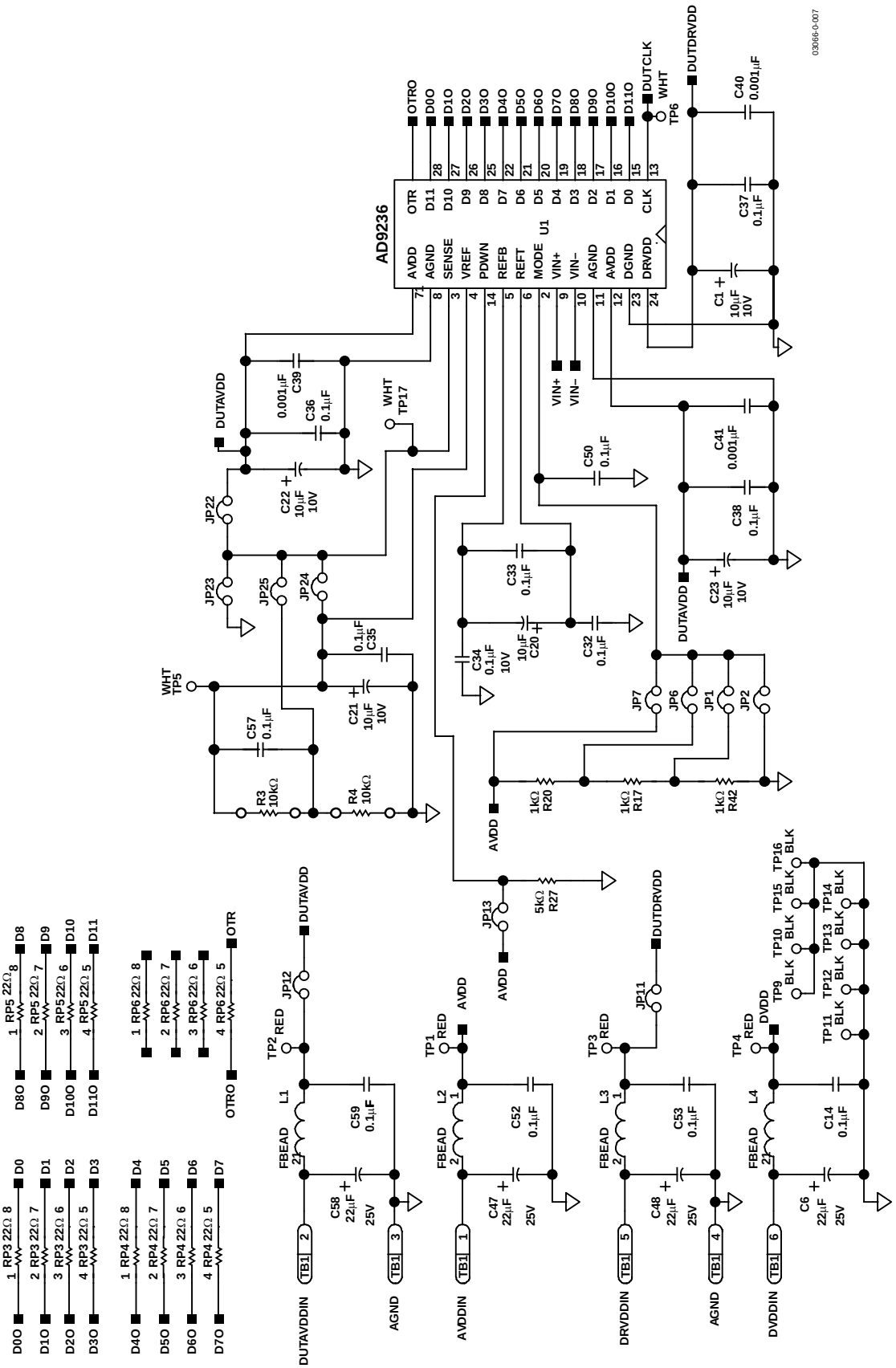

Figure 38. TSSOP Evaluation Board Schematic, DUT

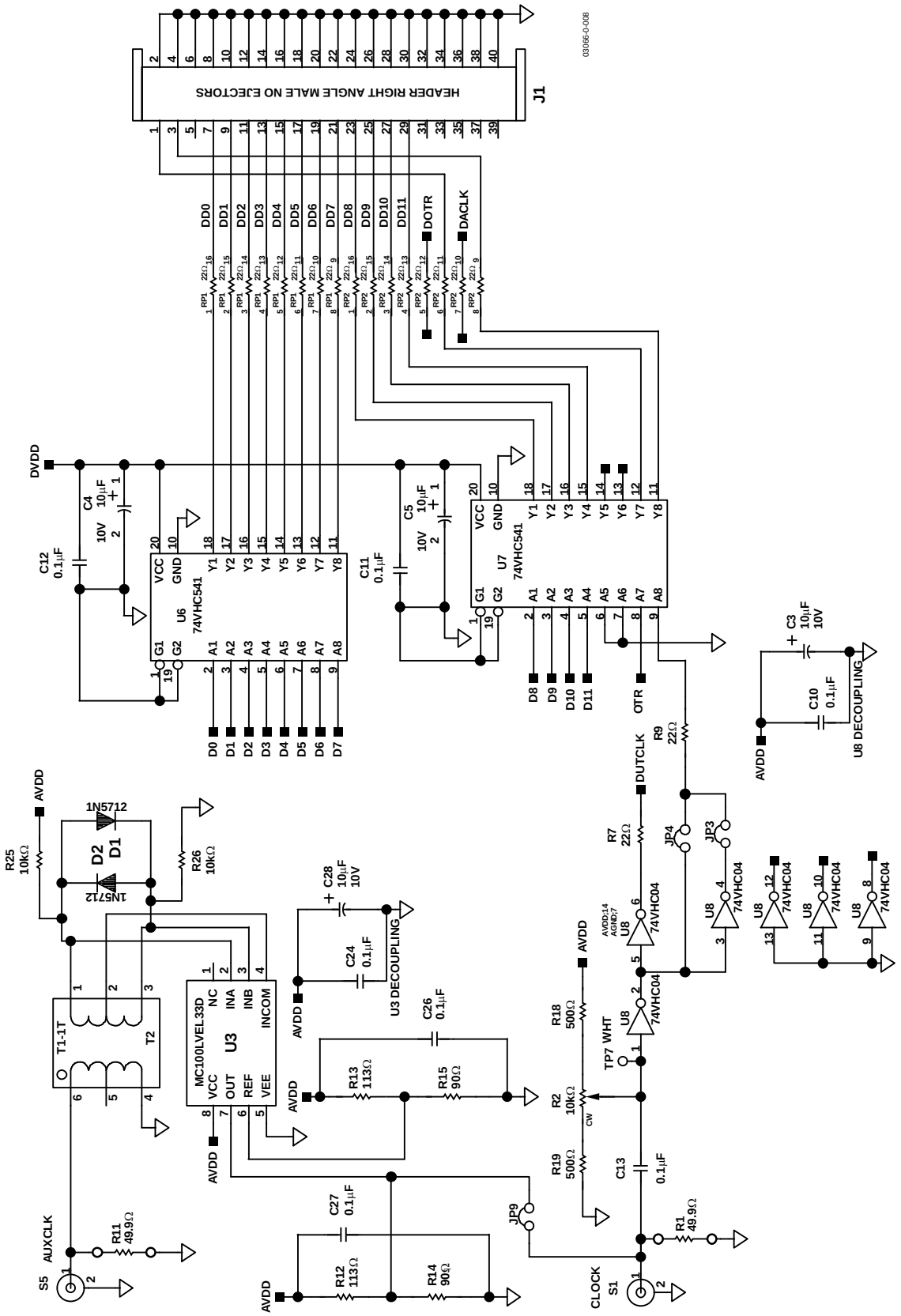

Figure 39. TSSOP Evaluation Board Schematic, Clock Inputs and Output Buffering

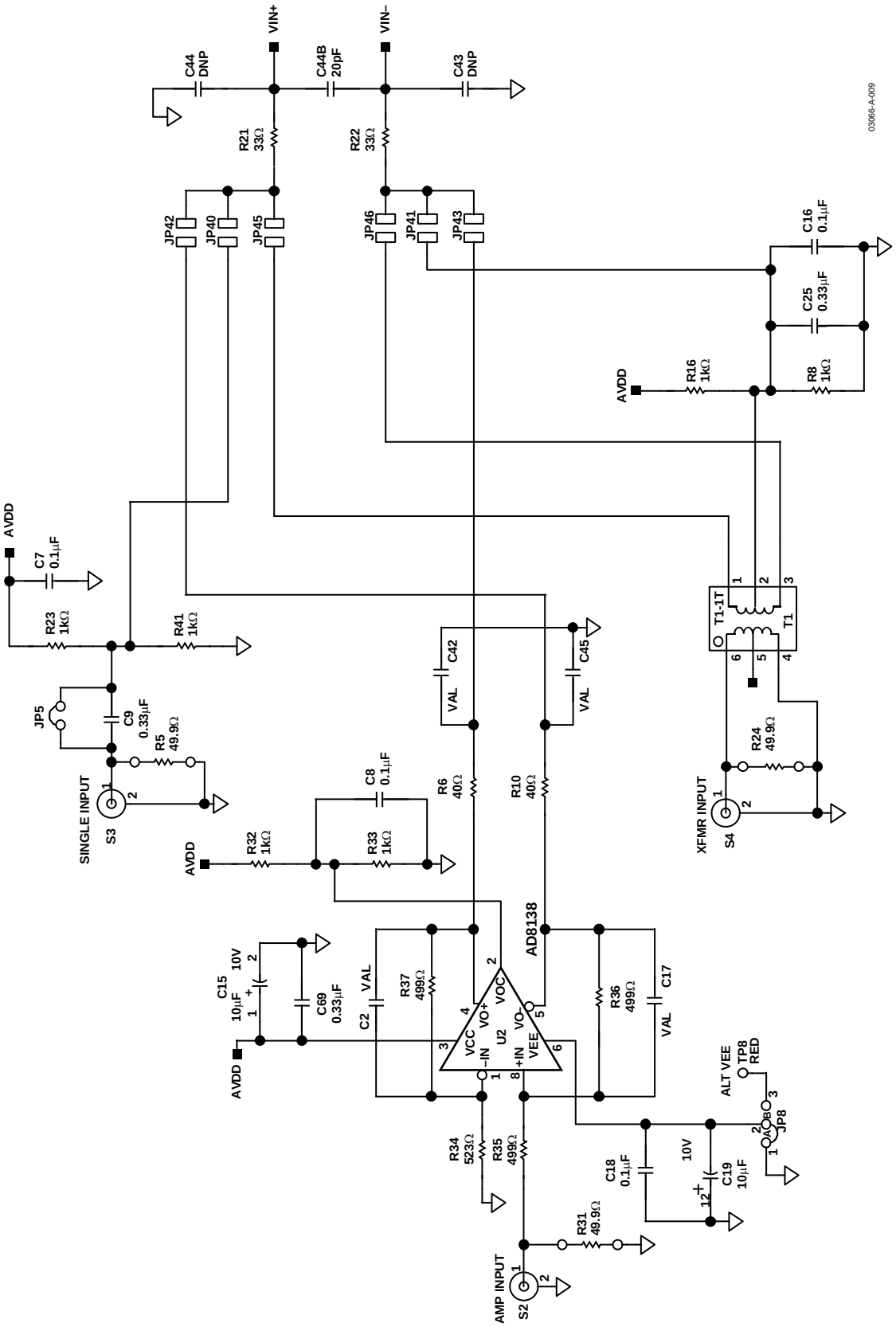

Figure 40. TSSOP Evaluation Board Schematic, Analog Inputs

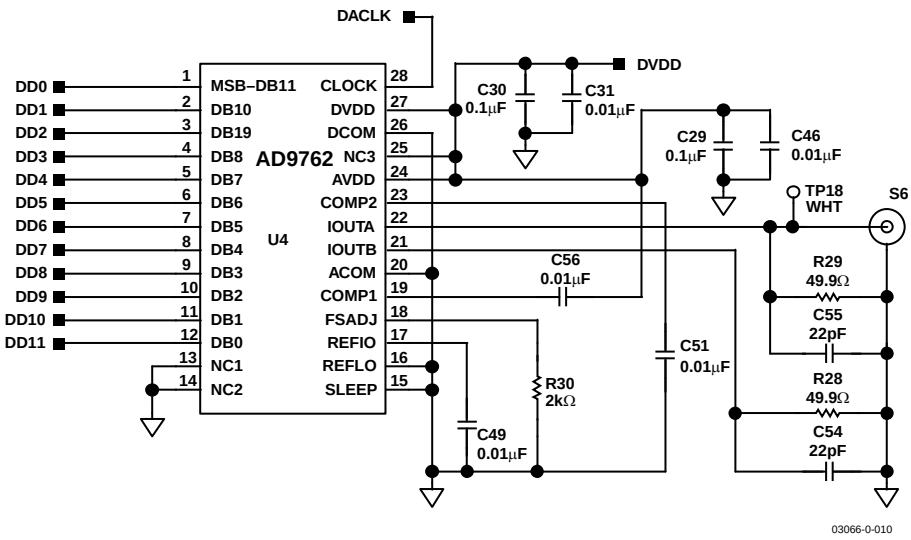

Figure 41. TSSOP Evaluation Board Schematic, Optional D/A Converter

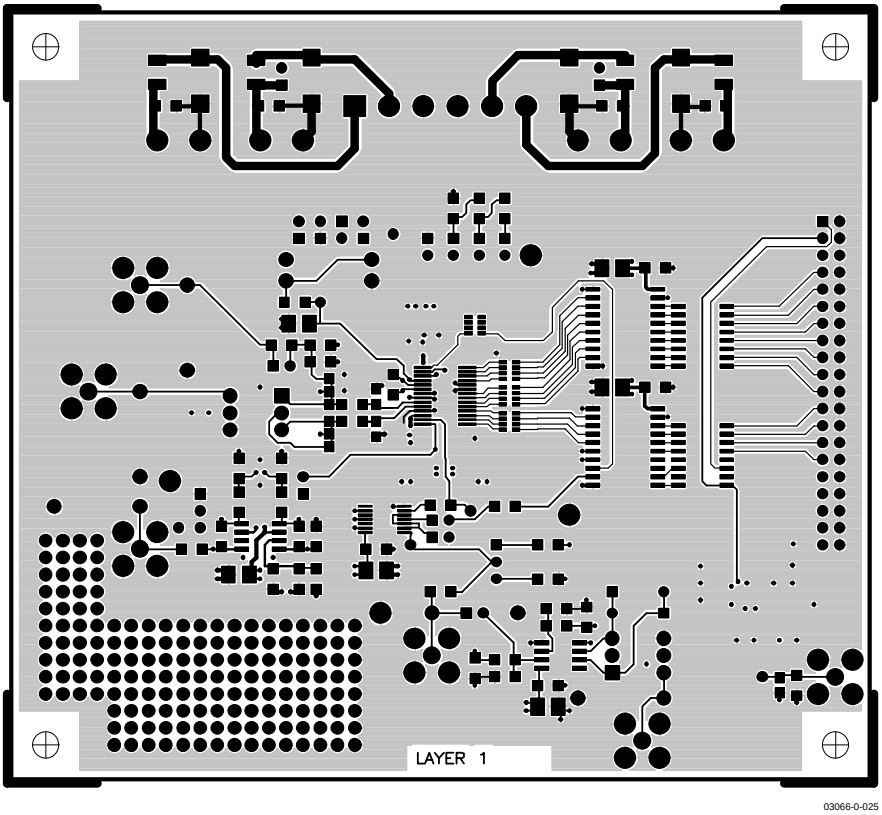

Figure 42. TSSOP Evaluation Board Layout, Primary Side

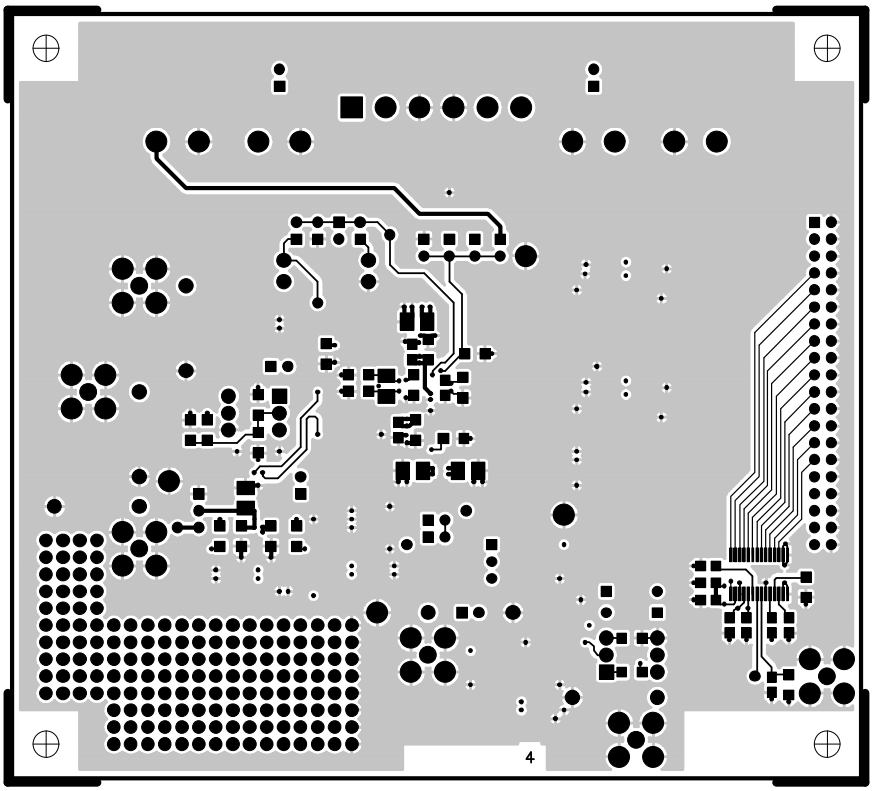

Figure 43. TSSOP Evaluation Board Layout, Secondary Side

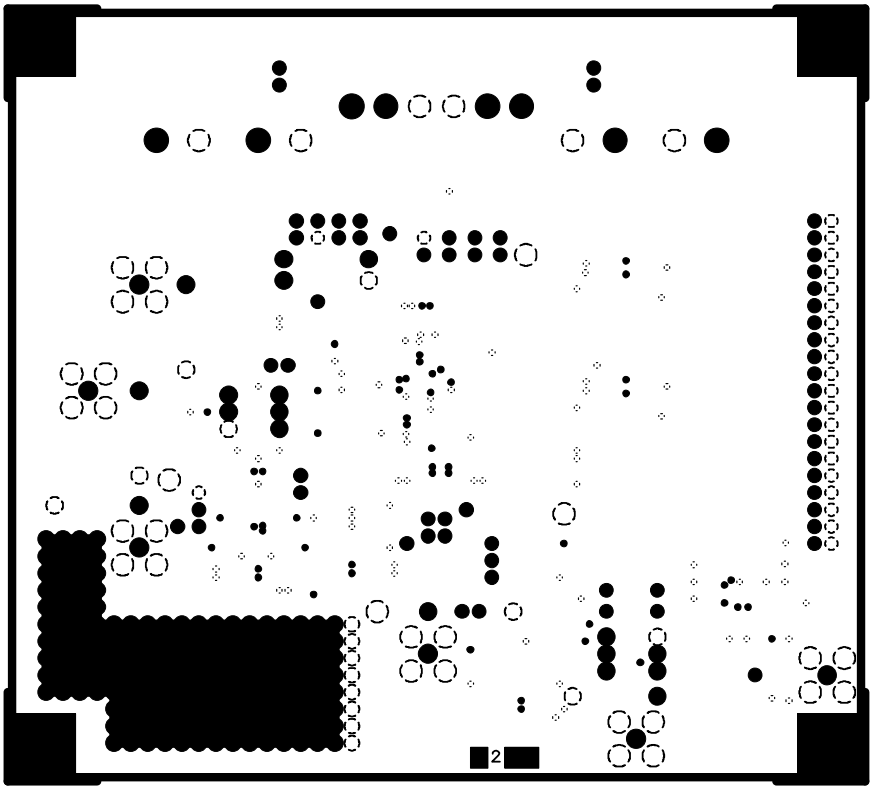

Figure 44. TSSOP Evaluation Board Layout, Ground Plane

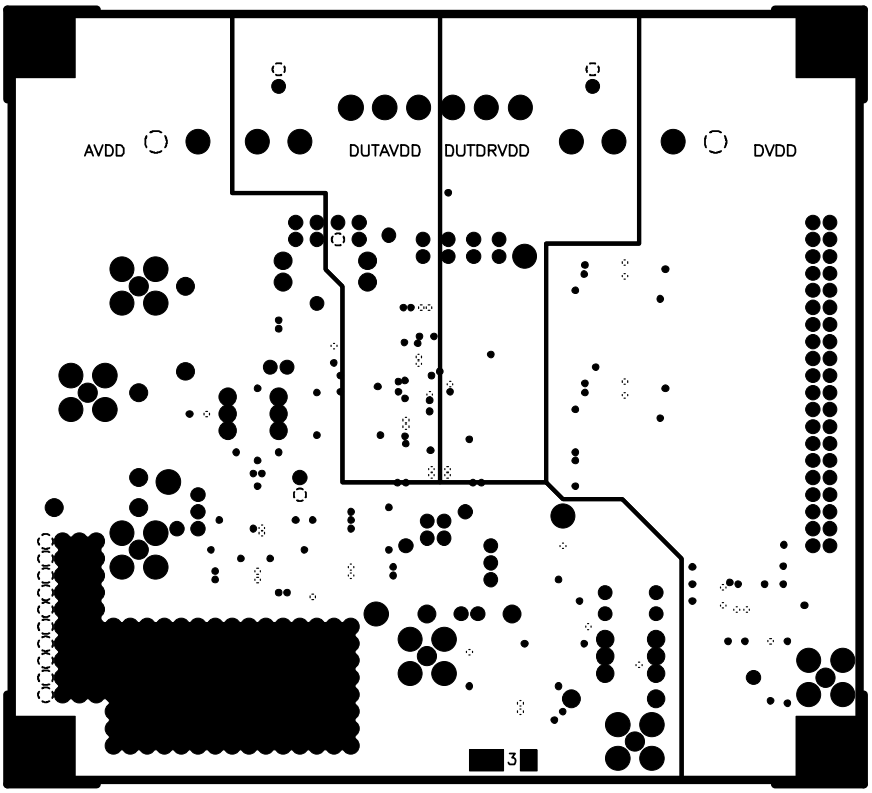

Figure 45. TSSOP Evaluation Board Layout, Power Plane

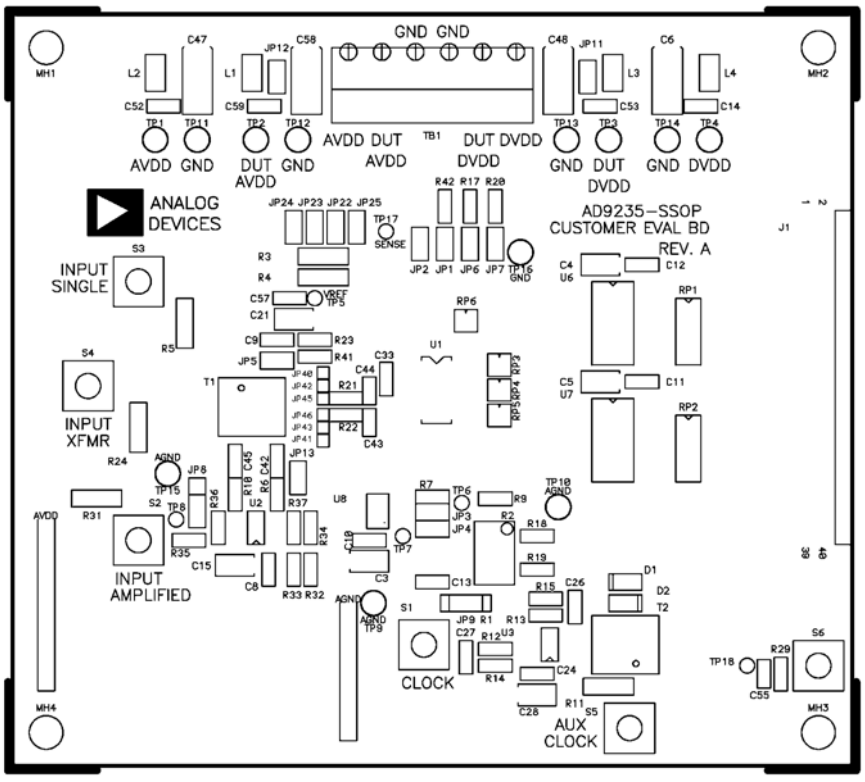

Figure 46. TSSOP Evaluation Board Layout, Primary Silkscreen

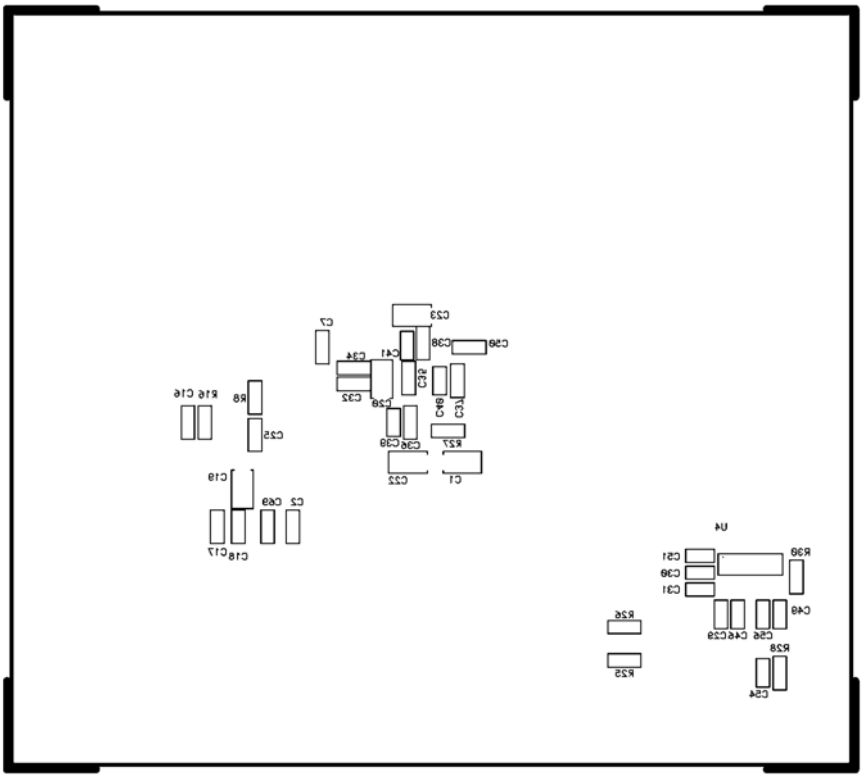

Figure 47. TSSOP Evaluation Board Layout, Secondary Silkscreen

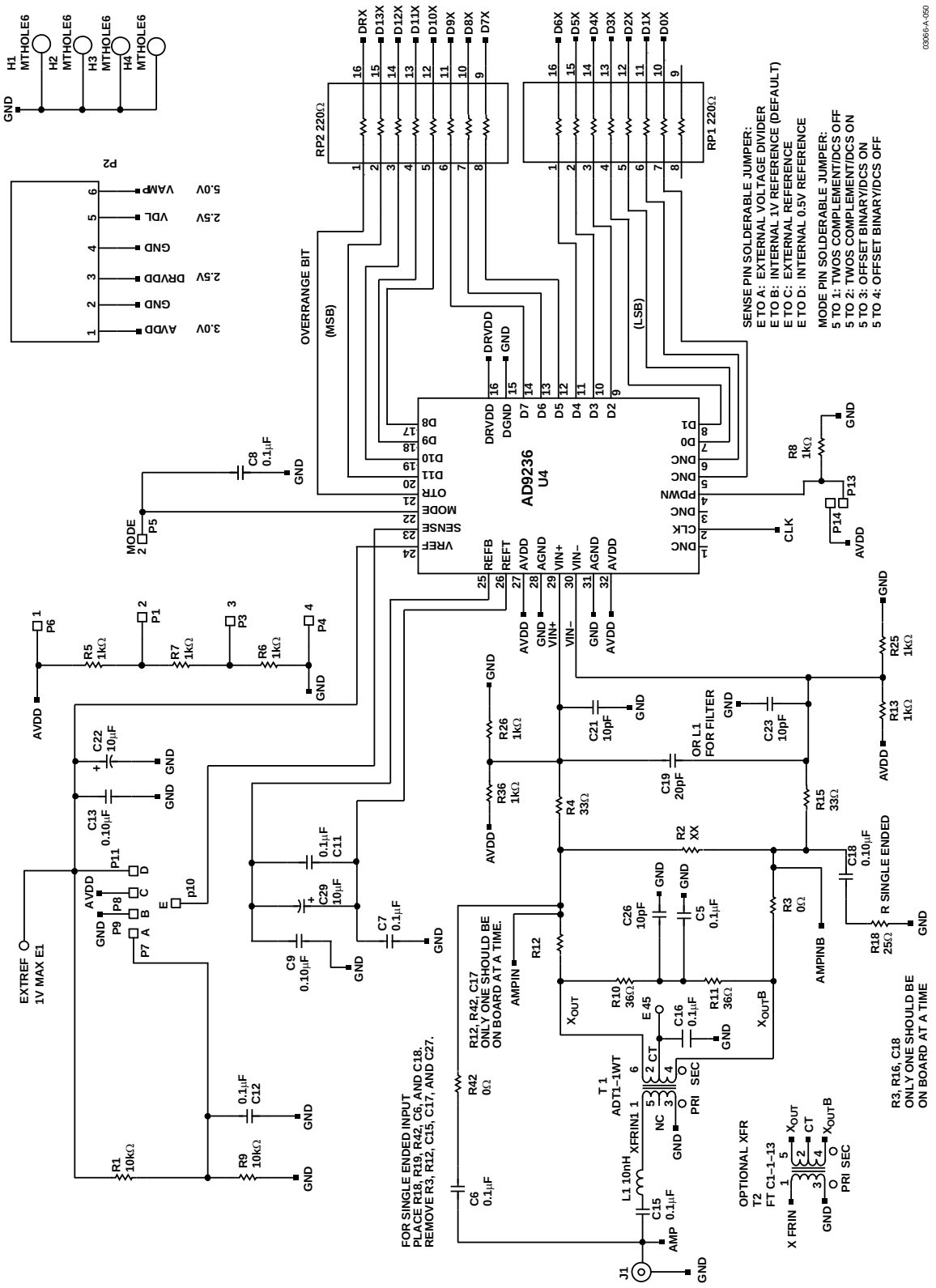

Figure 48. LFCSP Evaluation Board Schematic, Analog Inputs and DUT

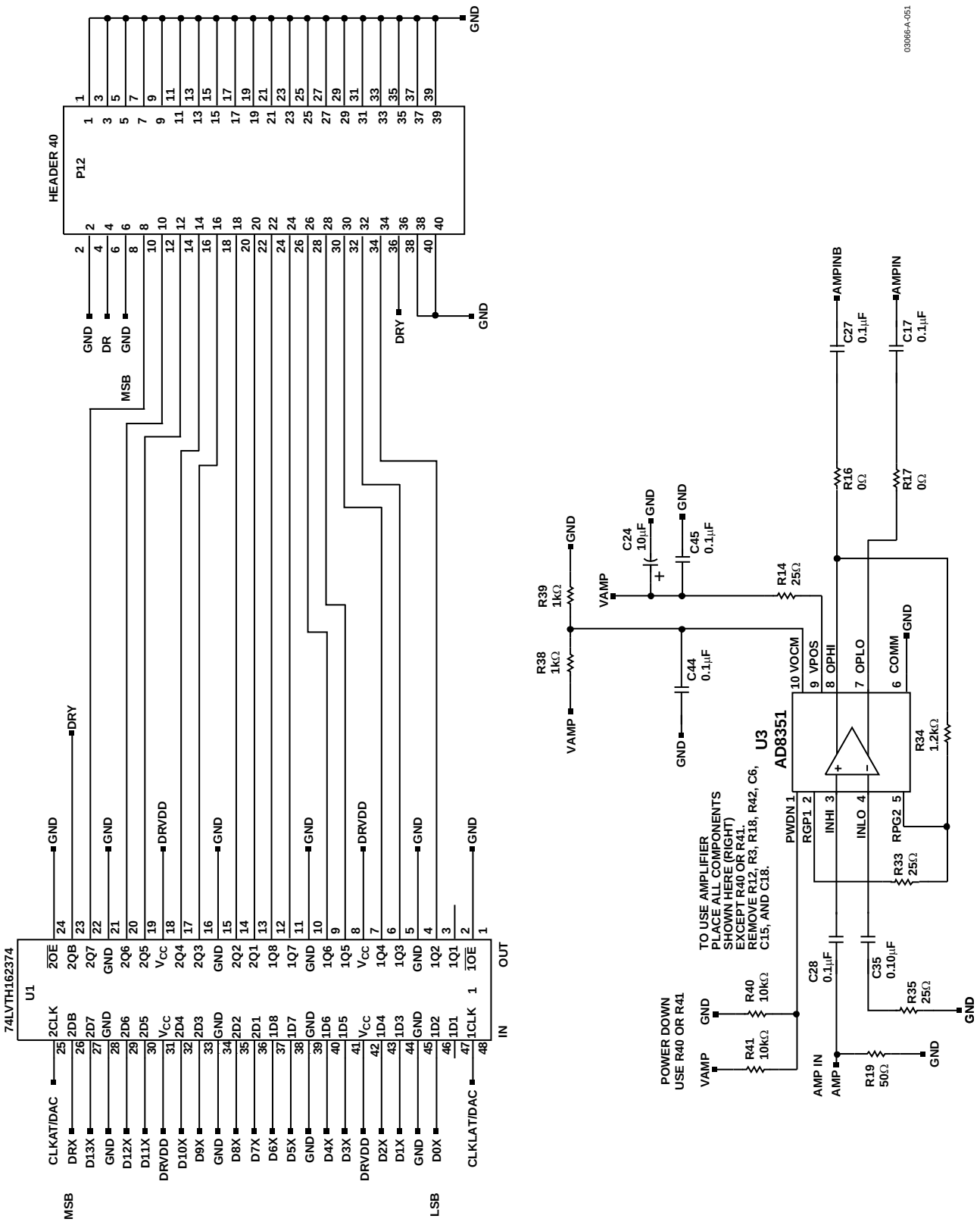

Figure 49. LFCSP Evaluation Board Schematic, Digital Path

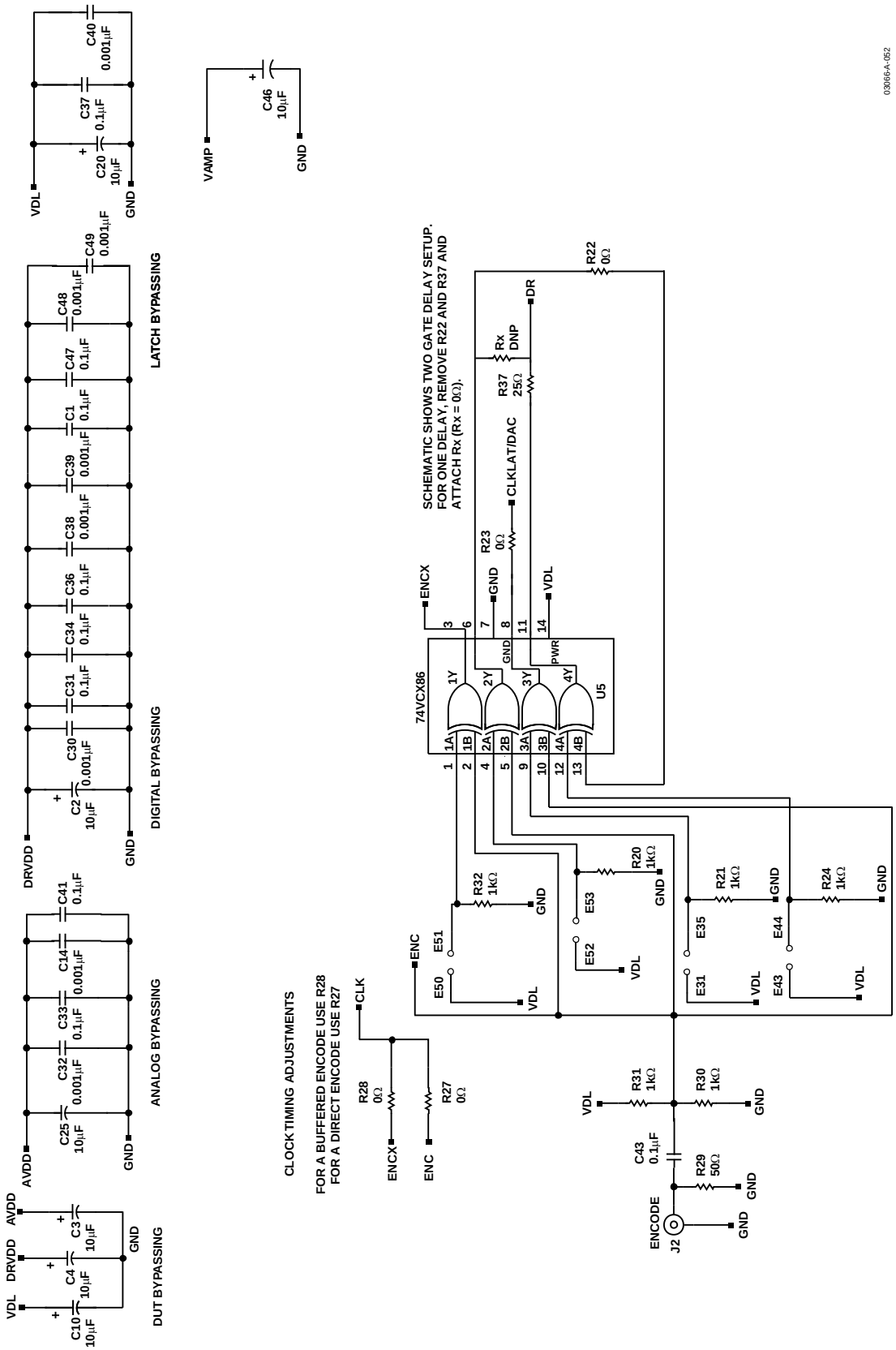

Figure 50. LFCSP Evaluation Board Schematic, Clock Input

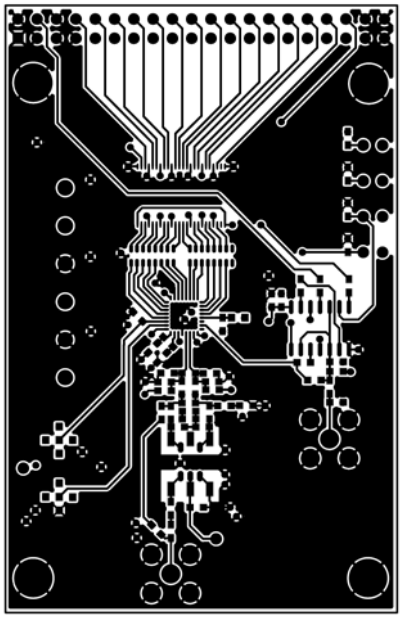

Figure 51. LFCSP Evaluation Board Layout, Primary Side

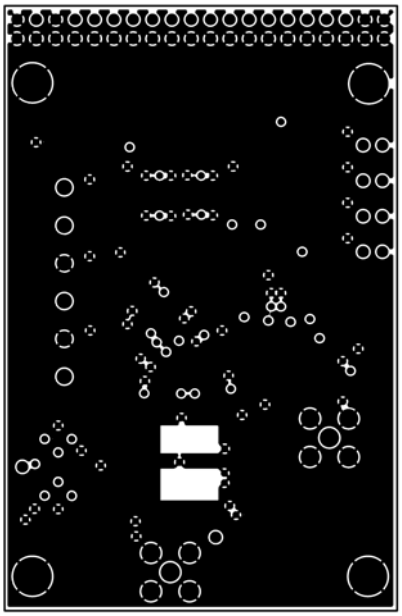

Figure 53. LFCSP Evaluation Board Layout, Ground Plane

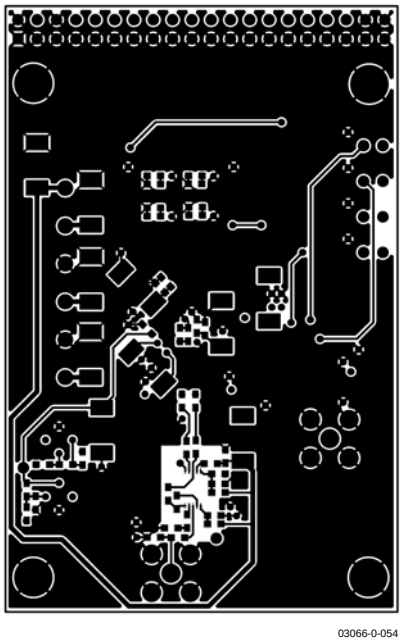

Figure 52. LFCSP Evaluation Board Layout, Secondary Side

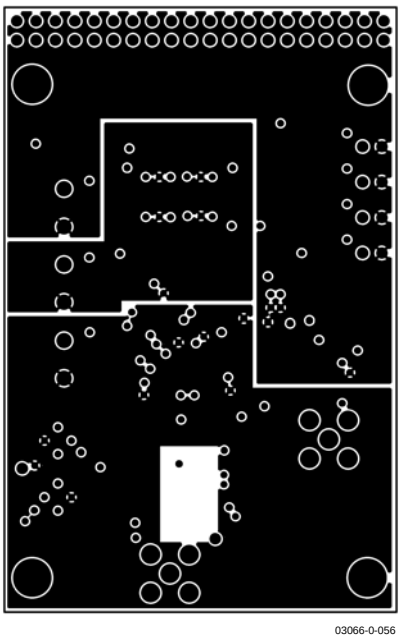

Figure 54. LFCSP Evaluation Board Layout, Power Plane

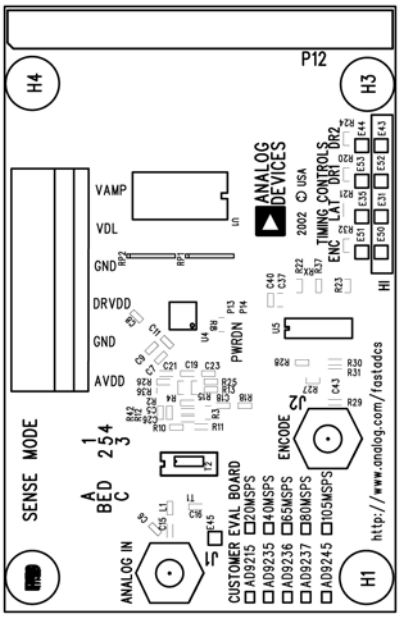

Figure 55. LFCSP Evaluation Board Layout, Primary Silkscreen

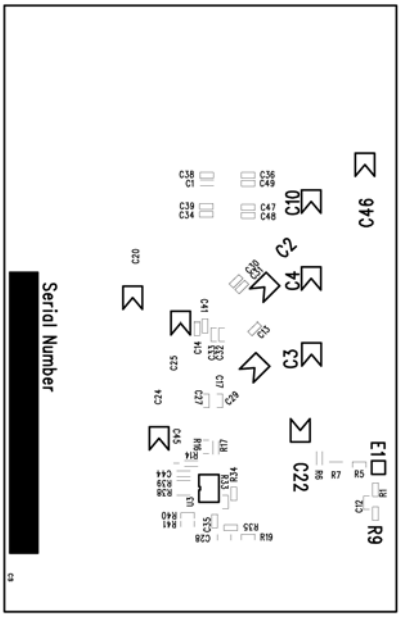

Figure 56. LFCSP Evaluation Board Layout, Secondary Silkscreen

Table 12. LFCSP Evaluation Board Bill of Materials

Item	Qty.	Omit[1]	Reference Designator	Device	Package	Value	Recommended Vendor/Part No.	Supplied by ADI
1	18		C1, C5, C7, C8, C9, C11, C12, C13, C15, C16, C31, C33, C34, C36, C37, C41, C43, C47	Chip Capacitors	0603	0.1 µF		
		8	C6, C18, C27, C17, C28, C35, C45, C44					
2	8		C2, C3, C4, C10, C20, C22, C25, C29	Tantalum Capacitors	TAJC	10 µF		
		2	C46, C24					
3	8		C14, C30, C32, C38, C39, C40, C48, C49	Chip Capacitors	0603	0.001 µF		
4	1		C19	Chip Capacitor	0603	20 pF		
5	1		C26	Chip Capacitors	0603	10 pF		
		2	C21, C23					
6	9		E31, E35, E43, E44, E50, E51, E52, E53	Headers	EHOLE		Jumper Blocks	
		2	E1, E45					
7	2		J1, J2	SMA Connectors/50 Ω	SMA			
8	1		L1	Inductor	0603	10 nH	Coilcraft/0603CS-10NXGBU	
9	1		P2	Terminal Block	TB6		Wieland/25.602.2653.0, z5-530-0625-0	
10	1		P12	Header Dual 20-Pin RT Angle	HEADER40		Digi-Key S2131-20-ND	
11	5		R3, R12, R23, R28, RX	Chip Resistors	0603	0 Ω		
		6	R37, R22, R42, R16, R17, R27					
12	2		R4, R15	Chip Resistors	0603	33 Ω		
13	14		R5, R6, R7, R8, R13, R20, R21, R24, R25, R26, R30, R31, R32, R36	Chip Resistors	0603	1 kΩ		
14	2		R10, R11	Chip Resistors	0603	36 Ω		
15	1		R29	Chip Resistor	0603	50 Ω		
		1	R19					
16	2		RP1, RP2	Resistor Pack	R_742	220 Ω	Digi-Key CTS/742C163221JTR	
17	1		T1	ADT1-1WT	AWT1-1T		Mini-Circuits	
18	1		U1	74LVTH162374 CMOS Register	TSSOP-48			
19	1		U4	AD9236BCP ADC (DUT)	CSP-32		Analog Devices, Inc.	X
20	1		U5	74VCX86M	SOIC-14		Fairchild	
21	1		PCB	AD92XXBCP/PCB	PCB		Analog Devices, Inc.	X
22		1	U3	AD8351 Op Amp	MSOP-8		Analog Devices, Inc.	X
23		1	T2	M/A-COM Transformer	ETC1-1-13	1-1 TX	M/A-COM/ETC1-1-13	
24		5	R9, R1, R2, R38, R39	Chip Resistors	0603	SELECT		
25		4	R18, R14, R33, R35	Chip Resistors	0603	25 Ω		
26		2	R40, R41	Chip Resistors	0603	10 kΩ		
27		1	R34	Chip Resistor		1.2 kΩ		
Total	81	35						

[1] These items are included in the PCB design, but are omitted at assembly.

OUTLINE DIMENSIONS

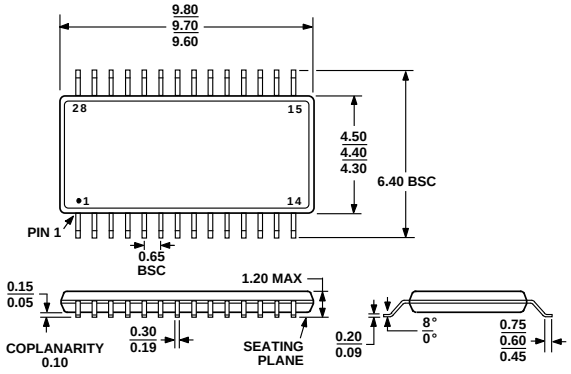

Figure 57. 28-Lead Thin Shrink Small Outline Package [TSSOP]
(RU-28)
Dimensions shown in millimeters

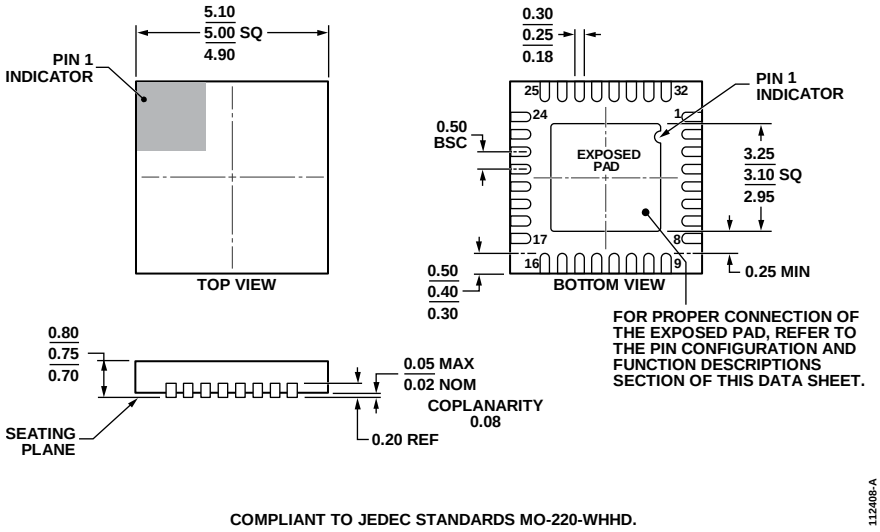

Figure 58. 32-Lead Frame Chip Scale Package [LFCSP_WQ]
5 mm × 5 mm Body, Very Very Thin Quad
(CP-32-7)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
AD9236BRUZ-80	−40°C to +85°C	28-Lead Thin Shrink Small Outline Package (TSSOP)	RU-28
AD9236BRUZRL7-80	−40°C to +85°C	28-Lead Thin Shrink Small Outline Package (TSSOP)	RU-28
AD9236BCPZ-80	−40°C to +85°C	32-Lead Lead Frame Chip Scale (LFCSP_WQ)	CP-32-7
AD9236BCPZRL7-80	−40°C to +85°C	32-Lead Lead Frame Chip Scale (LFCSP_WQ)	CP-32-7

[1] Z = RoHS Compliant Part.

NOTES

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D03066-0-2/13(C)