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REVISION HISTORY

5/09—Rev. A to Rev. B

Changes to Table 2.....	3
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4/09—Rev. 0 to Rev. A

Changes to Table 2.....	3
Changes to Ordering Guide	15

3/04—Revision 0: Initial Version

ELECTRICAL CHARACTERISTICS

10 k Ω , 50 k Ω , 100 k Ω versions: $V_{DD} = 3\text{ V} \pm 10\%$ or $5\text{ V} \pm 10\%$, $V_A = V_{DD}$, $V_B = 0\text{ V}$, $-40^\circ\text{C} < T_A < +105^\circ\text{C}$, unless otherwise noted.

Table 2.

Parameter	Symbol	Conditions	Min	Typ ¹	Max	Unit
DC CHARACTERISTICS RHEOSTAT MODE						
Resistor Differential Nonlinearity ²	R-DNL	R_{WB} , A = no connect	−0.5	±0.15	+0.5	LSB
Resistor Integral Nonlinearity ²	R-INL	R_{WB} , A = no connect	−1	±0.3	+1	LSB
Nominal Resistor Tolerance ³	$\Delta R_{AB}/R_{AB}$		−20		+20	%
Resistance Temperature Coefficient	$(\Delta R_{AB}/R_{AB})/\Delta T \times 10^6$			35		ppm/ $^\circ\text{C}$
Wiper Resistance	R_W	$V_{DD} = 2.7\text{ V}$ $V_{DD} = 2.8\text{ V to } 5.5\text{ V}$		100 50	250 200	Ω Ω
DC CHARACTERISTICS POTENTIOMETER DIVIDER MODE						
Resolution	N				6	Bits
Integral Nonlinearity ³	INL		−1	±0.1	+1	LSB
Differential Nonlinearity ^{3, 4}	DNL		−0.5	±0.1	+0.5	LSB
Voltage Divider Temperature Coefficient	$(\Delta V_W/V_W)/\Delta T \times 10^6$			5		ppm/ $^\circ\text{C}$
Full-Scale Error	V_{WFSSE}	Midscale $\geq +31$ steps from midscale $-40^\circ\text{C} < T_A < +60^\circ\text{C}$, $V_{DD} = 2.8\text{ V to } 5.5\text{ V}$	−1.2	−0.5	0	LSB
		≤ -32 steps from midscale $-40^\circ\text{C} < T_A < +60^\circ\text{C}$, $V_{DD} = 2.8\text{ V to } 5.5\text{ V}$	−1	−0.5	0	LSB
Zero-Scale Error	V_{WZSE}		0	0.5	1.2	LSB
			0	0.5	1	LSB
RESISTOR TERMINALS						
Voltage Range ⁵	$V_{A,B,W}$	With respect to GND	0		V_{DD}	V
Capacitance A, B ⁶	$C_{A,B}$	$f = 1\text{ MHz}$, measured to GND		140		pF
Capacitance W ⁶	C_W	$f = 1\text{ MHz}$, measured to GND		150		pF
Common-Mode Leakage	I_{CM}	$V_A = V_B = V_W$		1		nA
DIGITAL INPUTS ($\overline{CS}$, CLK, $\overline{U/D}$)						
Input Logic High	V_{IH}		2.4		5.5	V
Input Logic Low	V_{IL}		0		0.8	V
Input Current	I_I	$V_{IN} = 0\text{ V or } 5\text{ V}$			±1	μA
Input Capacitance ⁶	C_I			5		pF
POWER SUPPLIES						
Power Supply Range	V_{DD}		2.7		5.5	V
Supply Current	I_{DD}	$V_{IH} = 5\text{ V or } V_{IL} = 0\text{ V}$, $V_{DD} = 5\text{ V}$		0.4	3	μA
Power Dissipation ⁷	P_{DISS}	$V_{IH} = 5\text{ V or } V_{IL} = 0\text{ V}$, $V_{DD} = 5\text{ V}$			17	μW
Power Supply Sensitivity	PSSR	$V_{DD} = 5\text{ V} \pm 10\%$		0.01	0.05	%/%
DYNAMIC CHARACTERISTICS^{6, 8, 9}						
Bandwidth −3 dB	BW_10 k BW_50 k BW_100 k	$R_{AB} = 10\text{ k}\Omega$, midscale $R_{AB} = 50\text{ k}\Omega$, midscale $R_{AB} = 100\text{ k}\Omega$, midscale		460 100 50		kHz kHz kHz
Total Harmonic Distortion	THD	$V_A = 1\text{ V rms}$, $R_{AB} = 10\text{ k}\Omega$, $V_B = 0\text{ V dc}$, $f = 1\text{ kHz}$		0.05		%
Adjustment Settling Time	t_s	$V_A = 5\text{ V} \pm 1\text{ LSB error}$ band, $V_B = 0$, measured at V_W		1		μs
Resistor Noise Voltage	$e_{N_{WB}}$	$R_{WB} = 5\text{ k}\Omega$, $f = 1\text{ kHz}$		14		nV/ $\sqrt{\text{Hz}}$

Footnotes on the next page.

Parameter	Symbol	Conditions	Min	Typ ¹	Max	Unit
INTERFACE TIMING CHARACTERISTICS (applies to all parts ^{6, 10})						
Clock Frequency	f_{CLK}	Clock level high or low			50	MHz
Input Clock Pulse Width	t_{CH}, t_{CL}		10			ns
$\overline{CS}$ to CLK Setup Time	t_{CSS}		10			ns
$\overline{CS}$ Rise to CLK Hold Time	t_{CSH}		10			ns
$U/\overline{D}$ to Clock Fall Setup Time	t_{UDS}		10			ns

¹ Typicals represent average readings at 25°C, $V_{DD} = 5\text{ V}$.

² Resistor position nonlinearity error, R-INL, is the deviation from an ideal value measured between the maximum resistance and the minimum resistance wiper positions. R-DNL measures the relative step change from ideal between successive tap positions. Parts are guaranteed monotonic.

³ NL and DNL are measured at V_W with the RDAC configured as a potentiometer divider similar to a voltage output D/A converter. $V_A = V_{DD}$ and $V_B = 0\text{ V}$.

⁴ DNL specification limits of $\pm 1\text{ LSB}$ maximum are guaranteed monotonic operating conditions.

⁵ Resistor Terminals A, B, W have no limitations on polarity with respect to each other.

⁶ Guaranteed by design and not subject to production test.

⁷ P_{DISS} is calculated from $(I_{DD} \times V_{DD})$. CMOS logic level inputs result in minimum power dissipation.

⁸ Bandwidth, noise, and settling time are dependent on the terminal resistance value chosen. The lowest R value results in the fastest settling time and highest bandwidth. The highest R value results in the minimum overall power consumption.

⁹ All dynamic characteristics use $V_{DD} = 5\text{ V}$.

¹⁰ All input control voltages are specified with $t_R = t_F = 1\text{ ns}$ (10% to 90% of V_{DD}) and timed from a voltage level of 1.6 V. Switching characteristics are measured using $V_{DD} = 5\text{ V}$.

INTERFACE TIMING DIAGRAMS

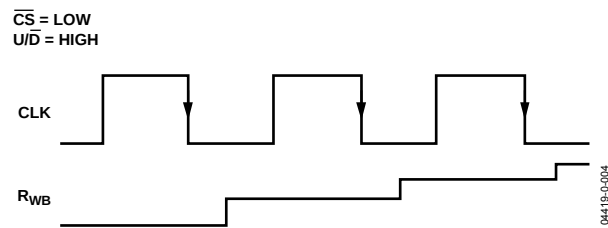


Figure 2. Increment R_{WB}

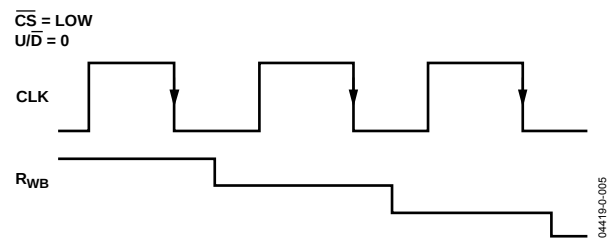


Figure 3. Decrement R_{WB}

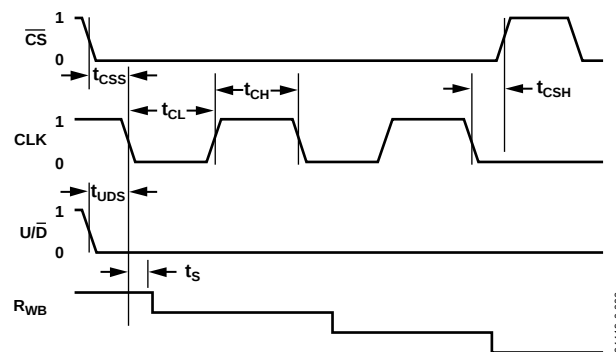


Figure 4. Detailed Timing Diagram (Only R_{WB} Decrement Shown)

ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Rating
V_{DD} to GND	−0.3 V, +7 V
V_A , V_B , V_W to GND	0 V, V_{DD}
Digital Input Voltage to GND ($\overline{CS}$, CLK, $U/\overline{D}$)	0 V, V_{DD}
Maximum Current	
I_{WB} , I_{WA} Pulsed	±20 mA
I_{WB} Continuous ($R_{WB} \leq 5 \text{ k}\Omega$, A open) ¹	±1 mA
I_{WA} Continuous ($R_{WA} \leq 5 \text{ k}\Omega$, B open) ¹	±1 mA
I_{AB} Continuous	±500 μA /
($R_{AB} = 10 \text{ k}\Omega/50 \text{ k}\Omega/100 \text{ k}\Omega$) ¹	±100 $\mu\text{A}/\pm 50 \mu\text{A}$
Operating Temperature Range	−40°C to +105°C
Maximum Junction Temperature (T_{Jmax})	150°C
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 10 s – 30 s)	245°C
Thermal Resistance ² θ_{JA}	230°C/W

¹ Maximum terminal current is bounded by the maximum applied voltage across any two of the A, B, and W terminals at a given resistance, the maximum current handling of the switches, and the maximum power dissipation of the package. $V_{DD} = 5 \text{ V}$.

² Package power dissipation = $(T_{Jmax} - T_A) / \theta_{JA}$.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



AD5227

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

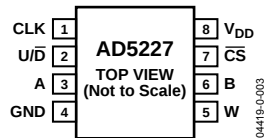


Figure 5. Pin Configuration

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	CLK	Clock Input. Each clock pulse executes the step-up or step-down of the resistance. The direction is determined by the state of the U/D pin. CLK is a negative-edge trigger. Logic high signal can be higher than V _{DD} , but lower than 5.5 V.
2	U/D	Up/Down Selections. Logic 1 selects up and Logic 0 selects down. U can be higher than V _{DD} , but lower than 5.5 V.
3	A	Resistor Terminal A. $GND \leq V_A \leq V_{DD}$.
4	GND	Common Ground.
5	W	Wiper Terminal W. $GND \leq V_W \leq V_{DD}$.
6	B	Resistor Terminal B. $GND \leq V_B \leq V_{DD}$.
7	CS	Chip Select. Active Low. Logic high signal can be higher than V _{DD} , but lower than 5.5 V.
8	V _{DD}	Positive Power Supply, 2.7 V to 5.5 V.

TYPICAL PERFORMANCE CHARACTERISTICS

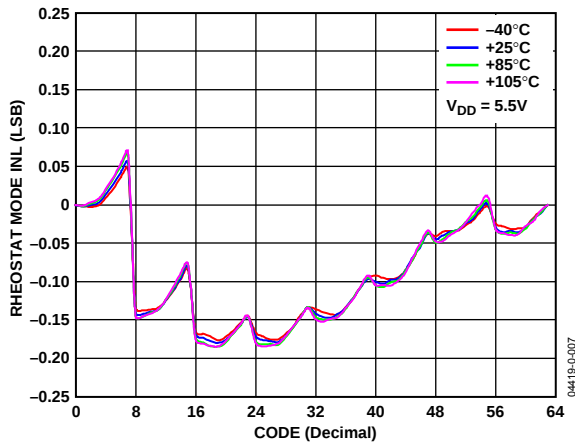


Figure 6. R-INL vs. Code vs. Temperature, $V_{DD} = 5\text{ V}$

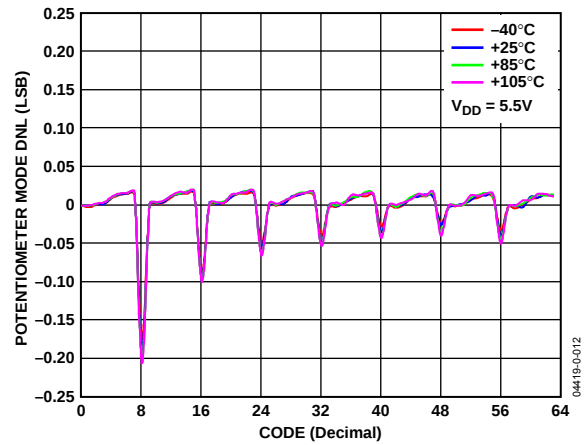


Figure 9. DNL vs. Code vs. Temperature, $V_{DD} = 5\text{ V}$

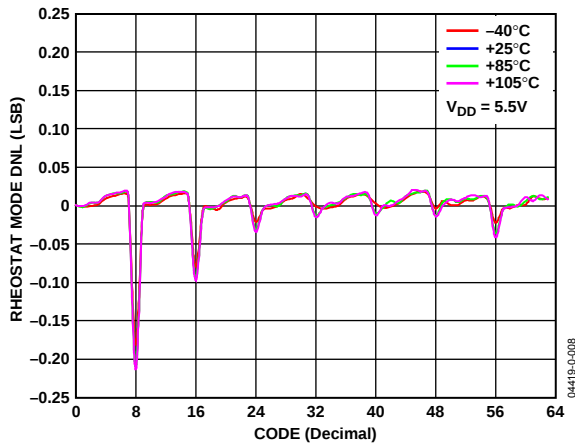


Figure 7. R-DNL vs. Code vs. Temperature, $V_{DD} = 5\text{ V}$

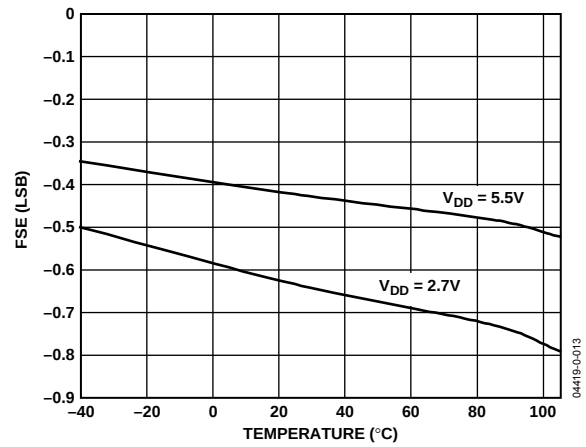


Figure 10. Full-Scale Error vs. Temperature

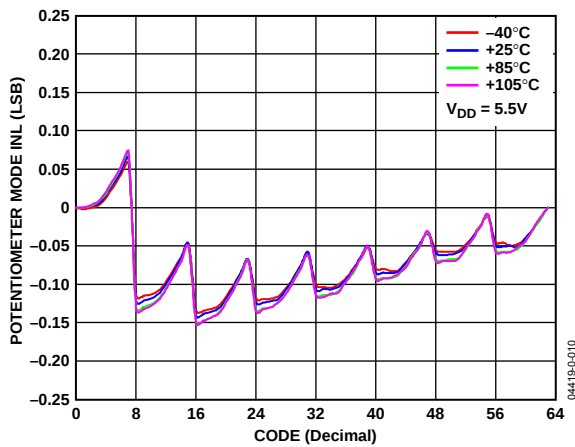


Figure 8. INL vs. Code, $V_{DD} = 5\text{ V}$

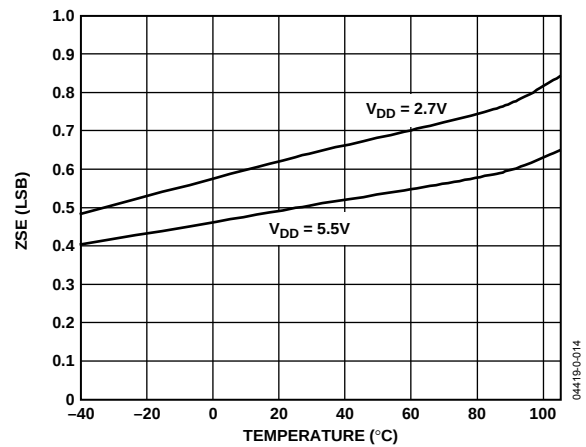


Figure 11. Zero-Scale Error vs. Temperature

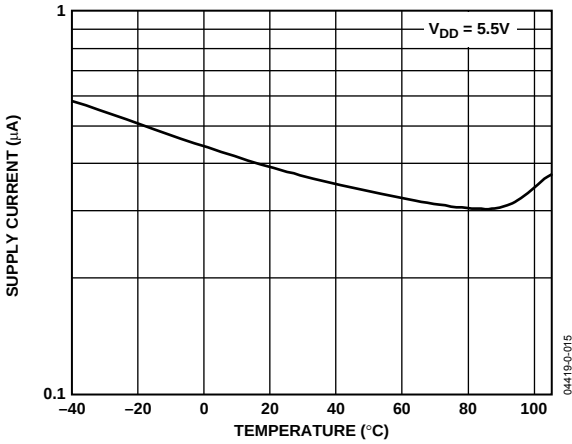


Figure 12. Supply Current vs. Temperature

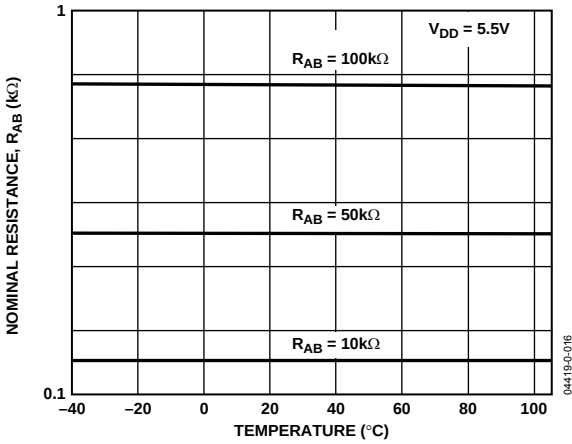


Figure 13. Nominal Resistance vs. Temperature

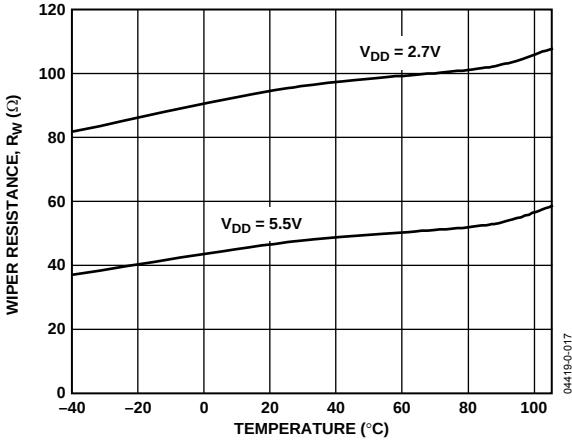


Figure 14. Wiper Resistance vs. Temperature

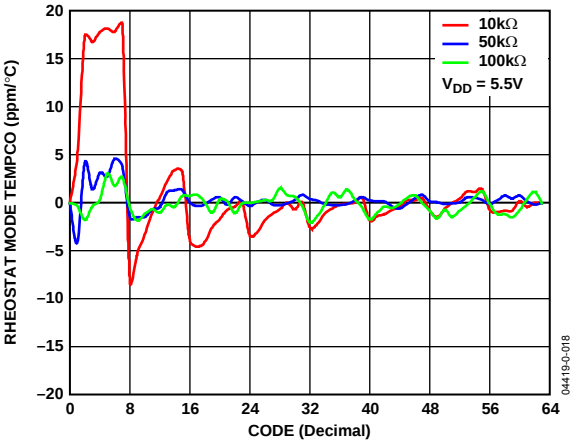


Figure 15. Rheostat Mode Tempco $\Delta R_{WB}/\Delta T$ vs. Code

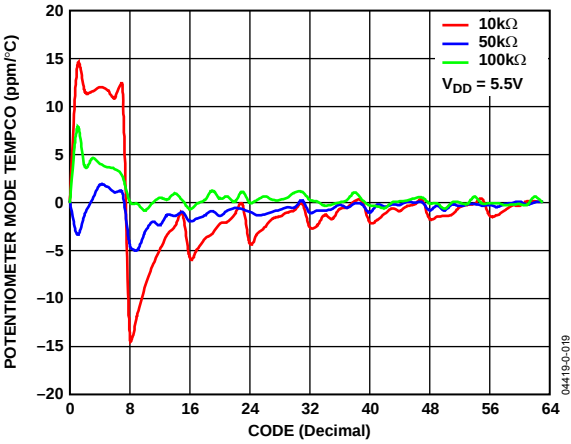


Figure 16. Potentiometer Mode Tempco $\Delta R_{WB}/\Delta T$ vs. Code

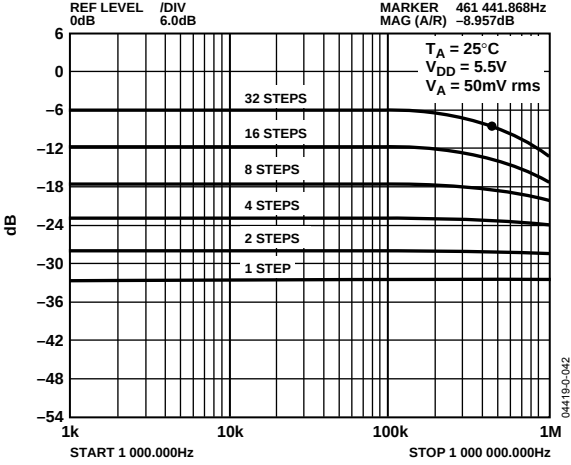


Figure 17. Gain vs. Frequency vs. Code, $R_{AB} = 10\text{ k}\Omega$

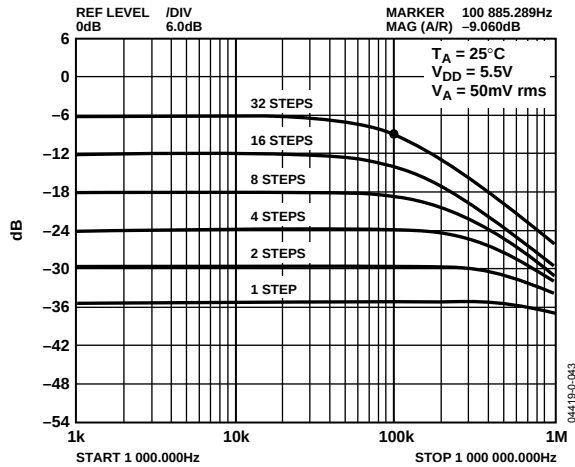
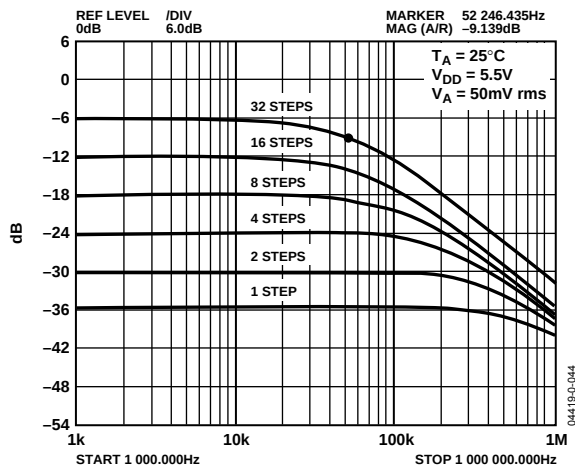
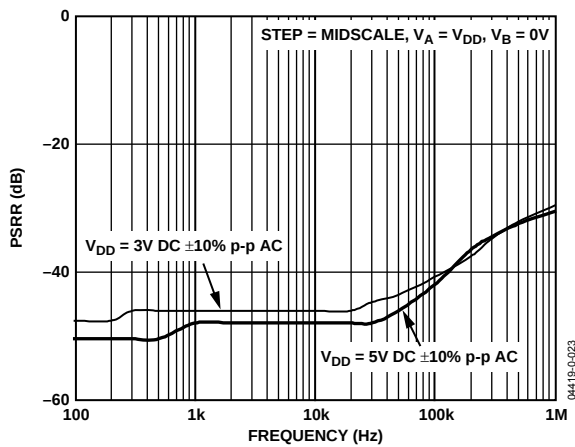
Figure 18. Gain vs. Frequency vs. Code, $R_{AB} = 50\text{ k}\Omega$ Figure 19. Gain vs. Frequency vs. Code, $R_{AB} = 100\text{ k}\Omega$ 

Figure 20. PSRR

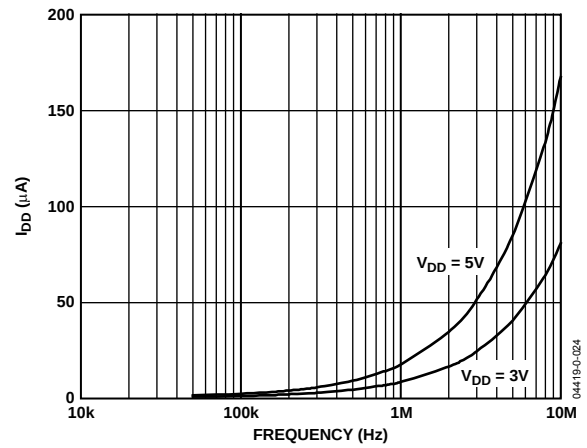
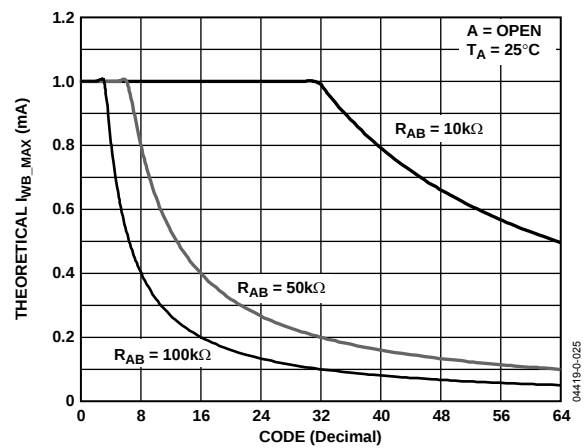
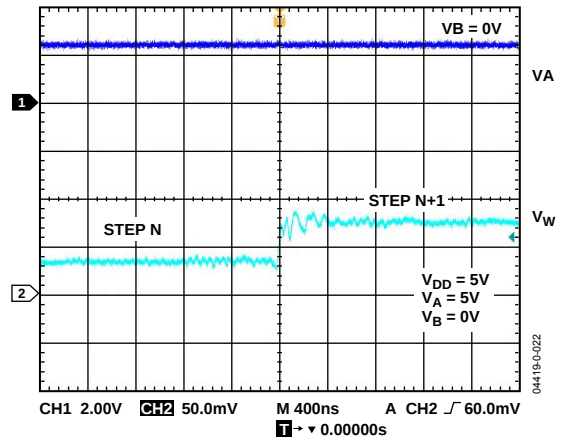
Figure 21. I_{DD} vs. CLK FrequencyFigure 22. Maximum I_{WB} vs. Code

Figure 23. Step Change Settling Time

The change of V_{WB} is known provided that the AD5227 has not reached the maximum or minimum scale. If one ignores the effect of the wiper resistance, the transfer functions can be simplified as

$$\Delta V_{WB} = +\frac{CP}{64}V_A \mid U/\overline{D} = 1 \quad (3)$$

$$\Delta V_{WB} = -\frac{CP}{64}V_A \mid U/\overline{D} = 0 \quad (4)$$

Unlike rheostat mode operation where the absolute tolerance is high, potentiometer mode operation yields an almost ratiometric function of $CP/64$ with a relatively small error contributed by the R_W term. The tolerance effect is, therefore, almost canceled. Although the thin film step resistor, R_s , and CMOS switches resistance, R_W , have very different temperature coefficients, the ratiometric adjustment also reduces the overall temperature coefficient to 5 ppm/°C except at low value codes where R_W dominates.

Potentiometer mode operation includes an op amp gain configuration among others. The A, W, and B terminals can be input or output terminals and have no polarity constraint provided that $|V_{AB}|$, $|V_{WA}|$, and $|V_{WB}|$ do not exceed V_{DD} -to-GND.

DIGITAL INTERFACE

The AD5227 contains a 3-wire serial input interface. The three inputs are clock (CLK), chip select ($\overline{CS}$), and up/down control ($U/\overline{D}$). These inputs can be controlled digitally for optimum speed and flexibility

When $\overline{CS}$ is pulled low, a clock pulse increments or decrements the up/down counter. The direction is determined by the state of the $U/\overline{D}$ pin. When a specific state of the $U/\overline{D}$ remains, the device continues to change in the same direction under consecutive clocks until it comes to the end of the resistance setting. All digital inputs, $\overline{CS}$, CLK, and $U/\overline{D}$ pins, are protected with a series input resistor and a parallel Zener ESD structure as shown in Figure 28.

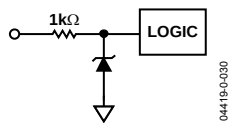


Figure 28. Equivalent ESD Protection Digital Pins

TERMINAL VOLTAGE OPERATION RANGE

The AD5227 is designed with internal ESD protection diodes (Figure 29), but the diodes also set the boundary of the terminal

operating voltages. Voltage present on Terminal A, B, or W that exceeds V_{DD} by more than 0.5 V is clamped by the diode and, therefore, elevates V_{DD} . There is no polarity constraint between V_{AB} , V_{WA} , and V_{WB} , but they cannot be higher than V_{DD} -to-GND.

POWER-UP AND POWER-DOWN SEQUENCES

Because of the ESD protection diodes, it is important to power on V_{DD} before applying any voltage to Terminals A, B, and W. Otherwise, the diodes are forward-biased such that V_{DD} can be powered unintentionally and can affect the rest of the system circuit. Similarly, V_{DD} should be powered down last. The ideal power-on sequence is in the following order: GND, V_{DD} , $V_{A/B/W}$, and digital inputs.

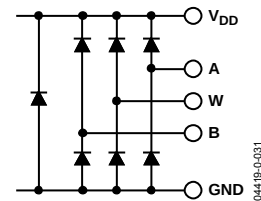


Figure 29. Maximum Terminal Voltages Set by V_{DD} and GND

LAYOUT AND POWER SUPPLY BIASING

It is a good practice to use compact, minimum lead length layout design. The leads to the input should be as direct as possible with a minimum conductor length. Ground paths should have low resistance and low inductance. It is also good practice to bypass the power supplies with quality capacitors. Low ESR (equivalent series resistance) 1 μ F to 10 μ F tantalum or electrolytic capacitors should be applied at the supplies to minimize any transient disturbance and filter low frequency ripple.

Figure 30 illustrates the basic supply bypassing configuration for the AD5227. The ground pin of the AD5227 is a digital ground reference that should be joined to the common ground at a single point to minimize the digital ground bounce.

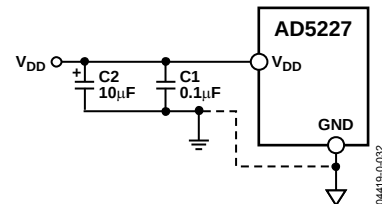


Figure 30. Power Supply Bypassing

APPLICATIONS

MANUAL CONTROL WITH TOGGLE AND PUSHBUTTON SWITCHES

The AD5227's simple interface allows it to be used with mechanical switches for simple manual operation. The states of the $\overline{CS}$ and $U/\overline{D}$ can be selected by toggle switches and the CLK input can be controlled by a pushbutton switch. Because of the numerous bounces due to contact closure, the pushbutton switch should be debounced by flip-flops or by the ADM812 as shown in Figure 31.

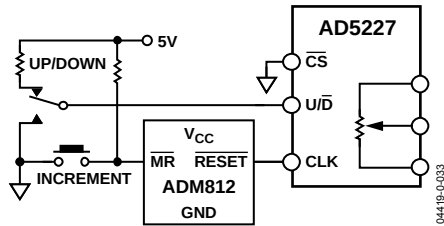


Figure 31. Manual Push Button Up/Down Control

MANUAL CONTROL WITH ROTARY ENCODER

Figure 32 shows another way of using AD5227 to emulate mechanical potentiometer in a rotary knob operation. The rotary encoder U1 has a C ground terminal and two out-of-phase signals, A and B. When U1 is turned clockwise, a pulse generated from the B terminal leads a pulse generated from the A terminal and vice versa. Signals A and B of U1 pass through a quadrature decoder U2 that translates the phase difference between A and B of U1 into compatible inputs for U3 AD5227. Therefore, when B leads A (clockwise), U2 provides the AD5227 with a logic high $U/\overline{D}$ signal, and vice versa. U2 also filters noise, jitter, and other transients as well as debouncing the contact bounces generated by U1.

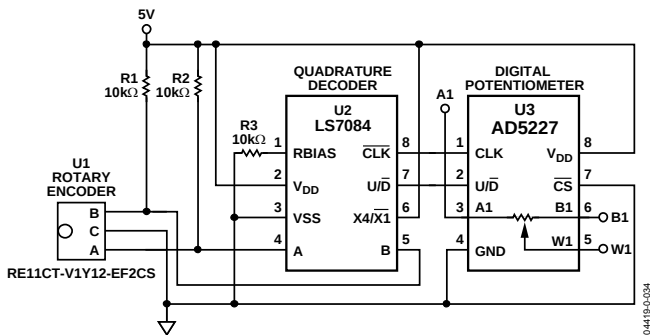


Figure 32. Manual Rotary Control

ADJUSTABLE LED DRIVER

The AD5227 can be used in many electronics-level adjustments such as LED drivers for LCD panel backlight control. Figure 33 shows an adjustable LED driver. The AD5227 sets the voltage across the white LED D1 for the brightness control. Since U2 handles up to 250 mA, a typical white LED with V_F of 3.5 V requires a resistor, R1, to limit the U2 current. This circuit is simple but not power-efficient, therefore the U2 shutdown pin can be toggled with a PWM signal to conserve power.

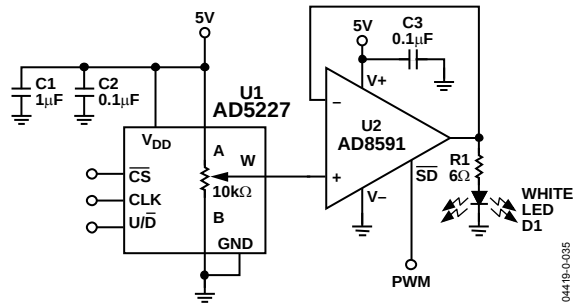


Figure 33. Low Cost Adjustable LED Driver

ADJUSTABLE CURRENT SOURCE FOR LED DRIVER

Since LED brightness is a function of current rather than forward voltage, an adjustable current source is preferred over a voltage source as shown in Figure 34.

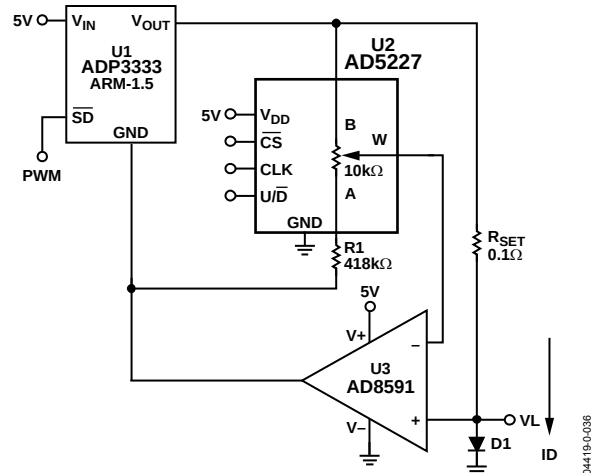


Figure 34. Adjustable Current Source for LED Driver

The load current can be found as the V_{WB} of the AD5227 divided by R_{SET} .

$$I_D = \frac{V_{WB}}{R_{SET}} \quad (5)$$

CONSTANT BIAS WITH SUPPLY TO RETAIN RESISTANCE SETTING

Users who consider EEMEM potentiometers but cannot justify the additional cost and programming for their designs can consider constantly biasing the AD5227 with the supply to retain the resistance setting as shown in Figure 38. The AD5227 is designed specifically with low power to allow power conservation even in battery-operated systems. As shown in Figure 39, a similar low power digital potentiometer is biased with a 3.4 V 450 mA/hour Li-Ion cell phone battery. The measurement shows that the device drains negligible power. Constantly biasing the potentiometer is a practical approach because most portable devices do not require detachable batteries for charging. Although the resistance setting of the AD5227 is lost when the battery needs to be replaced, this event occurs so infrequently that the inconvenience is minimal for most applications.

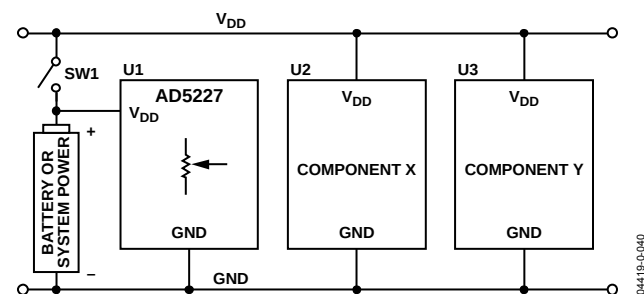


Figure 38. Constant Bias AD5227 for Resistance Retention

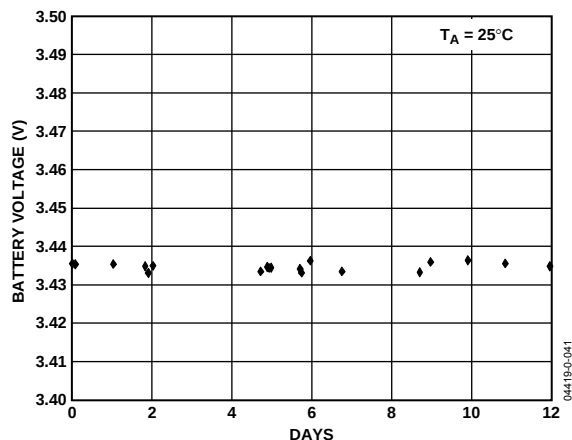
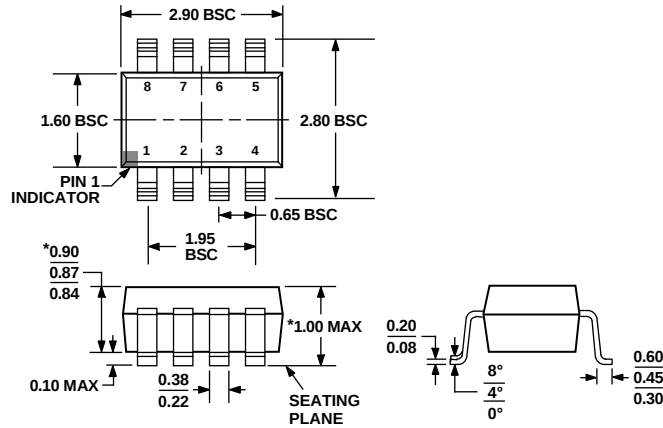


Figure 39. Battery Consumption Measurement

OUTLINE DIMENSIONS



*COMPLIANT TO JEDEC STANDARDS MO-193-BA WITH THE EXCEPTION OF PACKAGE HEIGHT AND THICKNESS.

Figure 40. 8-Lead Thin Small Outline Transistor Package [TSOT]
(UJ-8)
Dimensions shown in millimeters

ORDERING GUIDE

Model	R _{AB} ¹ (kΩ)	Temperature Range	Package Description	Package Option	Ordering Quantity	Branding
AD5227BUJZ10-RL7 ²	10	–40°C to +105°C	8-Lead TSOT	UJ-8	3000	D3G
AD5227BUJZ10-R2 ²	10	–40°C to +105°C	8-Lead TSOT	UJ-8	250	D3G
AD5227BUJZ50-RL7 ²	50	–40°C to +105°C	8-Lead TSOT	UJ-8	3000	D3H
AD5227BUJZ50-R2 ²	50	–40°C to +105°C	8-Lead TSOT	UJ-8	250	D3H
AD5227BUJZ100-RL7 ²	100	–40°C to +105°C	8-Lead TSOT	UJ-8	3000	D3J
AD5227BUJZ100-R2 ²	100	–40°C to +105°C	8-Lead TSOT	UJ-8	250	D3J
AD5227EVAL	10		Evaluation Board		1	

¹ The end-to-end resistance R_{AB} is available in 10 kΩ, 50 kΩ, and 100 kΩ versions. The final three characters of the part number determine the nominal resistance value, for example, 10 kΩ = 10.

² Z = RoHS Compliant Part.

AD5227

NOTES