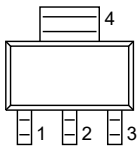
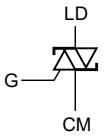
Symbol	Parameter	Conditions		Min	Typ	Max	Unit
		full sine wave; $T_{j(init)}$ = 25 °C; t_p = 16.7 ms		-	-	20	A
T_j	junction temperature			-	-	150	°C
V_{PP}	peak pulse voltage	T_j = 25 °C; non-repetitive, off-state; Fig. 6		-	-	2	kV
Static characteristics							
I_{GT}	gate trigger current	V_D = 12 V; I_T = 100 mA; LD+ G+; T_j = 25 °C; Fig. 8		-	-	10	mA
		V_D = 12 V; I_T = 100 mA; LD+ G-; T_j = 25 °C; Fig. 8		-	-	10	mA
		V_D = 12 V; I_T = 100 mA; LD- G-; T_j = 25 °C; Fig. 8		-	-	10	mA
I_H	holding current	V_D = 12 V; T_j = 25 °C; Fig. 10		-	-	10	mA
V_T	on-state voltage	I_T = 3 A; T_j = 25 °C; Fig. 11		-	-	2	V
V_{CL}	clamping voltage	I_{CL} = 0.1 mA; t_p = 1 ms; T_j = 25 °C		850	-	-	V
Dynamic characteristics							
dV_D/dt	rate of rise of off-state voltage	V_{DM} = 536 V; T_j = 125 °C; (V_{DM} = 67% of V_{DRM}); exponential waveform; gate open circuit		500	-	-	V/µs
		V_{DM} = 536 V; T_j = 150 °C; exponential waveform; gate open circuit		200	-	-	V/µs
dI_{com}/dt	rate of change of commutating current	V_D = 400 V; T_j = 150 °C; $I_{T(RMS)}$ = 2 A; dV_{com}/dt = 20 V/µs; gate open circuit; snubberless condition		1	-	-	A/ms
		V_D = 400 V; T_j = 150 °C; $I_{T(RMS)}$ = 2 A; dV_{com}/dt = 10 V/µs; gate open circuit		1.5	-	-	A/ms
		V_D = 400 V; T_j = 150 °C; $I_{T(RMS)}$ = 2 A; dV_{com}/dt = 1 V/µs; gate open circuit		3	-	-	A/ms

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	CM	common	 SC-73 (SOT223)	 003aaf296
2	LD	load		
3	G	gate		
mb	mb	mounting base; connected to load		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
ACTT2W-800ETN	SC-73	plastic surface-mounted package with increased heatsink; 4 leads	SOT223

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DRM}	repetitive peak off-state voltage			-	800	V
$I_{T(RMS)}$	RMS on-state current	full sine wave; $T_{sp} \leq$ 106 °C; Fig. 1; Fig. 2; Fig. 3		-	2	A
I_{TSM}	non-repetitive peak on-state current	full sine wave; $T_{j(init)}$ = 25 °C; t_p = 20 ms; Fig. 4; Fig. 5		-	18	A
		full sine wave; $T_{j(init)}$ = 25 °C; t_p = 16.7 ms		-	20	A
I^2t	I^2t for fusing	t_p = 10 ms; sine-wave pulse		-	1.6	A²s
dI_T/dt	rate of rise of on-state current	I_G = 20 mA		-	100	A/µs
I_{GM}	peak gate current			-	2	A
P_{GM}	peak gate power			-	5	W
$P_{G(AV)}$	average gate power	over any 20 ms period		-	0.5	W
T_{stg}	storage temperature			-40	150	°C
T_j	junction temperature			-	150	°C
V_{PP}	peak pulse voltage	T_j = 25 °C; non-repetitive, off-state; Fig. 6		-	2	kV

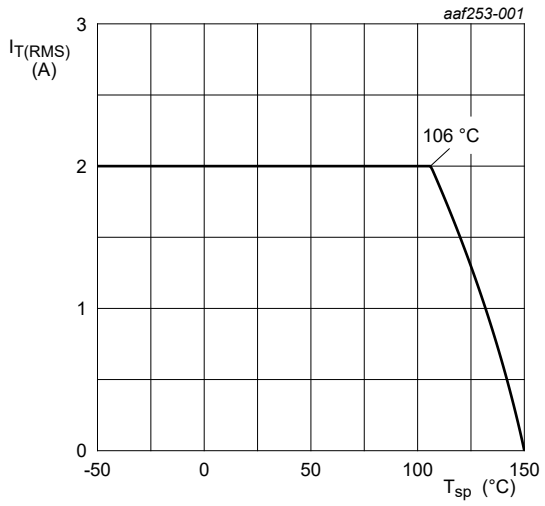
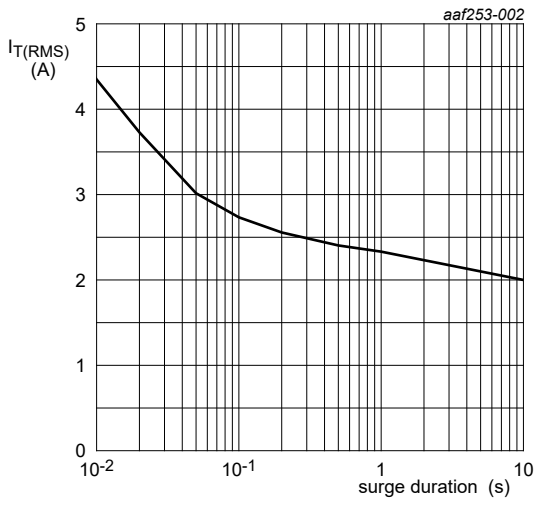
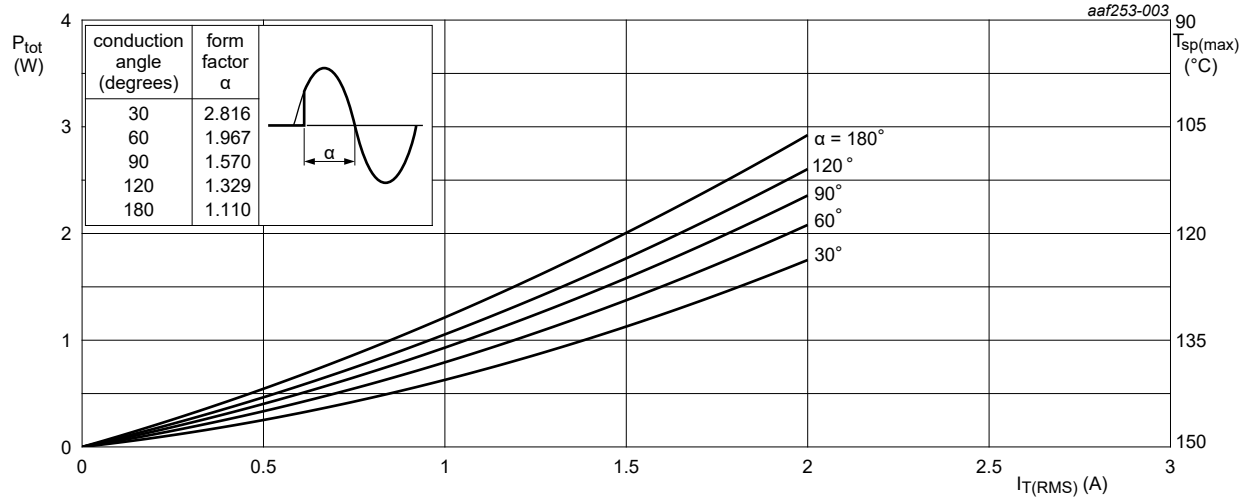


Fig. 1. RMS on-state current as a function of solder point temperature; maximum values



f = 50 Hz; T_{sp} = 106 °C

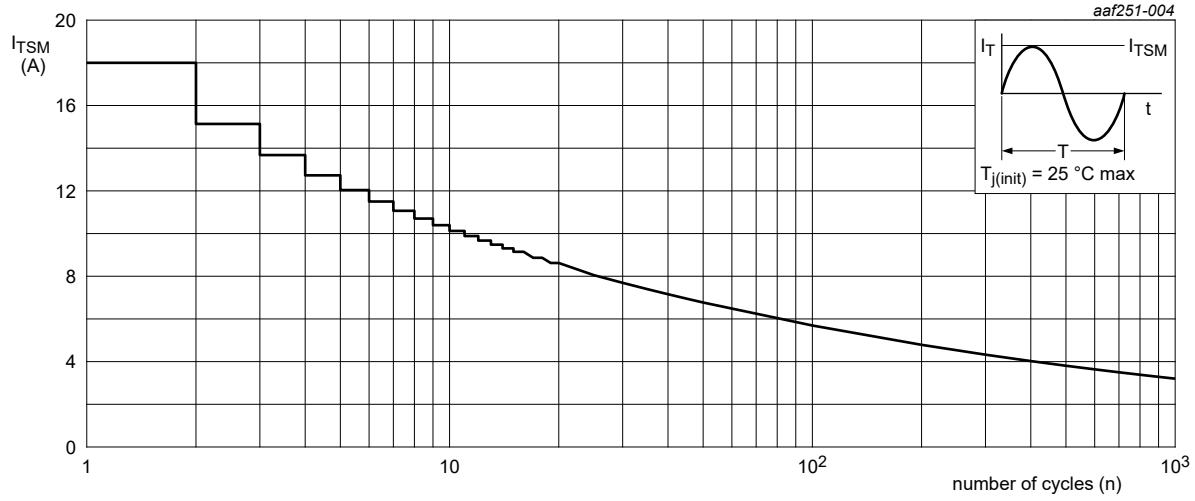
Fig. 2. RMS on-state current as a function of surge duration; maximum values



α = conduction angle

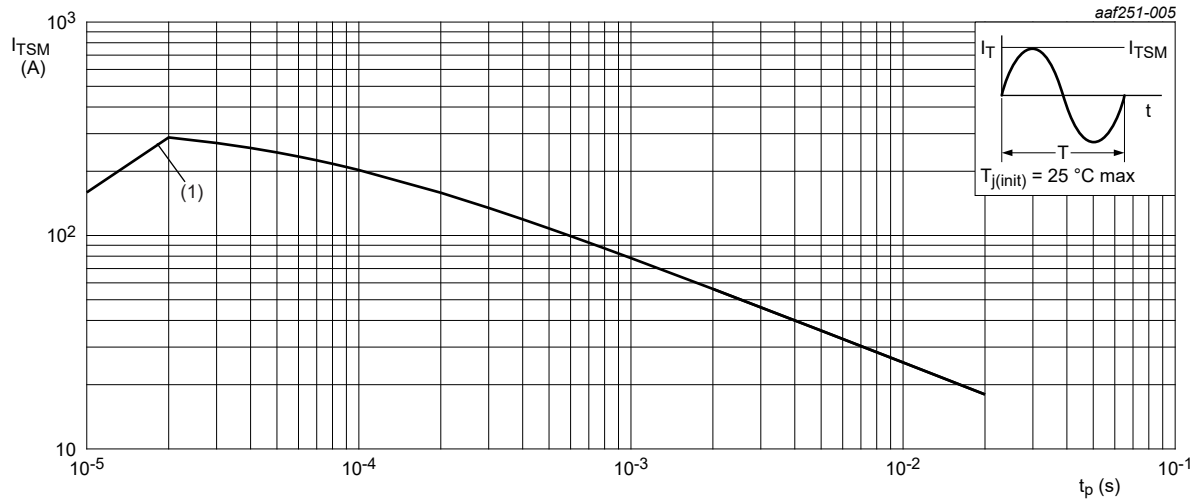
a = form factor = $I_{T(RMS)}$ / $I_{T(AV)}$

Fig. 3. Total power dissipation as a function of RMS on-state current; maximum values



f = 50 Hz

Fig. 4. Non-repetitive peak on-state current as a function of the number of sinusoidal current cycles; maximum values



$t_p \leq 20$ ms

(1) dI_T/dt limit

Fig. 5. Non-repetitive peak on-state current as a function of pulse width; maximum values

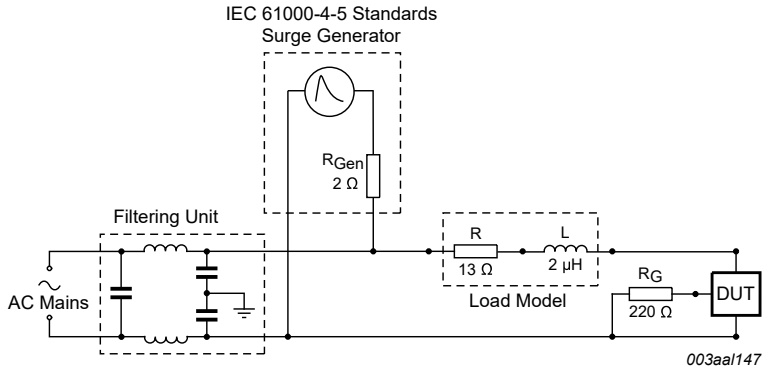


Fig. 6. Test circuit for inductive and resistive loads with conditions equivalent to IEC 61000-4-5

8. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$R_{th(j-sp)}$	thermal resistance from junction to solder point	Fig. 7		-	-	15	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient free air	Full cycle; printed-circuit board mounted for pad area		-	70	-	K/W
		Full cycle; printed-circuit board mounted for minimum footprint		-	156	-	K/W

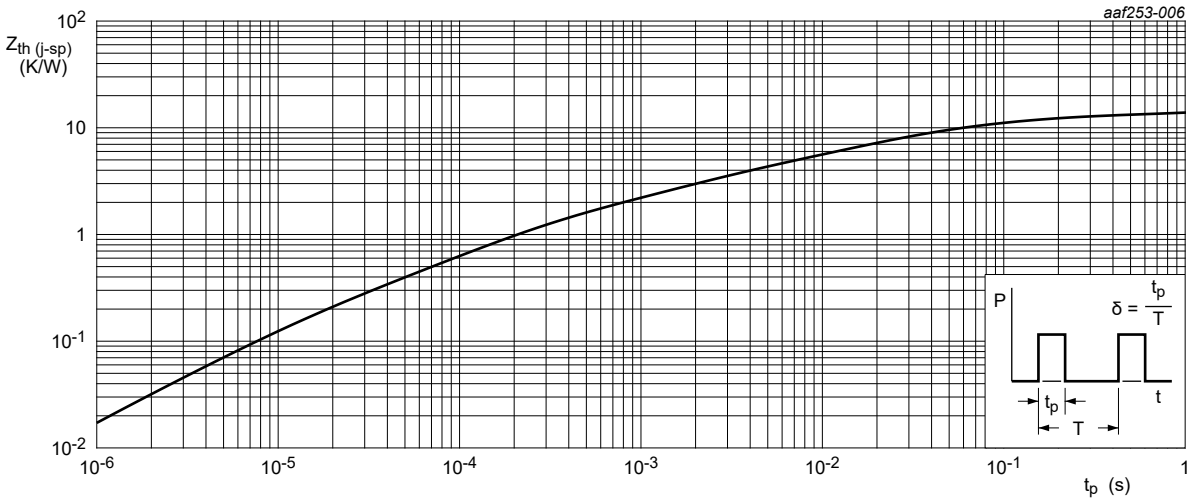
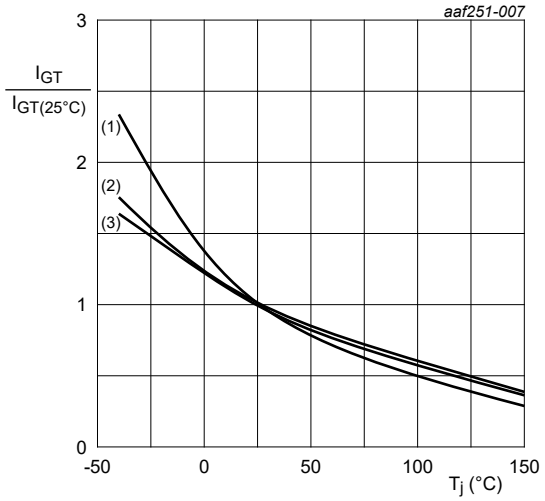


Fig. 7. Transient thermal impedance from junction to solder point as a function of pulse duration

9. Characteristics

Table 6. Characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Static characteristics							
I_{GT}	gate trigger current	V_D = 12 V; I_T = 100 mA; LD+ G+; T_j = 25 °C; Fig. 8		-	-	10	mA
		V_D = 12 V; I_T = 100 mA; LD+ G-; T_j = 25 °C; Fig. 8		-	-	10	mA
		V_D = 12 V; I_T = 100 mA; LD- G-; T_j = 25 °C; Fig. 8		-	-	10	mA
I_L	latching current	V_D = 12 V; I_G = 100 mA; LD+ G+; T_j = 25 °C; Fig. 9		-	-	25	mA
		V_D = 12 V; I_G = 100 mA; LD+ G-; T_j = 25 °C; Fig. 9		-	-	35	mA
		V_D = 12 V; I_G = 100 mA; LD- G-; T_j = 25 °C; Fig. 9		-	-	25	mA
I_H	holding current	V_D = 12 V; T_j = 25 °C; Fig. 10		-	-	10	mA
V_T	on-state voltage	I_T = 3 A; T_j = 25 °C; Fig. 11		-	-	2	V
V_{GT}	gate trigger voltage	V_D = 12 V; I_T = 100 mA; T_j = 25 °C; Fig. 12		-	0.8	1	V
		V_D = 400 V; I_T = 100 mA; T_j = 150 °C; Fig. 12		0.2	0.5	-	V
I_D	off-state current	V_D = 800 V; T_j = 25 °C		-	-	10	µA
		V_D = 800 V; T_j = 150 °C		-	-	2	mA
V_{CL}	clamping voltage	I_{CL} = 0.1 mA; t_p = 1 ms; T_j = 25 °C		850	-	-	V
Dynamic characteristics							
dV_D/dt	rate of rise of off-state voltage	V_{DM} = 536 V; T_j = 125 °C; (V_{DM} = 67% of V_{DRM}); exponential waveform; gate open circuit		500	-	-	V/µs
		V_{DM} = 536 V; T_j = 150 °C; exponential waveform; gate open circuit		200	-	-	V/µs
dI_{com}/dt	rate of change of commutating current	V_D = 400 V; T_j = 150 °C; $I_{T(RMS)}$ = 2 A; dV_{com}/dt = 20 V/µs; gate open circuit; snubberless condition		1	-	-	A/ms
		V_D = 400 V; T_j = 150 °C; $I_{T(RMS)}$ = 2 A; dV_{com}/dt = 10 V/µs; gate open circuit		1.5	-	-	A/ms
		V_D = 400 V; T_j = 150 °C; $I_{T(RMS)}$ = 2 A; dV_{com}/dt = 1 V/µs; gate open circuit		3	-	-	A/ms



(1) LD- G-
(2) LD+ G-
(3) LD+ G+

Fig. 8. Normalized gate trigger current as a function of junction temperature

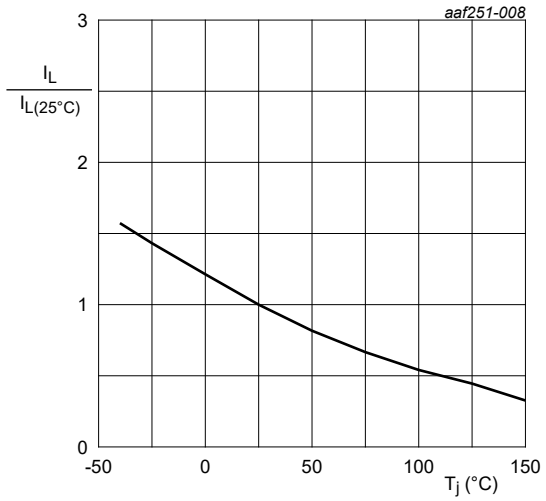


Fig. 9. Normalized latching current as a function of junction temperature

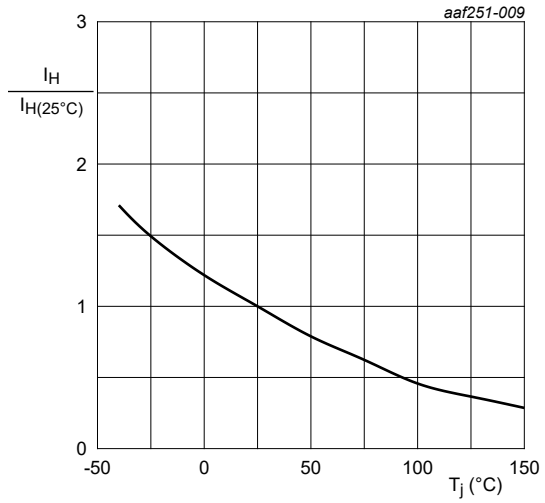
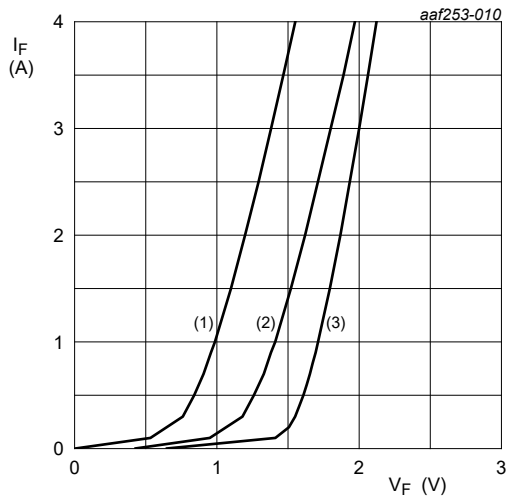


Fig. 10. Normalized holding current as a function of junction temperature



V_o = 1.073 V; R_s = 0.2475 Ω
(1) T_j = 150 °C; typical values
(2) T_j = 150 °C; maximum values
(3) T_j = 25 °C; maximum values

Fig. 11. On-state current as a function of on-state voltage

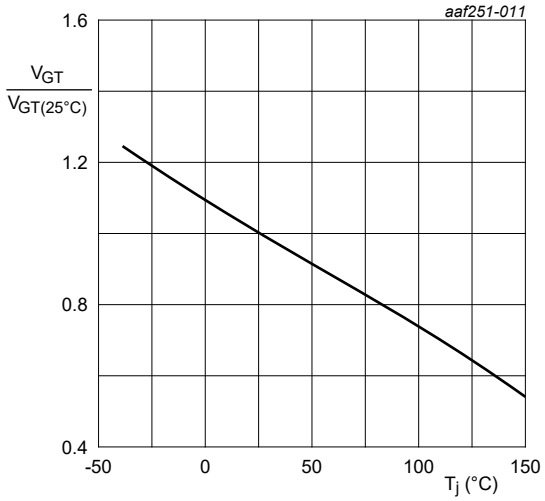
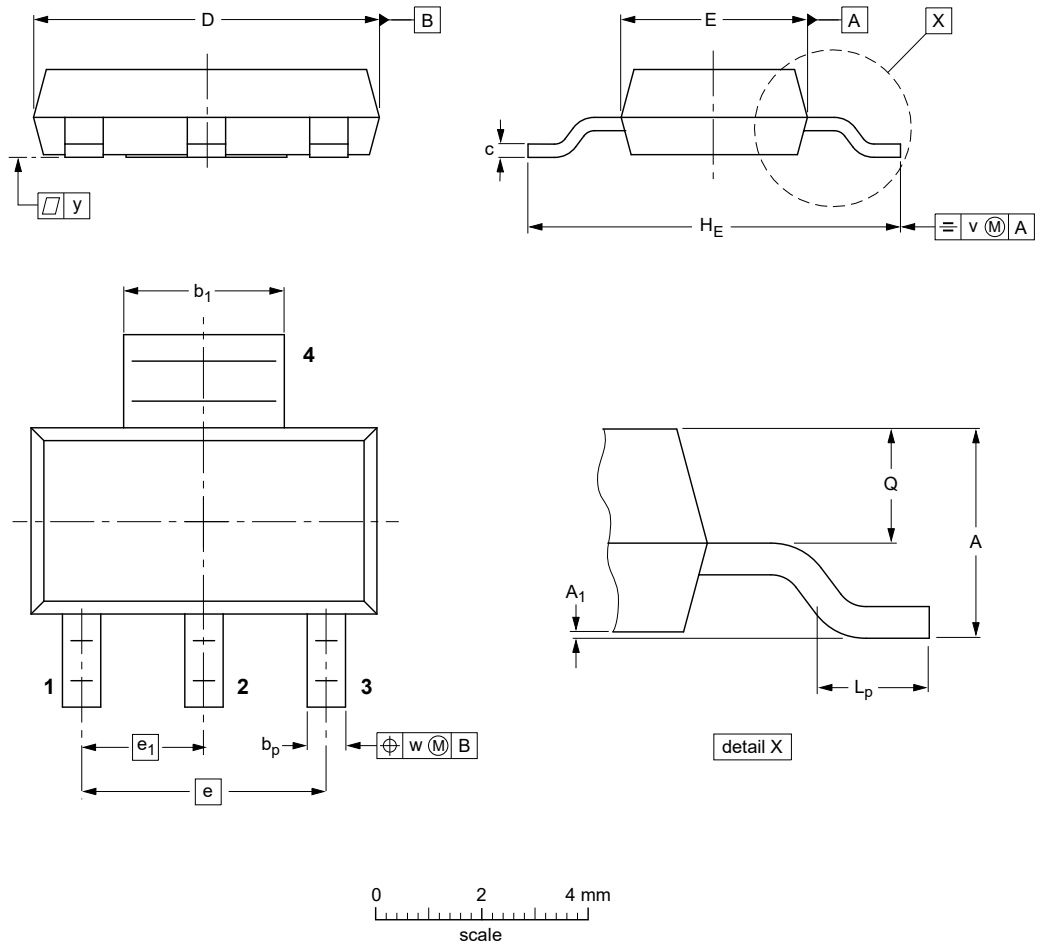


Fig. 12. Normalized gate trigger voltage as a function of junction temperature

10. Package outline

Plastic surface-mounted package with increased heatsink; 4 leads **SOT223**



DIMENSIONS (mm are the original dimensions)

UNIT	A	A_1	b_p	b_1	c	D	E	e	e_1	H_E	L_p	Q	v	w	y
mm	1.8 1.5	0.10 0.01	0.80 0.60	3.1 2.9	0.32 0.22	6.7 6.3	3.7 3.3	4.6	2.3	7.3 6.7	1.1 0.7	0.95 0.85	0.2	0.1	0.1

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT223			SC-73			~~04-11-10~~ 06-03-16

Fig. 13. Package outline SC-73 (SOT223)

11. Legal information

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Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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