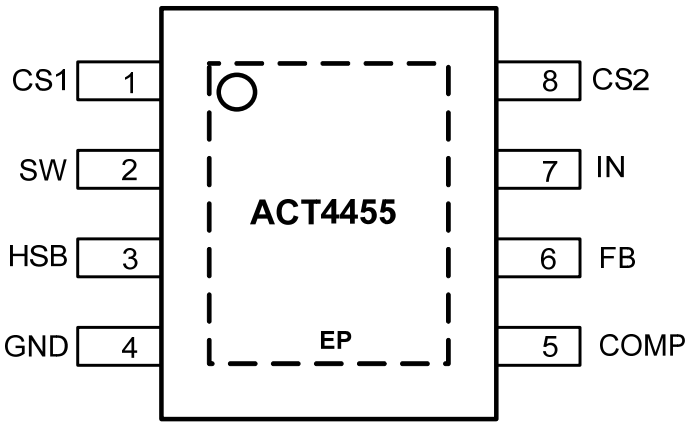
ORDERING INFORMATION

PART NUMBER	OPERATION TEMPERATURE RANGE	PACKAGE	PINS	PACKING
ACT4455YH-T	-40°C to 85°C	SOP-8EP	8	TAPE & REEL

PIN CONFIGURATION



SOP-8EP

PIN DESCRIPTIONS

PIN	NAME	DESCRIPTION
1	CS1	The output current of V_{OUT1} is sensed by this pin. When the voltage on this pin reaches 116mV for 750μs, the IC shuts down for 2.5 seconds before initiating a restartup.
2	SW	Switch Output. Connect this pin to the switching end of the external inductor.
3	HSB	High Side Bias. This pin acts as the positive rail for the high-side switch's gate driver. Connect a 22nF-100nF capacitor between HSB and SW pins.
4	GND	Ground.
5	COMP	Compensation Node. COMP is used to compensate the voltage regulation loop.
6	FB	Feedback Input. FB senses the output voltage to regulate that voltage. Drive FB with a resistive voltage divider from the output voltage. The feedback threshold is 0.808V. See *Setting the Output Voltage*.
7	IN	Input Supply. Bypass this pin to GND with a 10μF or greater low ESR capacitor.
8	CS2	The output current of V_{OUT2} is sensed by this pin. When the voltage on this pin reaches 116mV for 750μs, the IC shuts down for 2.5 seconds and then restarts.
	Exposed Pad	Exposed Pad. Connect this pad to thick copper plane via copper vias.

ABSOLUTE MAXIMUM RATINGS①

PARAMETER	VALUE	UNIT
IN to GND	-0.3 to 44	V
SW to GND	-0.3 to V_{IN} + 0.3	V
HSB to GND	V_{SW} - 0.3 to V_{SW} + 7	V
FB, CS1, CS2, COMP to GND	-0.3 to + 6	V
Junction to Ambient Thermal Resistance	50	°C/W
Operating Junction Temperature	-40 to 150	°C
Storage Junction Temperature	-55 to 150	°C
Lead Temperature (Soldering 10 sec.)	300	°C

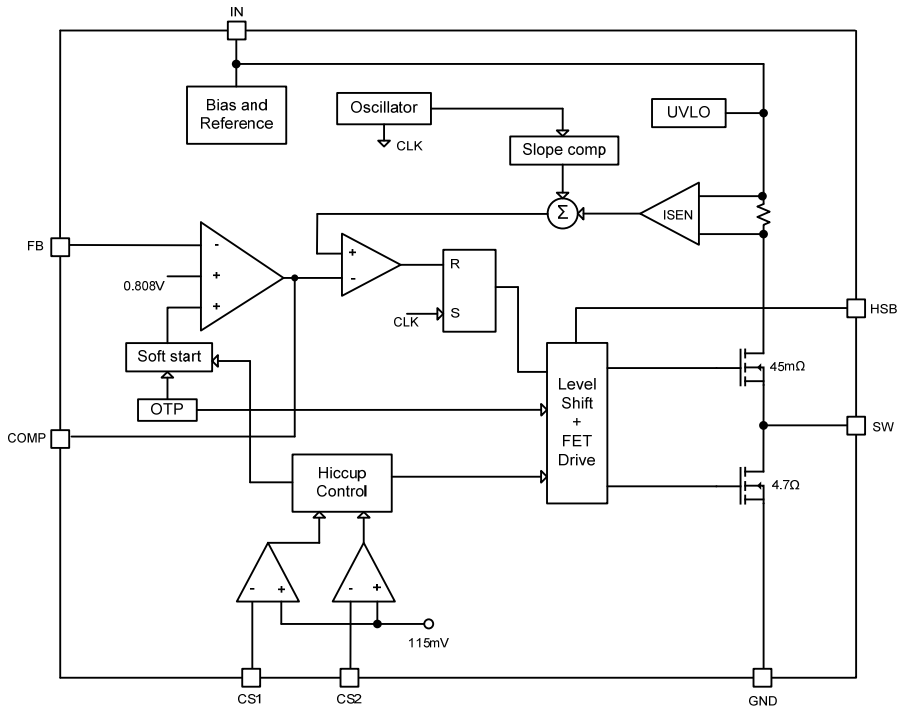
①: Do not exceed these limits to prevent damage to the device. Exposure to absolute maximum rating conditions for long periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{IN} = 12V, T_A = 25°C, unless otherwise specified.)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Feedback Voltage	V_{FB}	7.5V ≤ V_{IN} ≤ 40V	798	808	818	mV
Error Amplifier Voltage Gain	A_{EA}			4000		V/V
Error Amplifier Transconductance	G_{EA}	ΔI_{COMP} = ± 10μA		650		μA/V
Over Voltage Protection Threshold	V_{OVP}			41		V
Max E/A Source Current	I_{SRCMAX}	V_{FB} = 0.5V		120		μA
Max E/A Sink Current	$I_{SINKMAX}$	V_{FB} = 1.0V		120		μA
High-Side Switch ON-Resistance	$R_{DS(ON)1}$	At 25°C		38		mΩ
Low-Side Switch ON-Resistance	$R_{DS(ON)2}$			5		Ω
Maximum Duty Cycle	D_{MAX}			80		%
Switching Frequency	F_{SW}		180	200	220	kHz
Upper Switch Current Limit	I_{LIM}	Duty Cycle = 65%		6.5		A
COMP to Current Limit Transconductance	G_{COMP}			5		A/V
Minimum on Time	T_{ON_MIN}			250		ns
Input Under Voltage Lockout Threshold	V_{IN_Rise}	V_{IN} Rising	6.75	7	7.25	V
Input Under Voltage Lockout Hysteresis	$V_{IN\_Falling}$	V_{IN} Falling		650		mV
Internal Soft Startup Time	T_{SS}			3.0		ms
CS1 reference voltage	V_{CS1}		113	116	119	mV
CS2 reference voltage	V_{CS2}		113	116	119	mV
Frequency Foldback Threshold	$V_{FB\_Foldback}$			0.65		V
Cord Compensation		V_{IN} = 12V, R_{FB1}=200k, I_{OUT} = 5A		0.35		V
Thermal Shutdown				150		°C

FUNCTIONAL BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

Operation

As seen in *Functional Block Diagram*, the ACT4455 is a current mode controlled regulator. The EA output voltage (COMP voltage) is proportional to the peak inductor current.

A switching cycle starts when the rising edge of the Oscillator clock output causes the High-Side Power Switch to turn on and the Low-Side Power Switch to turn off. With the SW side of the inductor now connected to IN, the inductor current ramps up to store energy. The inductor current level is measured by the Current Sense Amplifier and added to the Oscillator ramp signal. If the resulting summation is higher than the COMP voltage, the output of the PWM Comparator goes high. When this happens or when Oscillator clock output goes low, the High-Side Power Switch turns off and the inductor freewheels through the schottky diode causing the inductor current to decrease and magnetic energy to be transferred to output. This state continues until the cycle starts again. The High-Side Power Switch is driven by logic using HSB as the positive rail. This pin is charged to V_{SW} + 5V when the Low-Side Power Switch turns on. The Comp voltage is the integration of the error between FB input and internal 0.808V reference. If FB is lower than the reference voltage, COMP tends to go higher to increase current to the output.

Over Current and Short Circuit Protection

CS pins are connected to the high side of current sensing resistors to prevent output over current. With independent CS1 and CS2 pins, two output currents are detected. If the voltage at either CS pins exceeds 116mV for more than 750μs. The converter shuts down and goes into sleeping mode. A new soft startup is triggered after 2.5s. If the fault condition is un-cleared, the converter shuts down again until over current condition is cleared. With this long-waiting-time hiccup mode, the power consumption at over loading or outputs short is reduced to nearly zero.

Thermal Shutdown

The ACT4455 shuts down when its junction temperature exceeds 150°C. The converter triggers a soft-start when the temperature has dropped by 10°C. The soft-restart avoids output over voltage at thermal hiccup.

APPLICATIONS INFORMATION

Output Voltage Setting

Figure 1:

Output Voltage Setting

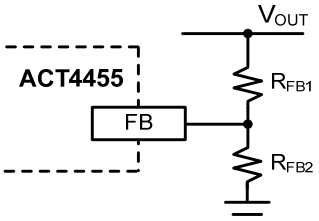


Figure 1 shows the connections for setting the output voltage. Select the proper ratio of the two feedback resistors R_{FB1} and R_{FB2} based on the output voltage. Typically, use R_{FB2} ≈ 10kΩ and determine R_{FB1} from the following equation:

$$R_{FB1} = R_{FB2}\left(\frac{V_{OUT}}{0.808\ V} - 1\right) \quad (1)$$

Over Current Protection Setting

The output over current threshold is calculated by:

$$I_{OCP1} = I_{OCP2} = 116mV / R_{SENSE} \quad (2)$$

It is recommended that 1% or 0.5% high-accuracy current sensing resistor is selected to achieve high-accuracy over current protection. Two over current protection thresholds can be different based on different current sensing resistance.

Inductor Selection

The inductor maintains a continuous current to the output load. This inductor current has a ripple that is dependent on the inductance value:

Higher inductance reduces the peak-to-peak ripple current. The trade off for high inductance value is the increase in inductor core size and series resistance, and the reduction in current handling capability. In general, select an inductance value L based on ripple current requirement:

$$L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} f_{SW} I_{LOADMAX} K_{RIPPLE}} \quad (3)$$

where V_{IN} is the input voltage, V_{OUT} is the output voltage, f_{SW} is the switching frequency, $I_{LOADMAX}$ is the maximum load current, and K_{RIPPLE} is the ripple factor. Typically, choose K_{RIPPLE} = 30% to correspond to the peak-to-peak ripple current being 30% of the maximum load current.

With a selected inductor value the peak-to-peak inductor current is estimated as:

$$I_{LPK-PK} = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{L \times V_{IN} \times f_{SW}} \quad (4)$$

The peak inductor current is estimated as:

$$I_{LPK} = I_{LOADMAX} + \frac{1}{2} I_{LPK-PK} \quad (5)$$

The selected inductor should not saturate at I_{LPK}. The maximum output current is calculated as:

$$I_{OUTMAX} = I_{LIM} - \frac{1}{2} I_{LPK-PK} \quad (6)$$

I_{LIM} is the internal current limit, which is typically 6.5A, as shown in Electrical Characteristics Table.

Input Capacitor

The input capacitor needs to be carefully selected to maintain sufficiently low ripple at the supply input of the converter. A low ESR capacitor is highly recommended. Since large current flows in and out of this capacitor during switching, its ESR also affects efficiency.

The input capacitance needs to be higher than 10μF. The best choice is the ceramic type, however, low ESR tantalum or electrolytic types may also be used provided that the RMS ripple current rating is higher than 50% of the output current. The input capacitor should be placed close to the IN and G pins of the IC, with the shortest traces possible. In the case of tantalum or electrolytic types, they can be further away if a small parallel 0.1μF ceramic capacitor is placed right next to the IC.

Output Capacitor

The output capacitor also needs to have low ESR to keep low output voltage ripple. The output ripple voltage is:

$$V_{RIPPLE} = I_{OUTMAX} K_{RIPPLE} R_{ESR} + \frac{V_{IN}}{28 \times f_{SW}^2 LC_{OUT}} \quad (7)$$

Where I_{OUTMAX} is the maximum output current, K_{RIPPLE} is the ripple factor, R_{ESR} is the ESR of the output capacitor, f_{SW} is the switching frequency, L is the inductor value, and C_{OUT} is the output capacitance. In the case of ceramic output capacitors, R_{ESR} is very small and does not contribute to the ripple. Therefore, a lower capacitance value can be used for ceramic type. In the case of tantalum or electrolytic capacitors, the ripple is dominated by R_{ESR} multiplied by the ripple

APPLICATIONS INFORMATION CONT'D

current. In that case, the output capacitor is chosen to have sufficiently low ESR.

For ceramic output capacitor, typically choose a capacitance of about 22μF. For tantalum or electrolytic capacitors, choose a capacitor with less than 50mΩ ESR.

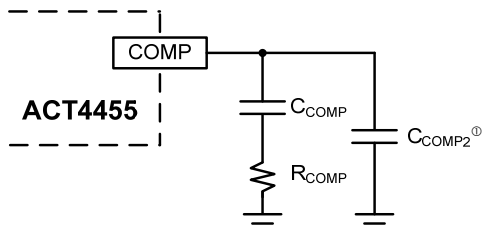
Rectifier Diode

Use a Schottky diode as the rectifier to conduct current when the High-Side Power Switch is off. The Schottky diode must have current rating higher than the maximum output current and a reverse voltage rating higher than the maximum input voltage.

STABILITY COMPENSATION

Figure 2:

Stability Compensation



①: C_{COMP2} is needed only for high ESR output capacitor

The feedback loop of the IC is stabilized by the components at the COMP pin, as shown in Figure 2. The DC loop gain of the system is determined by the following equation:

$$A_{VDC} = \frac{0.808\ V}{I_{OUT}} A_{VEA} G_{COMP} \quad (8)$$

The dominant pole P1 is due to C_{COMP}:

$$f_{P1} = \frac{G_{EA}}{2\pi A_{VEA} C_{COMP}} \quad (9)$$

The second pole P2 is the output pole:

$$f_{P2} = \frac{I_{OUT}}{2\pi V_{OUT} C_{OUT}} \quad (10)$$

The first zero Z1 is due to R_{COMP} and C_{COMP}:

$$f_{Z1} = \frac{1}{2\pi R_{COMP} C_{COMP1}} \quad (11)$$

And finally, the third pole is due to R_{COMP} and C_{COMP2} (if C_{COMP2} is used):

$$f_{P3} = \frac{1}{2\pi R_{COMP} C_{COMP2}} \quad (12)$$

The following steps should be used to compensate the IC:

STEP 1. Set the cross over frequency at 1/10 of the switching frequency via R_{COMP}:

$$R_{COMP} = \frac{2\pi V_{OUT} C_{OUT} f_{SW}}{10 G_{EA} G_{COMP} \times 0.808V}$$

$$= 0.48 \times 10^{8} V_{OUT} C_{OUT} \ (\Omega) \quad (13)$$

STEP 2. Set the zero f_{Z1} at 1/4 of the cross over frequency. If R_{COMP} is less than 15kΩ, the equation for C_{COMP} is:

$$C_{COMP} = \frac{3.18 \times 10^{-5}}{R_{COMP}} \ (F) \quad (14)$$

If R_{COMP} is limited to 15kΩ, then the actual cross over frequency is 6.36 / ($V_{OUT}C_{OUT}$). Therefore:

$$C_{COMP} = 6.67 \times 10^{-6} V_{OUT} C_{OUT} \ (F) \quad (15)$$

STEP 3. If the output capacitor's ESR is high enough to cause a zero at lower than 4 times the cross over frequency, an additional compensation capacitor C_{COMP2} is required. The condition for using C_{COMP2} is:

$$R_{ESRCOUT} \geq Min\left(\frac{1.1 \times 10^{-6}}{C_{OUT}}, 0.012 \times V_{OUT}\right) \ (\Omega) \quad (16)$$

And the proper value for C_{COMP2} is:

$$C_{COMP2} = \frac{C_{OUT} R_{ESRCOUT}}{R_{COMP}} \quad (17)$$

Though C_{COMP2} is unnecessary when the output capacitor has sufficiently low ESR, a small value C_{COMP2} such as 100pF may improve stability against PCB layout parasitic effects.

Table 1 shows some calculated results based on the compensation method above.

Table 1:

Typical Compensation for Different Output Voltages and Output Capacitors

V_{OUT}	C_{OUT}	R_{COMP}	C_{COMP}	C_{COMP2}①
2.5V	47μF SP CAP	5.6kΩ	5.6nF	None
3.3V	47μF SP CAP	7.5kΩ	4.7nF	None
5V	47μF SP CAP	11kΩ	3.3nF	None
2.5V	680μF/6.3V/30mΩ	15kΩ	3.3nF	220pF
3.3V	680μF/6.3V/30mΩ	15kΩ	3.3nF	220pF
5V	680μF/6.3V/30mΩ	15kΩ	4.7nF	220pF

①: C_{COMP2} is needed for high ESR output capacitor.

Output Cable Resistance Compensation

To compensate for resistive voltage drop across the charger's output cable, the ACT4455 integrates a simple, user-programmable cable voltage drop compensation using the impedance at the FB pin. Use the curve in Figure 3 to choose the proper feedback resistance values for cable compensation. R_{FB1} is the high side resistor of voltage divider.

STABILITY COMPENSATION CONT'D

In the case of high R_{FB1} used, the frequency compensation needs to be adjusted correspondingly. As show in Figure 4, adding a capacitor in paralled with R_{FB1} or increasing the compensation capacitance at COMP pin helps the system stability.

Figure 3:

Cable Compensation at Various Resistor Divider Values

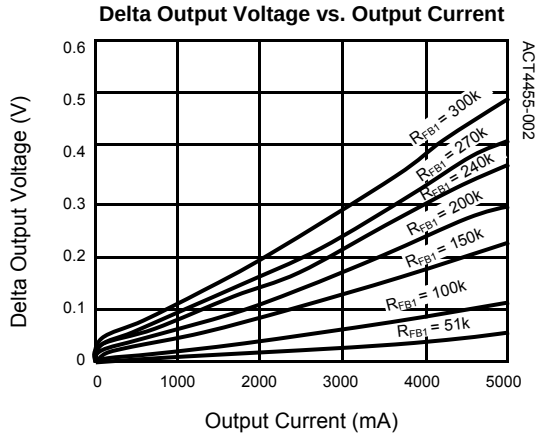
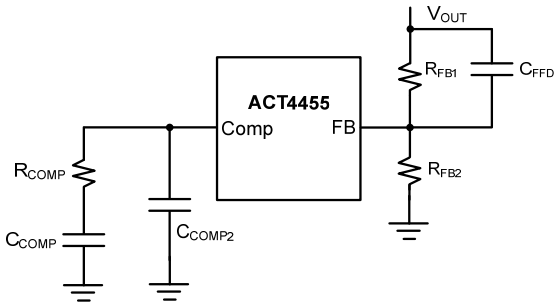


Figure 4:

Frequency Compensation for High R_{FB1}



PC Board Layout Guidance

When laying out the printed circuit board, the following checklist should be used to ensure proper operation of the IC.

1) Arrange the power components to reduce the AC loop size consisting of C_{IN}, IN pin, SW pin and the schottky diode.
2) Place input decoupling ceramic capacitor C_{IN} as close to IN pin as possible. C_{IN} is connected power GND with vias or short and wide path.
3) Return FB, COMP and ISET to signal GND pin, and connect the signal GND to power GND at a single point for best noise immunity. Connect exposed pad to power ground copper area with copper and vias.
4) Use copper plane for power GND for best heat dissipation and noise immunity.
5) Place feedback resistor close to FB pin.
6) Use short trace connecting HSB-C_{HSB}-SW loop
7) SW pad is noisy node switching from V_{IN} to GND. It should be isolated away from the rest of circuit for good EMI and low noise operation.

Figure 5:
Typical Application Circuit for 5V/4.2A Dual-output Car Charger

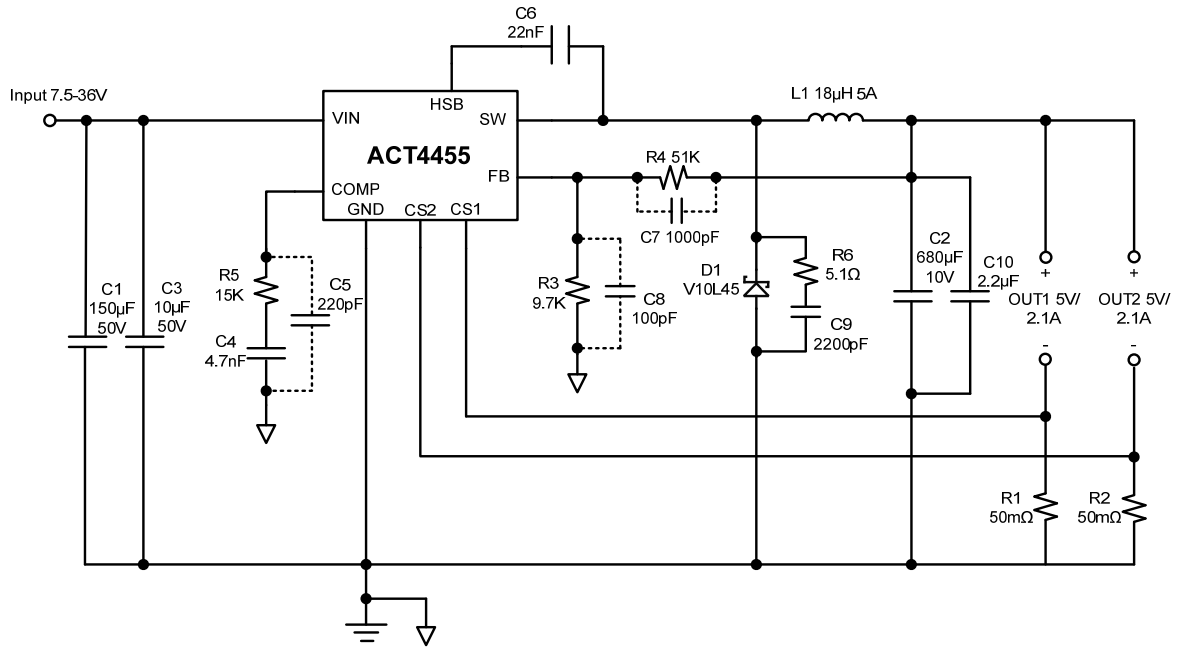


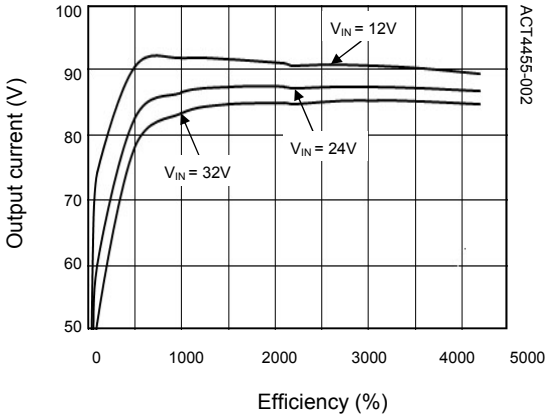
Table 2:
BOM List for 5V/4.2A Dual-output Car Charger

ITEM	REFERENCE	DESCRIPTION	MANUFACTURER	QTY
1	U1	IC ACT4455YH, SOP-8EP	Active-Semi	1
2	C1	Capacitor, Electrolytic, 150µF/50V, 8×8mm	Koshin	1
3	C2	Capacitor, Electrolytic, 680µF/10V, 8×11.5mm	Koshin	1
4	C3	Capacitor, Ceramic, 10µF/50V, 1206, SMD	Murata, TDK	1
5	C4	Capacitor, Ceramic, 4.7nF/25V, 0603, SMD	Murata, TDK	1
6	C5	Capacitor, Ceramic, 220pF/25V, 0603, SMD (Optional)	Murata, TDK	1
7	C6	Capacitor, Ceramic, 2.2nF/25V, 0603, SMD	Murata, TDK	1
8	C7	Capacitor, Ceramic, 1000pF/25V, 0603, SMD (Optional)	Murata, TDK	1
9	C8	Capacitor, Ceramic, 100pF/25V, 0603, SMD (Optional)	Murata, TDK	1
10	C9	Capacitor, Ceramic, 2200pF/25V, 0805, SMD	Murata, TDK	1
11	C10	Capacitor, Ceramic, 2.2µF/16V, 0603, SMD	Murata, TDK	1
12	L1	Inductor, 18µH, 5A, 20%, DIP	Electronic-Magnetics	1
13	D1	Diode, Schottky, 45V/10A, V10L45	Vishay	1
14	R1, R2	Chip Resistor, 50mΩ, 1206, 1%	Murata, TDK	2
15	R3	Chip Resistor, 9.7kΩ, 0603, 1%	Murata, TDK	1
16	R4	Chip Resistor, 51kΩ, 0603, 1%	Murata, TDK	1
17	R5	Chip Resistor, 15kΩ, 0603, 5%	Murata, TDK	1
18	R6	Chip Resistor, 5.1Ω, 1206, 5%	Murata, TDK	1

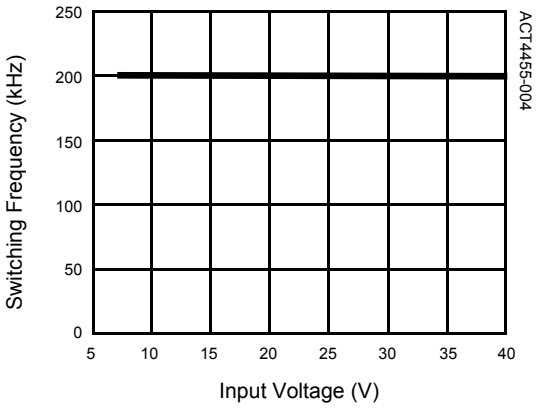
TYPICAL PERFORMANCE CHARACTERISTICS

(Circuit of Figure 7, R_{CS1} = R_{CS2} = 50mΩ, L = 18μH, C_{IN} = 150μF, C_{OUT} = 680μF, T_A = 25°C, unless otherwise specified.)

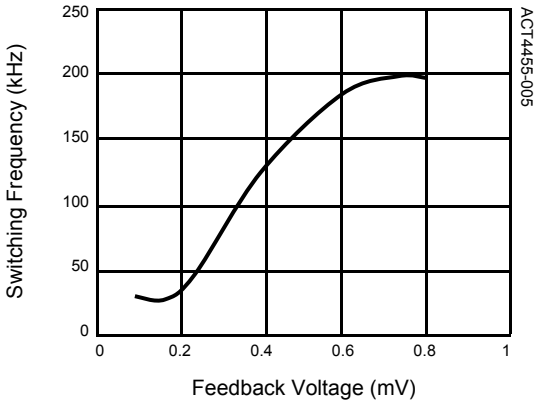
Efficiency vs. Load current



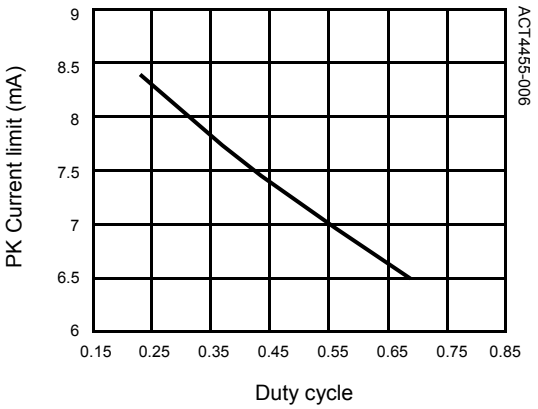
Switching Frequency vs. Input Voltage



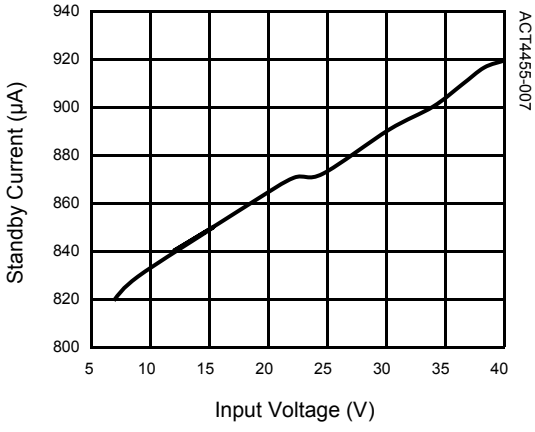
Switching Frequency vs. Feedback Voltage



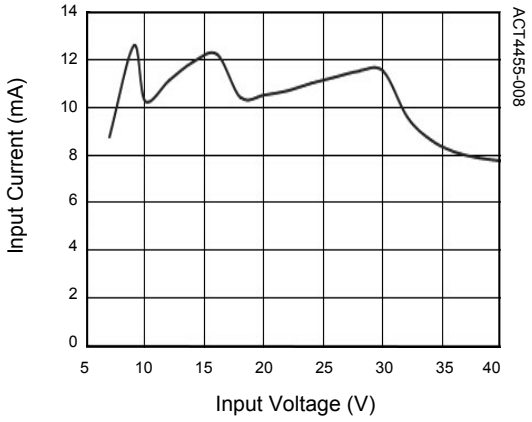
Maximum Peak Current vs. Duty Cycle



Standby Current vs. Input Voltage



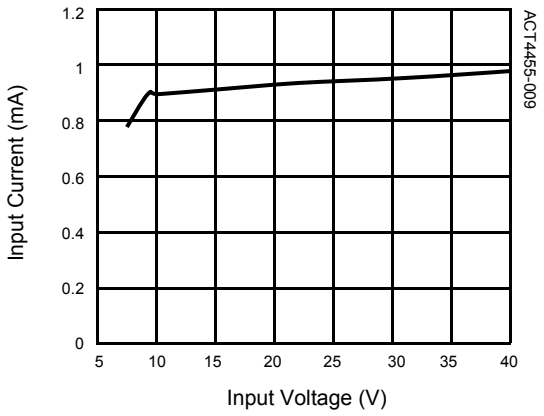
Input Current vs. Input Voltage at No Load



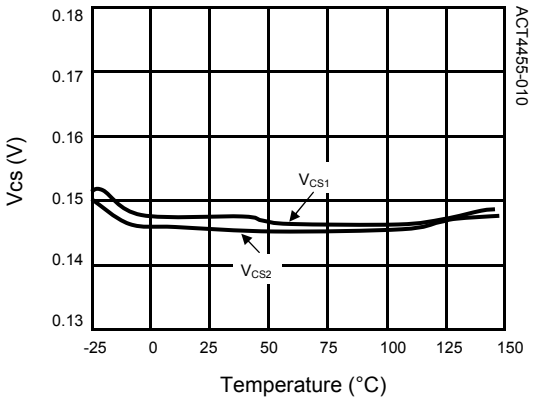
TYPICAL PERFORMANCE CHARACTERISTICS CONT'D

(Circuit of Figure 7, R_{CS1} = R_{CS2} = 50mΩ, L = 18μH, C_{IN} = 150μF, C_{OUT} = 680μF, T_A = 25°C, unless otherwise specified.)

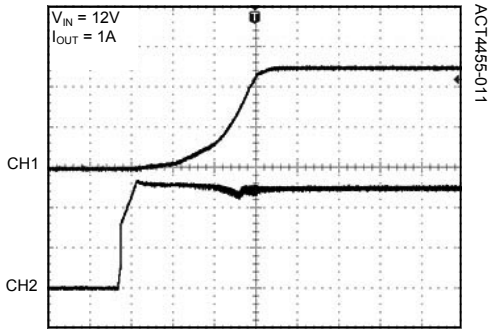
Input Current at Output Short Output



Vcs vs. Temperature

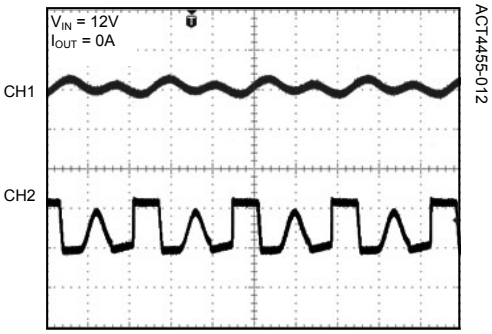


Start Up



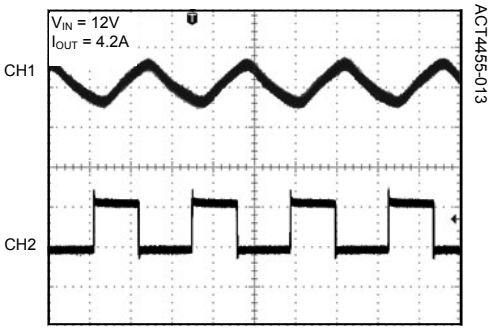
CH1: V_{OUT}, 2V/div
CH2: V_{IN}, 5V/div
TIME: 1ms/div

SW vs. Output Ripples



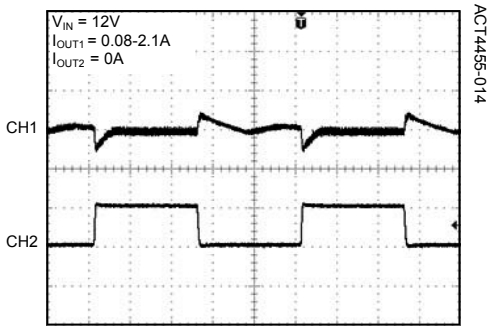
CH1: Ripper, 50mV/div
CH2: SW, 10V/div
TIME: 2μs/div

SW vs. Output Ripples



CH1: Ripper, 50mV/div
CH2: SW, 10V/div
TIME: 2μs/div

Load Step Waveforms

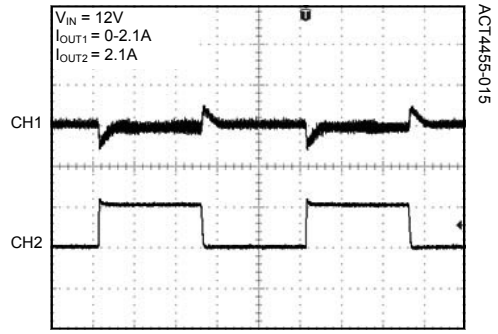


CH1: V_{OUT} Ripple, 200mV/div
CH2: I_{OUT}, 2A/div
TIME: 400μs/div

TYPICAL PERFORMANCE CHARACTERISTICS CONT'D

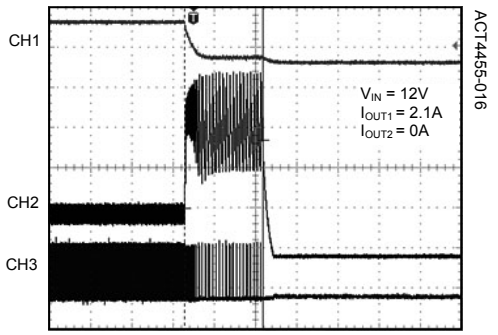
(Circuit of Figure 7, R_{CS1} = R_{CS2} = 50mΩ, L = 18μH, C_{IN} = 150μF, C_{OUT} = 680μF, T_A = 25°C, unless otherwise specified.)

Load Step Waveforms



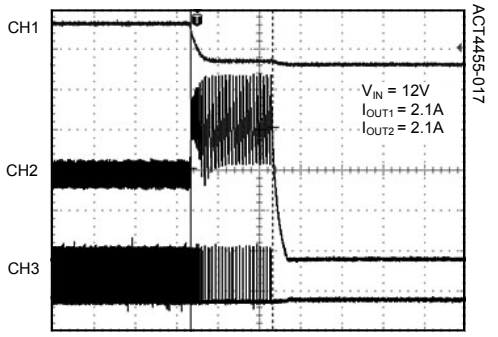
CH1: V_{OUT} Ripper, 200mV/div
CH2: I_{OUT}, 2A/div
TIME: 400μs/div

Short Circuit



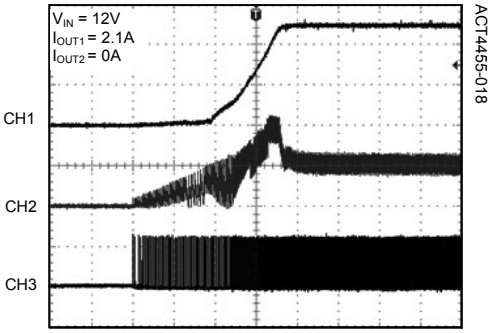
CH1: V_{OUT}, 5V/div
CH2: IL, 2A/div
CH3: SW, 10V/div
TIME: 400μs/div

Short Circuit



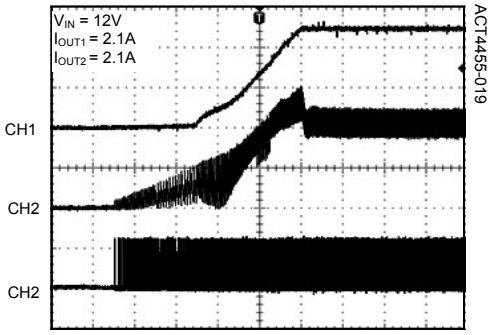
CH1: V_{OUT}, 5V/div
CH2: IL, 2A/div
CH3: SW, 10V/div
TIME: 400μs/div

Short Circuit Recovery



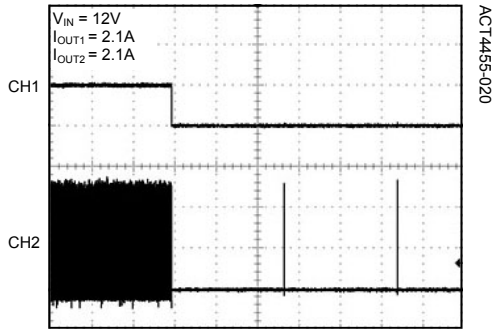
CH1: V_{OUT}, 2V/div
CH2: IL, 2A/div
CH3: SW, 10V/div
TIME: 1ms/div

Short Circuit Recovery



CH1: V_{OUT}, 2V/div
CH2: IL, 2A/div
CH3: SW, 10V/div
TIME: 1ms/div

Hiccup Mode

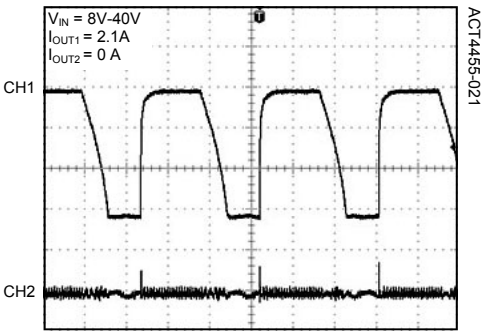


CH1: V_{OUT}, 5V/div
CH2: SW, 5V/div
TIME: 1s/div

TYPICAL PERFORMANCE CHARACTERISTICS CONT'D

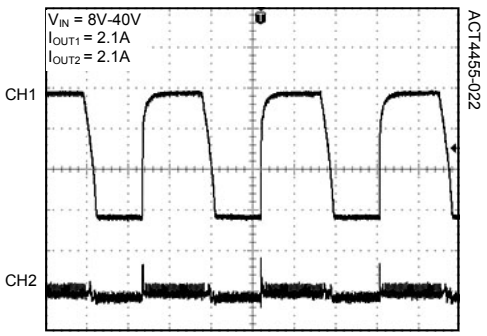
(Circuit of Figure 7, R_{CS1} = R_{CS2} = 50mΩ, L = 18μH, C_{IN} = 150μF, C_{OUT} = 680μF, T_A = 25°C, unless otherwise specified.)

Input Surge



CH1: V_{IN}, 10V/div
CH2: V_{OUT} Ripper, 200mV/div
TIME: 10ms/div

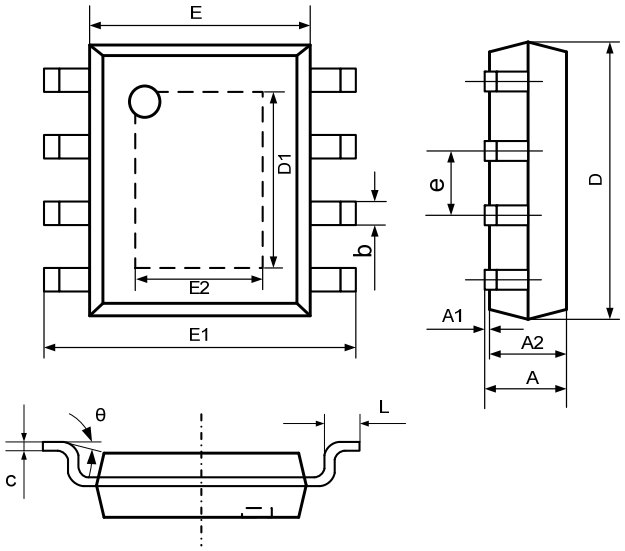
Input Surge



CH1: V_{IN}, 10V/div
CH2: V_{OUT} Ripper, 200mV/div
TIME: 10ms/div

PACKAGE OUTLINE

SOP-8EP PACKAGE OUTLINE AND DIMENSIONS



SYMBOL	DIMENSION IN MILLIMETERS		DIMENSION IN INCHES	
	MIN	MAX	MIN	MAX
A	1.350	1.700	0.053	0.067
A1	0.000	0.100	0.000	0.004
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.007	0.010
D	4.700	5.100	0.185	0.200
D1	3.202	3.402	0.126	0.134
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
E2	2.313	2.513	0.091	0.099
e	1.270 TYP		0.050 TYP	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°