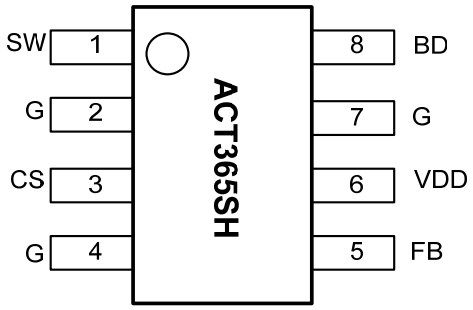
## ORDERING INFORMATION

| PART NUMBER | TEMPERATURE RANGE | PACKAGE | PINS | PACKING METHOD | TOP MARK |
|---|---|---|---|---|---|
| ACT365SH-T | -40°C to 85°C | SOP-8 | 8 | TAPE & REEL | ACT365SH |

## PIN CONFIGURATION




**SOP-8**
**ACT365SH**

## PIN DESCRIPTIONS

| PIN | NAME | DESCRIPTION |
|---|---|---|
| 1 | SW | Switch Drive. Switch node for the external NPN transistor. Connect this pin to the external power NPN's emitter. This pin also supplies current to VDD during startup. |
| 2,4,7 | G | Ground. |
| 8 | BD | Base Drive. Base driver for the external NPN transistor. |
| 6 | VDD | Power Supply. This pin provides bias power for the IC during startup and steady state operation. |
| 5 | FB | Feedback Pin. Connect this pin to a resistor divider network from the auxiliary winding. |
| 3 | CS | Current Sense Pin. Connect an external resistor ($R_{CS}$) between this pin and ground to set peak current limit for the primary switch. The peak current limit is set by (0.396V × 0.9) / $R_{CS}$. For more detailed information, see Application Information. |

## ABSOLUTE MAXIMUM RATINGS①

| PARAMETER | VALUE | UNIT |
|---|---|---|
| VDD, BD, SW to G | -0.3 to +28 | V |
| Maximum Continuous VDD Current | 100 | mA |
| FB, CS to G | -0.3 to +6 | V |
| Continuous SW Current | Internally limited | A |
| Maximum Power Dissipation (derate 6.7mW/˚C above $T_A$ = 50˚C) | 0.95 | W |
| Junction to Ambient Thermal Resistance ($\theta_{JA}$) | 105 | ˚C/W |
| Operating Junction Temperature | -40 to 150 | ˚C |
| Storage Junction | -55 to 150 | ˚C |
| Lead Temperature (Soldering, 10 sec) | 300 | ˚C |

①: Do not exceed these limits to prevent damage to the device. Exposure to absolute maximum rating conditions for long periods may affect device reliability.

## ELECTRICAL CHARACTERISTICS

($V_{DD}$ = 14V, $V_{OUT}$ = 5V, $L_P$ = 1.5mH, $N_P$ = 140, $N_S$ = 7, $N_A$ = 19, $T_A$ = 25°C, unless otherwise specified.)

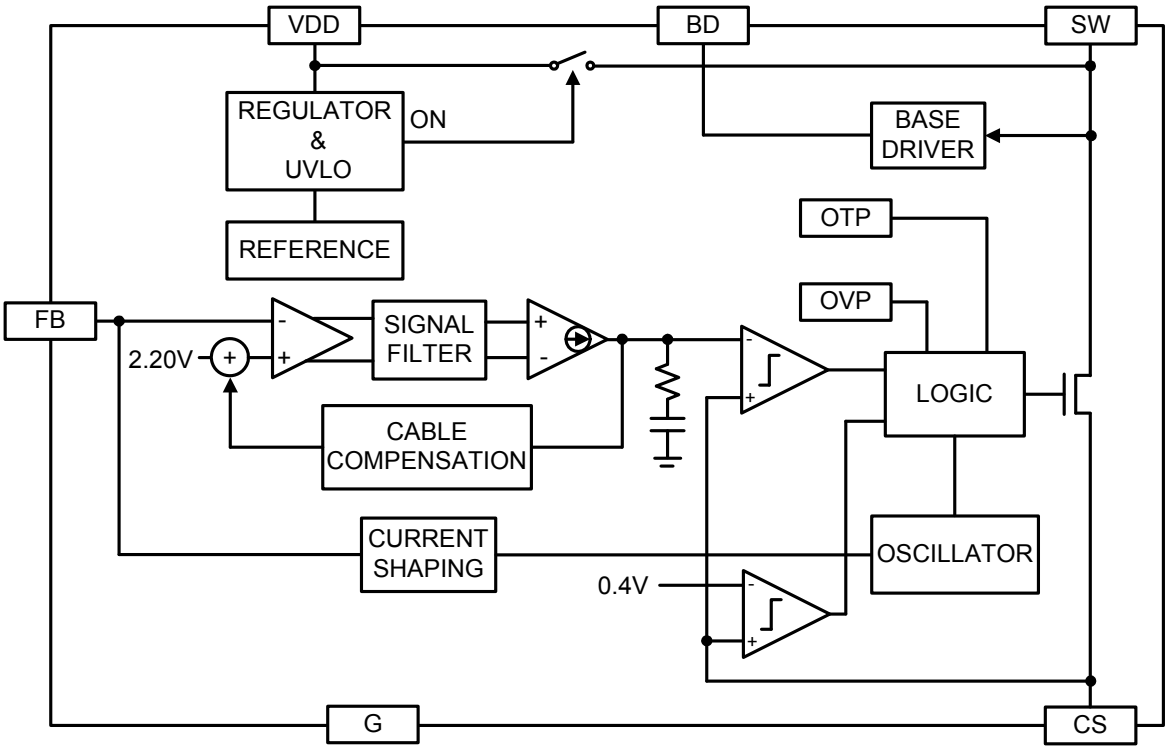
| PARAMETER | SYMBOL | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **Supply** | | | | | | |
| VDD Turn-On Voltage | $V_{DDON}$ | $V_{DD}$ Rising from 0V | 17.6 | 18.6 | 19.6 | V |
| VDD Turn-Off Voltage | $V_{DDOFF}$ | $V_{DD}$ Falling after Turn-on | 5.25 | 5.5 | 5.75 | V |
| Supply Current | $I_{DD}$ | $V_{DD}$ = 14V, after Turn-on | | 1 | 2 | mA |
| Start Up Supply Current | $I_{DDST}$ | $V_{DD}$ = 14V, before Turn-on | | 25 | 45 | μA |
| BD Current during Startup | $I_{BDST}$ | | | | 1 | μA |
| Internal Soft Startup Time | | | | 10 | | ms |
| **Oscillator** | | | | | | |
| Switching Frequency | $f_{SW}$ | 100% $V_{OUTCV}$ @ full load | | 80 | | kHz |
| | | 25% $V_{OUTCV}$ @ full load | | 40 | | |
| Maximum Switching Frequency | $F_{CLAMP}$ | | 85 | 100 | 110 | kHz |
| Maximum Duty Cycle | $D_{MAX}$ | | 65 | 75 | 85 | % |
| **Feedback** | | | | | | |
| Effective FB Voltage | $V_{FB}$ | | 2.176 | 2.200 | 2.224 | V |
| FB Leakage Current | $I_{FBLK}$ | | | | 100 | nA |
| Output Cable Resistance Compensation | $DV_{COMP}$ | No $R_{CORD}$ between VDD and SW | | 0 | | % |
| | | $R_{CORD}$ = 300k | | 3 | | |
| | | $R_{CORD}$ = 150k | | 6 | | |
| | | $R_{CORD}$ = 75k | | 9 | | |
| | | $R_{CORD}$ = 33k | | 12 | | |

## ELECTRICAL CHARACTERISTICS CONT'D

($V_{DD}$ = 14V, $V_{OUT}$ = 5V, $L_P$ = 1.5mH, $N_P$ = 140, $N_S$ = 7, $N_A$ = 19, $T_A$ = 25°C, unless otherwise specified.)

| PARAMETER | SYMBOL | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **Current Limit** | | | | | | |
| SW Current Limit Range | $I_{LIM}$ | | 100 | | 800 | mA |
| CS Current Limit Threshold | $V_{CSLIM}$ | $t_{OFF\_DELAY}$ = 0 | 380 | 396 | 412 | mV |
| Leading Edge Blanking Time | | | 200 | 300 | | ns |
| **Driver Outputs** | | | | | | |
| Switch ON-Resistance | $R_{ON}$ | $I_{SW}$ = 50mA | | 1.6 | 3 | Ω |
| SW Off Leakage Current | | $V_{SW}$ = $V_{DD}$ = 22V | | | 5 | μA |
| **Protection** | | | | | | |
| VDD Latch-Off Voltage | $V_{DDOVP}$ | | $V_{DDON}$ +2 | $V_{DDON}$ +3 | $V_{DDON}$ +4 | V |
| Thermal Shutdown Temperature | | | | 135 | | ˚C |
| Thermal Hysteresis | | | | 20 | | ˚C |
| Line UVLO | $I_{FBUVLO}$ | | | 116 | | μA |

## FUNCTIONAL BLOCK DIAGRAM



# FUNCTIONAL DESCRIPTION

As shown in the *Functional Block Diagram,* to regulate the output voltage in CV (constant voltage) mode, the ACT365 compares the feedback voltage at FB pin to the internal reference and generates an error signal to the pre-amplifier. The error signal, after filtering out the switching transients and compensated with the internal compensation network, modulates the external NPN transistor peak current at CS pin with current mode PFWM (Pulse Frequency and Width Modulation) control. To regulate the output current in CC (constant current) mode, the oscillator frequency is modulated by the output voltage.

SW is a driver output that drives the emitter of an external high voltage NPN transistor. This base-emitter-drive method makes the drive circuit the most efficient.

## Fast Startup

VDD is the power supply terminal for the ACT365. During startup, the ACT365 typically draws only 20μA supply current. The startup resistor from the rectified high voltage DC rail supplies current to the base of the NPN transistor. This results in an amplified emitter current to VDD through the SW pin via Active-Semi's proprietary fast-startup circuitry until it exceeds the $V_{DDON}$ threshold 19V. At this point, the ACT365 enters internal startup mode with the peak current limit ramping up in 10ms. After switching starts, the output voltage begins to rise. The VDD bypass capacitor must supply the ACT365 internal circuitry and the NPN base drive until the output voltage is high enough to sustain VDD through the auxiliary winding. The $V_{DDOFF}$ threshold is 5.5V; therefore, the voltage on the VDD capacitor must remain above 5.5V while the output is charging up.

## Constant Voltage (CV) Mode Operation

In constant voltage operation, the ACT365 captures the auxiliary flyback signal at FB pin through a resistor divider network R5 and R6 in Figure 6. The signal at FB pin is pre-amplified against the internal reference voltage, and the secondary side output voltage is extracted based on Active-Semi's proprietary filter architecture.

This error signal is then amplified by the internal error amplifier. When the secondary output voltage is above regulation, the error amplifier output voltage decreases to reduce the switch current. When the secondary output voltage is below regulation, the error amplifier output voltage increases to ramp up the switch current to bring the secondary output back to regulation. The output regulation voltage is determined by the following relationship:

$$V_{OUTCV} = 2.20V \times \left(1 + \frac{R_{FB1}}{R_{FB2}}\right) \times \frac{N_S}{N_A} - V_D \qquad (1)$$

where $R_{FB1}$ (R5) and $R_{FB2}$ (R6) are top and bottom feedback resistor, $N_S$ and $N_A$ are numbers of transformer secondary and auxiliary turns, and $V_D$ is the rectifier diode forward drop voltage at approximately 0.1A bias.

### *Standby (No Load) Mode*

In no load standby mode, the ACT365 oscillator frequency is further reduced to a minimum frequency while the current pulse is reduced to a minimum level to minimize standby power. The actual minimum switching frequency is programmable with an output preload resistor.

### *Loop Compensation*

The ACT365 integrates loop compensation circuitry for simplified application design, optimized transient response, and minimal external components.

### *Output Cable Resistance Compensation*

The ACT365 provides programmable output cable resistance compensation during constant voltage regulation, monotonically adding an output voltage correction up to predetermined percentage at full power. There are four levels to program the output cable compensation by connecting a resistor (R10 in Figure 3) from the SW pin to VDD pin. The percentage at full power is programmable to be 3%, 6%, 9% or 12%, and by using a resistor value of 300k, 150k, 75k or 33k respectively. If there is no resistor connection, there is no cord compensation.

This feature allows for better output voltage accuracy by compensating for the output voltage droop due to the output cable resistance.

## Constant Current (CC) Mode Operation

When the secondary output current reaches a level set by the internal current limiting circuit, the ACT365 enters current limit condition and causes the secondary output voltage to drop. As the output voltage decreases, so does the flyback voltage in a proportional manner. An internal current shaping circuitry adjusts the switching frequency based on the flyback voltage so that the transferred power remains proportional to the output voltage, resulting

## FUNCTIONAL DESCRIPTION CONT'D

in a constant secondary side output current profile. The energy transferred to the output during each switching cycle is ½($L_P$ × $I_{LIM}^2$) × η, where $L_P$ is the transformer primary inductance, $I_{LIM}$ is the primary peak current, and η is the conversion efficiency. From this formula, the constant output current can be derived:

$$I_{OUTCC} = \frac{1}{2} \times L_P \times \left( \frac{0.396\,V \times 0.9}{R_{CS}} \right)^2 \times \left( \frac{\eta \times f_{SW}}{V_{OUTCV}} \right) \quad (2)$$

where $f_{SW}$ is the switching frequency and $V_{OUTCV}$ is the nominal secondary output voltage.

The constant current operation typically extends down to lower than 40% of nominal output voltage regulation.

#### *Primary Inductance Compensation*

The ACT365 integrates a built-in proprietary (patent-pending) primary inductance compensation circuit to maintain constant current regulation despite variations in transformer manufacturing. The compensated range is ±7%.

#### *Primary Inductor Current Limit Compensation*

The ACT365 integrates a primary inductor peak current limit compensation circuit to achieve constant input power over line and load ranges.

### Protection

The ACT365 incorporates multiple protection functions including over-voltage, over-current and over-temperature.

#### *Output Short Circuit Protection*

When the secondary side output is short circuited, the ACT365 enters hiccup mode operation. In this condition, the VDD voltage drops below the $V_{DDOFF}$ threshold and the auxiliary supply voltage collapses. This turns off the ACT365 and causes it to restart. This hiccup behavior continues until the short circuit is removed.

#### *Output Over Voltage Protection*

The ACT365 includes output over-voltage protection circuitry, which shuts down the IC when the output voltage is 40% above the normal regulation voltage for 4 consecutive switching cycles. The ACT365 enters hiccup mode when an output over voltage fault is detected.

#### *Over Temperature Shutdown*

The thermal shutdown circuitry detects the ACT365 die temperature. The typical over temperature threshold is 135°C with 20°C hysteresis. When the die temperature rises above this threshold the ACT365 is disabled until the die temperature falls by 20°C, at which point the ACT365 is re-enabled.

## TYPICAL APPLICATION

### Design Example

The design example below gives the procedure for a DCM flyback converter using the ACT365. Refer to Application Circuit in Figure 3, the design for a adapter application starts with the following specification:

| | |
|---|---|
| Input Voltage Range | 85VAC - 265VAC, 50/60Hz |
| Output Power, $P_O$ | 10.5W |
| Output Voltage, $V_{OUTCV}$ | 5.0V |
| Full Load Current, $I_{OUTFL}$ | 2.1A |
| OCP Current, $I_{OUTMAX}$ | 2.4A |
| Transformer Efficiency, $\eta_{xfm}$ | 0.89 |
| System Efficiency CC, $\eta_{system}$ | 0.76 |
| System Efficiency CV, η | 0.77 |

The operation for the circuit shown in Figure 3 is as follows: the rectifier bridge BD1 and the capacitor C1/C2 convert the AC line voltage to DC. This voltage supplies the primary winding of the transformer T1 and the startup resistor R7. The primary power current path is formed by the transformer's primary winding, the NPN transistor, the ACT365 internal MOSFET and the current sense resistor R9. The network consisting of capacitor C4 and diode D6 provides a VDD supply voltage for ACT365 from the auxiliary winding of the transformer. C4 is the decoupling capacitor of the supply voltage and energy storage component for startup. The diode D8 and the capacitor C5/C6 rectifies and filters the output voltage. The resistor divider consisting of R5 and R6 programs the output voltage.

The minimum and maximum DC input voltages can be calculated:

$$V_{INDCMIN} = \sqrt{2V_{ACMIN}^2 - \frac{2P_{OUT}\left(\frac{1}{2f_L} - t_C\right)}{\eta \times C_{IN}}}$$

$$= \sqrt{2 \times 85^2 - \frac{2 \times 10.5\left(\frac{1}{2 \times 50} - 4.5ms\right)}{76\% \times 2 \times 10\,\mu F}} \approx 90V \quad (3)$$

$$V_{INDCMAX} = \sqrt{2} \times V_{ACMAX} = \sqrt{2} \times 265 = 375V \quad (4)$$

## TYPICAL APPLICATION CONT'D

where η is the estimated circuit efficiency, $f_L$ is the line frequency, $t_C$ is the estimated rectifier conduction time, $C_{IN}$ is empirically selected to be 2 × 10μF electrolytic capacitors based on the 2μF/W rule of thumb.

When the transistor is turned off, the voltage on the transistor's collector consists of the input voltage and the reflected voltage from the transformer's secondary winding. There is a ringing on the rising top edge of the flyback voltage due to the leakage inductance of the transformer. This ringing is clamped by a RCD network if it is used. Design this clamped voltage as 50V below the breakdown of the NPN transistor. The flyback voltage has to be considered with selection of the maximum reverse voltage rating of secondary rectifier diode. If a 40V Schottky diode is used, then the flyback voltage can be calculated:

$$V_{RO} = \frac{V_{INDCMAX} \times (V_{OUTCV} + V_{DS})}{V_{DREV} - V_{OUTCV}} = \frac{375 \times (5 + 0.5)}{40 \times 0.8 - 5} = 76V \quad (5)$$

where $V_{DS}$ is the Schottky diode forward voltage, $V_{DREV}$ is the maximum reverse voltage rating of the diode and $V_{OUTCV}$ is the output voltage.

The maximum duty cycle is set to be 46% at low line voltage 85$V_{AC}$ and the circuit efficiency is estimated to be 76%. Then the full load input current is:

$$I_{IN} = \frac{V_{OUTCV} \times I_{OUTPL}}{V_{INDCMIN} \times \eta} = \frac{5 \times 2.1}{90 \times 76\%} = 153.5mA \quad (6)$$

The maximum input primary peak current at full load base on duty of 46%:

$$I_{PK} = \frac{2 \times I_{IN}}{D} = \frac{2 \times 153.5}{46\%} = 667\ mA \quad (7)$$

The primary inductance of the transformer:

$$L_P = \frac{V_{INDCMIN} \times D}{I_{PK} \times f_{SW}} = \frac{90 \times 46\%}{667\ mA \times 60\ kHz} \approx 1.0mH \quad (8)$$

ACT365 needs to work in DCM in all conditions, thus $N_P/N_S$ should meet

$$\frac{L_P \times I_{PK}}{V_{INDCMIN}} + \frac{L_P \times I_{PK}}{(V_{OUTCV} + V_{DS}) \times \frac{N_P}{N_S}} < \frac{0.9}{f_{SW}} \Rightarrow \frac{N_P}{N_S} > 16.16 \quad (9)$$

The auxiliary to secondary turns ratio $N_A/N_S$:

$$\frac{N_A}{N_S} = \frac{V_{DD} + V_{DA} + V_R}{V_{OUTCV} + V_{DS} + V_{CORD}} = \frac{11 + 0.25 + 1}{5 + 0.3 + 0.35} \approx 2.2 \quad (10)$$

Where $V_{DA}$ is diode forward voltage of the auxiliary side and $V_R$ is the resister voltage.
An EPC17 transformer gapped core with an effective inductance $A_{LE}$ of 80nH/$T^2$ is selected. The number of turns of the primary winding is:

$$N_P = \sqrt{\frac{L_P}{A_{LE}}} = \sqrt{\frac{1.0mH}{80nH / T^2}} = 110 \quad (11)$$

The number of turns of secondary and auxiliary windings can be derived when Np/Ns=14:

$$N_S = \frac{N_S}{N_P} \times N_P = \frac{1}{14} \times 110 \approx 8 \quad (12)$$

$$N_A = \frac{N_A}{N_S} \times N_S = 2.2 \times 9 = 20 \quad (13)$$

The current sense resistance ($R_{CS}$) determines the current limit value based on the following equation:

$$R_{CS} = \frac{0.9 \times V_{CSLIM}}{\sqrt{\frac{(I_{OUTFL} + I_{OUTMAX}) \times (V_{OUT} + V_{DS})}{L_P \times f_{SW} \times \left(\frac{\eta_{system}}{\eta_{xfm}}\right)}}} = \frac{0.9 \times 0.396}{\sqrt{\frac{(2.1 + 2.5) \times 5.3}{1.0 \times 60 \times \left(\frac{0.76}{0.89}\right)}}} = 0.52R \quad (14)$$

The voltage feedback resistors are selected according to below equation:

$$R_{FB1} = \frac{N_A}{N_P} \times \frac{L_P}{R_{CS}} \times K = \frac{20}{110} \times \frac{1.0}{0.52} \times 200000 \approx 68k \quad (15)$$

In actual application 66.5K is selected.

Where K is IC constant and K = 200000.

$$R_{FB2} = \frac{V_{FB}}{(V_{OUTCV} + V_{DS}) \frac{N_A}{N_S} - V_{FB}} R_{FB1} \quad (16)$$

$$= \frac{2.20}{(5 + 0.45) \times 2.2 - 2.20} \times 66.5K \approx 15k$$

When selecting the output capacitor, a low ESR electrolytic capacitor is recommended to minimize ripple from the current ripple. The approximate equation for the output capacitance value is given by:

$$C_{OUT} = \frac{I_{OUTCC} \times D}{f_{SW} \times \triangle V_{RIPPLE}} = \frac{2.1 \times 0.46}{60kHz \times 50mV} = 320\mu F \quad (17)$$

A 1000μF electrolytic capacitor is used to keep the ripple small.

### PCB Layout Guideline

Good PCB layout is critical to have optimal performance. Decoupling capacitor (C4), current sense resistor (R9) and feedback resistor (R5/R6) should be placed close to $V_{DD}$, CS and FB pins respectively. There are two main power path loops. One is formed by C1/C2, primary winding, NPN transistor and the ACT365. The other is the secondary winding, rectifier D8 and output capacitors (C5,C6). Keep these loop areas as small as possible. Connect high current ground returns,

## TYPICAL APPLICATION CONT'D

the input capacitor ground lead, and the ACT365 G pin to a single point (star ground configuration).

### $V_{FB}$ Sampling Waveforms

ACT365 senses the output voltage information through the $V_{FB}$ waveforms. Proper $V_{FB}$ waveforms are required for IC to operate in a stable status. To avoid mis-sampling, 1.0μs blanking time is added to blank the ringing period due to the leakage inductance and the circuit parasitic capacitance.

Figure 2 is the recommended $V_{FB}$ waveform to guarantee the correct sampling point so that the output information can be sent back into the IC to do the appropriate control.

**Figure 2:**

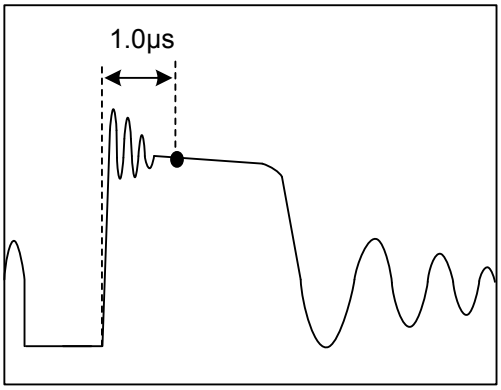


**Figure 3:**

**Universal VAC Input, 5V/2.1A Output Adapter**

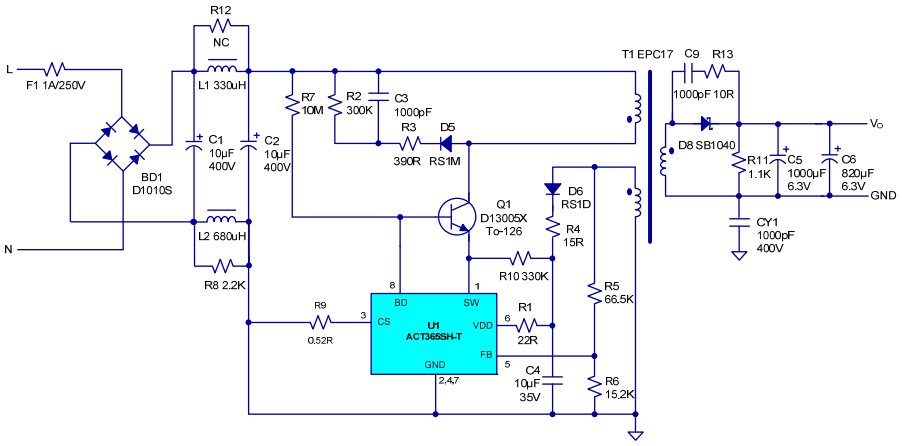



**Table 2:**

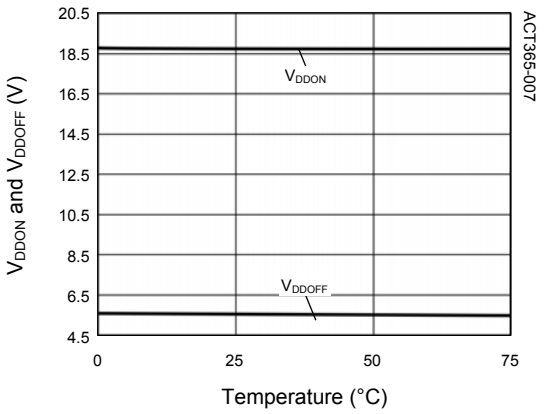
**ACT365 Bill of Materials**

| ITEM | REFERENCE | DESCRIPTION | QTY | MANUFACTURER |
|---|---|---|---|---|
| 1 | C1, C2 | Capacitor, Electrolytic, 10µF/400V, 10×16mm | 2 | KSC |
| 2 | C3 | Capacitor, Ceramic,1000pF/500V,1206,SMD | 1 | POE |
| 3 | C4 | Capacitor, Ceramic, 10µF/35V,1206,SMD | 1 | KSC |
| 4 | C5 | Capacitor, Electrolytic, 1000µF/6.3V, 8 ×16mm | 1 | KSC |
| 5 | C6 | Capacitor, Electrolytic, 820µF/6.3V, 6.3 × 16mm | 1 | KSC |
| 6 | C9 | Capacitor, Ceramic,1000pF/50V,0805,SMD | 1 | POE |
| 7 | CY1 | Safety Y1,Capacitor,1000pF/400V,Dip | 1 | UXT |
| 8 | BD1 | Bridge Rectifier,D1010S,1000V/1.0A,SDIP | 1 | PANJIT |
| 9 | D5 | Fast Recovery Rectifier, RS1M,1000V/1.0A, RMA | 1 | PANJIT |
| 10 | D6 | Fast Recovery Recti-fier,RS1D,200V/1.0A,SMA | 1 | PANJIT |
| 11 | D8 | Diode, Schottky, 40V/10A, PDS1040L, SMD | 1 | Diodes |
| 12 | L1 | Choke Coil, 330uH, 0410, DIP | 1 | Amode Tech |
| 13 | L2 | Axial Inductor, 680uH, ¢6x8mm, DIP | 1 | Amode Tech |
| 14 | Q1 | Transistor, NPN, 700V,D13005,TO-126 | 1 | Huawei |
| 15 | F1 | Fuse:1A 250V 3.6*10mm With Pigtail, ce-ramic tube | 1 | walter |
| 16 | R1 | Chip Resistor, 22Ω, 0805, 5% | 1 | TY-OHM |
| 17 | R2 | Chip Resistor, 300k,1206, 5% | 1 | TY-OHM |
| 18 | R3 | Chip Resistor, 390Ω,1206, 5% | 1 | TY-OHM |
| 19 | R4 | Chip Resistor, 15Ω, 0805, 5% | 1 | TY-OHM |
| 20 | R5 | Chip Resistor, 66.5k,0805, 1% | 1 | TY-OHM |
| 21 | R6 | Chip Resistor,15.2k,0805, 1% | 1 | TY-OHM |
| 21 | R7 | Chip Resistor, 10MΩ, 1206, 5% | 2 | TY-OHM |
| 22 | R8 | Chip Resistor, 2.2KΩ, 0805, 5% | 2 | TY-OHM |
| 23 | R9 | Chip Resistor, 0.52Ω,1206, 1% | 1 | TY-OHM |
| 24 | R10 | Chip Resistor, 330k,0805, 5% | 1 | TY-OHM |
| 25 | R11 | Chip Resistor, 1.1k, 0805, 5% | 1 | TY-OHM |
| 26 | R13 | Chip Resistor, 10Ω, 0805, 5% | 1 | TY-OHM |
| 27 | T1 | Transformer, $L_P$ = 1.0mH±7%, EPC17 | 1 | |
| 28 | USB | Double-layer USB Rev:A | 1 | |
| 29 | U1 | IC, ACT365SH-T, SOP-8 | 1 | Active-Semi |

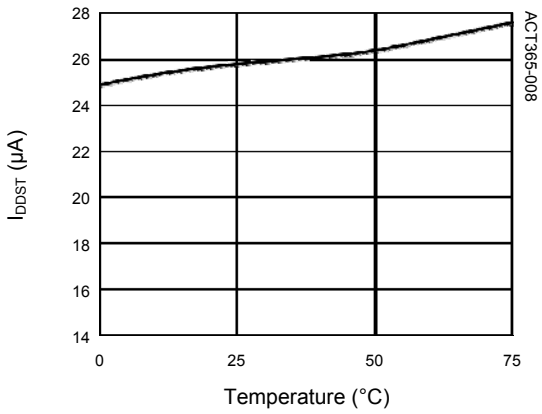
# TYPICAL PERFORMANCE CHARACTERISTICS CONT'D

(Circuit of Figure 6, unless otherwise specified.)

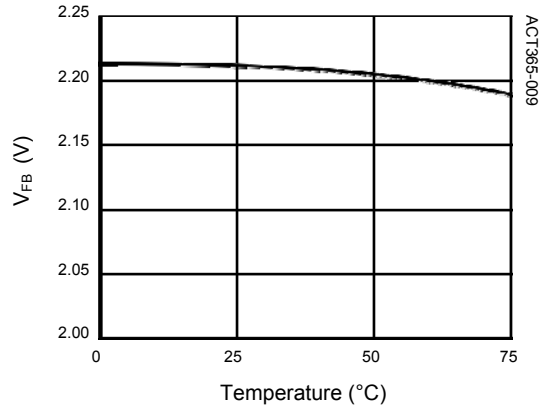
**VDD ON/OFF Voltage vs. Temperature**



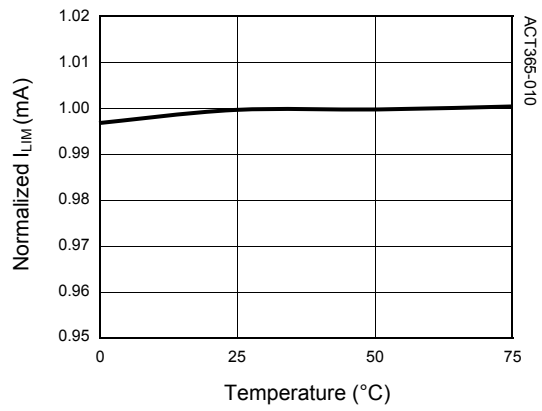

**Start Up Supply Current vs. Temperature**



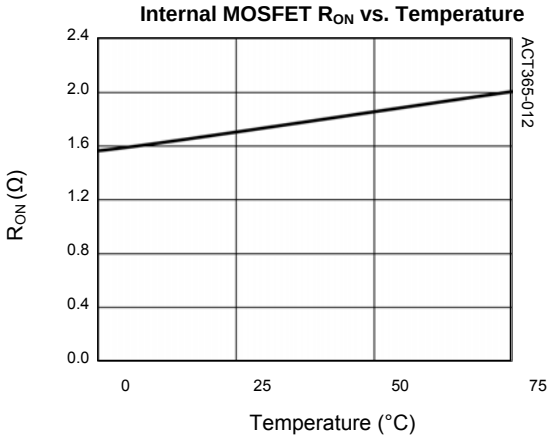

**FB Voltage vs. Temperature**




**Normalized $I_{LIM}$ vs. Temperature**

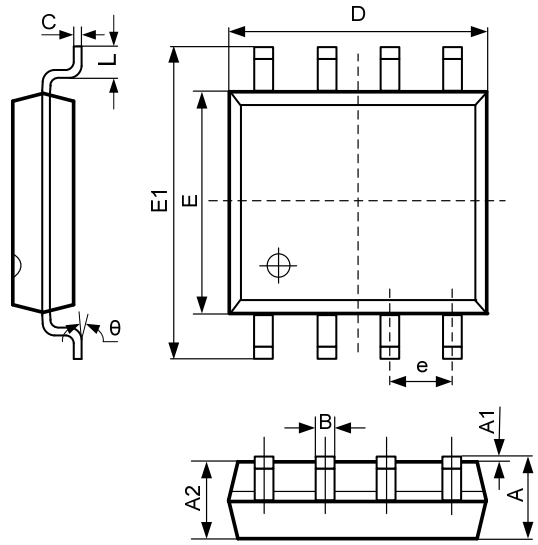



**Internal MOSFET $R_{ON}$ vs. Temperature**



# PACKAGE OUTLINE

## SOP-8 PACKAGE OUTLINE AND DIMENSIONS




| SYMBOL | DIMENSION IN MILLIMETERS | | DIMENSION IN INCHES | |
|---|---|---|---|---|
| | MIN | MAX | MIN | MAX |
| A | 1.350 | 1.750 | 0.053 | 0.069 |
| A1 | 0.100 | 0.250 | 0.004 | 0.010 |
| A2 | 1.250 | 1.650 | 0.049 | 0.065 |
| B | 0.310 | 0.510 | 0.012 | 0.020 |
| C | 0.100 | 0.250 | 0.004 | 0.010 |
| D | 4.700 | 5.100 | 0.185 | 0.201 |
| E | 3.800 | 4.000 | 0.150 | 0.157 |
| E1 | 5.800 | 6.200 | 0.228 | 0.244 |
| e | 1.270 TYP | | 0.050 TYP | |
| L | 0.400 | 1.270 | 0.016 | 0.050 |
| θ | 0° | 8° | 0° | 8° |

Note:
1. Dimension D does not include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.15mm per end.
2. Dimension E does not include interlead flash or protrusion. Interlead flash or protrusion shall not exceed 0.25mm per side.