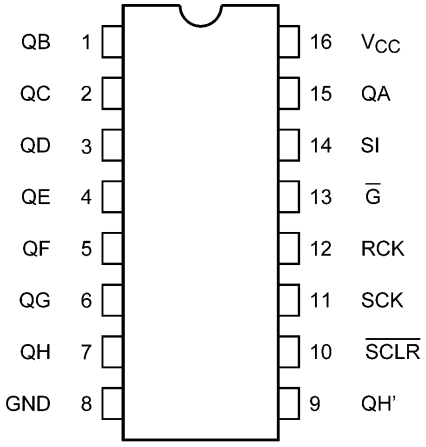
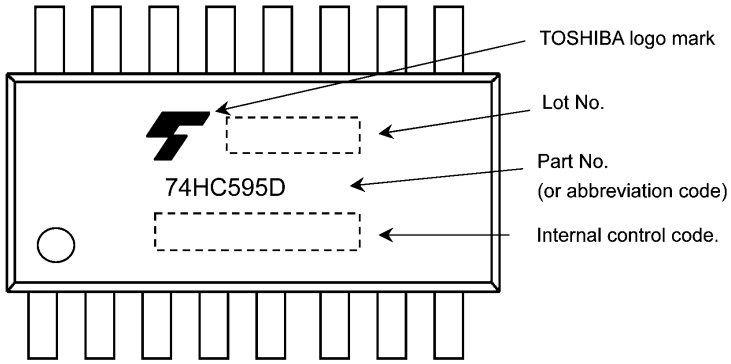
5. Pin Assignment

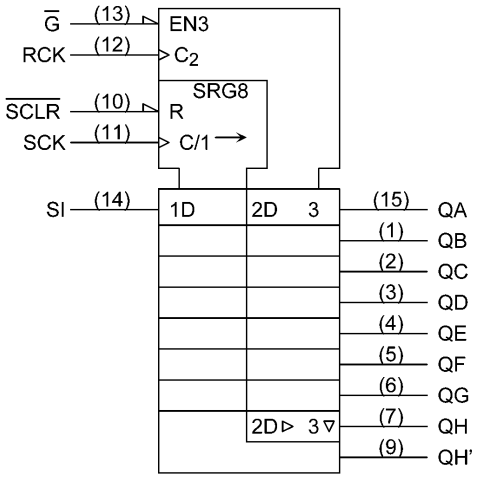


(top view)

6. Marking



7. IEC Logic Symbol

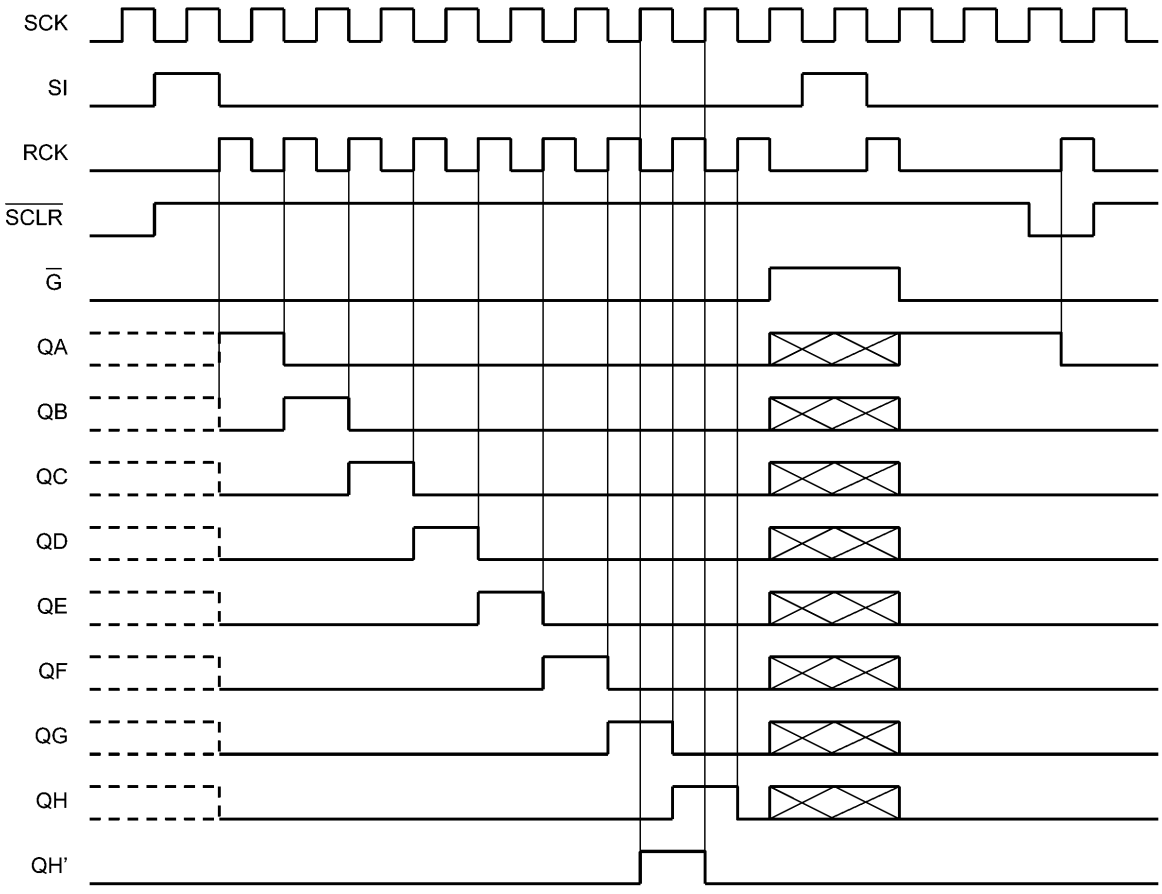


8. Truth Table

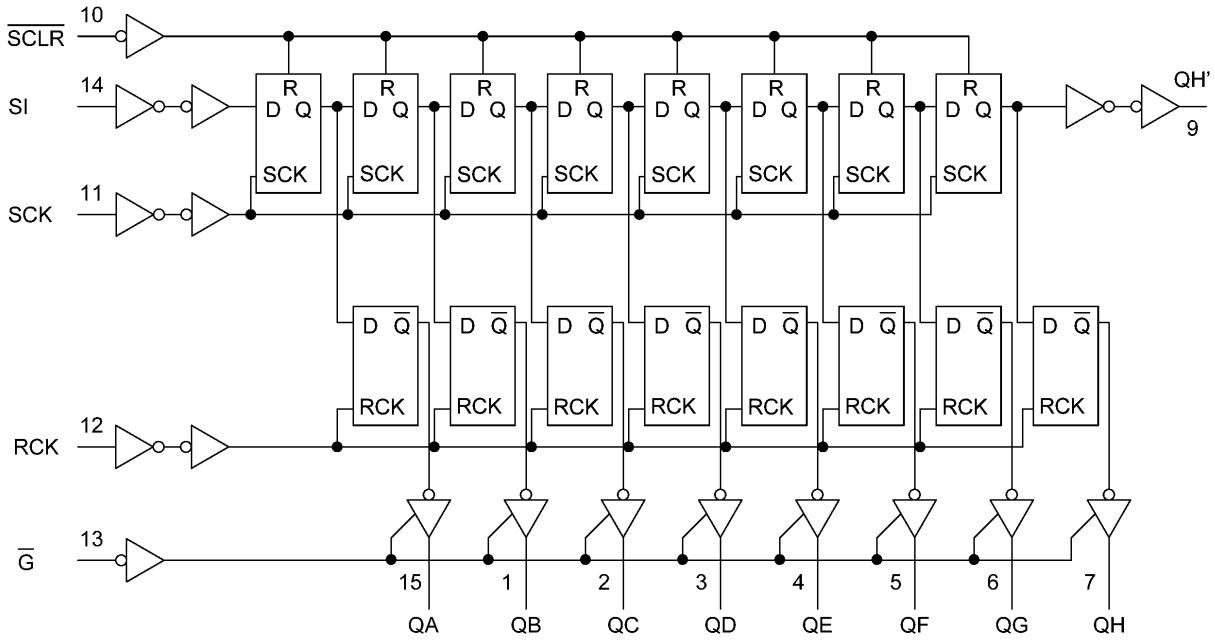
Inputs					Function
SI	SCK	$\overline{SCLR}$	RCK	$\overline{G}$	
X	X	X	X	H	QA thru QH outputs disable
X	X	X	X	L	QA thru QH outputs enable
X	X	L	X	X	Shift register is cleared.
L	↑	H	X	X	First stage of S.R. becomes “L”. Other stages store the data of previous stage, respectively.
H	↑	H	X	X	First stage of S.R. becomes “H”. Other stages store the data of previous stage, respectively.
X	↓	H	X	X	State of S.R. is not changed.
X	X	X	↑	X	S.R. data is stored into storage register.
X	X	X	↓	X	Storage register stage is not changed.

X: Don't care

9. Timing Chart



10. System Diagram



11. Absolute Maximum Ratings (Note)

Characteristics	Symbol	Note	Rating	Unit
Supply voltage	V_{CC}		-0.5 to 7.0	V
Input voltage	V_{IN}		-0.5 to V_{CC} + 0.5	V
Output voltage	V_{OUT}		-0.5 to V_{CC} + 0.5	V
Input diode current	I_{IK}		±20	mA
Output diode current	I_{OK}		±20	mA
Output current (QH')	I_{OUT}		±25	mA
Output current (QA to QH)			±35	
V_{CC}/ground current	I_{CC}		±75	mA
Power dissipation	P_D	(Note 1)	500	mW
Storage temperature	T_{stg}		-65 to 150	°C

Note: Exceeding any of the absolute maximum ratings, even briefly, lead to deterioration in IC performance or even destruction.

Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook (“Handling Precautions”/“Derating Concept and Methods”) and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note 1: P_D derates linearly with -8 mW/°C above 85 °C

12. Operating Ranges (Note)

Characteristics	Symbol	Test Condition	Rating	Unit
Supply voltage	V_{CC}	—	2.0 to 6.0	V
Input voltage	V_{IN}	—	0 to V_{CC}	V
Output voltage	V_{OUT}	—	0 to V_{CC}	V
Operating temperature	T_{opr}	—	-40 to 125	°C
Input rise and fall times	t_r,t_f	—	0 to 50	μs

Note: The operating ranges must be maintained to ensure the normal operation of the device.
Unused inputs must be tied to either V_{CC} or GND.

13. Electrical Characteristics

13.1. DC Characteristics (Unless otherwise specified, T_a = 25 °C)

Characteristics	Symbol	Test Condition		V_{CC} (V)	Min	Typ.	Max	Unit
High-level input voltage	V_{IH}	—		2.0	1.50	—	—	V
				4.5	3.15	—	—	
				6.0	4.20	—	—	
Low-level input voltage	V_{IL}	—		2.0	—	—	0.50	V
				4.5	—	—	1.35	
				6.0	—	—	1.80	
High-level output voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} = -20 μA	2.0	1.9	2.0	—	V
				4.5	4.4	4.5	—	
				6.0	5.9	6.0	—	
High-level output voltage QH'			I_{OH} = -4 mA	4.5	4.18	4.31	—	
			I_{OH} = -5.2 mA	6.0	5.68	5.80	—	
High-level output voltage QA to QH			I_{OH} = -6 mA	4.5	4.18	4.31	—	
			I_{OH} = -7.8 mA	6.0	5.68	5.80	—	
Low-level output voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} = 20 μA	2.0	—	0.0	0.1	V
				4.5	—	0.0	0.1	
				6.0	—	0.0	0.1	
Low-level output voltage QH'			I_{OL} = 4 mA	4.5	—	0.17	0.26	
			I_{OL} = 5.2 mA	6.0	—	0.18	0.26	
Low-level output voltage QA to QH			I_{OL} = 6 mA	4.5	—	0.17	0.26	
			I_{OL} = 7.8 mA	6.0	—	0.18	0.26	
3-state output OFF-state leakage current	I_{OZ}	V_{IN} = V_{IH} or V_{IL} V_{OUT} = V_{CC} or GND		6.0	—	—	±0.5	μA
Input leakage current	I_{IN}	V_{IN} = V_{CC} or GND		6.0	—	—	±0.1	μA
Quiescent supply current	I_{CC}	V_{IN} = V_{CC} or GND		6.0	—	—	4.0	μA

13.2. DC Characteristics (Unless otherwise specified, T_a = -40 to 85 °C)

Characteristics	Symbol	Test Condition		V_{CC} (V)	Min	Max	Unit
High-level input voltage	V_{IH}	—		2.0	1.50	—	V
				4.5	3.15	—	
				6.0	4.20	—	
Low-level input voltage	V_{IL}	—		2.0	—	0.50	V
				4.5	—	1.35	
				6.0	—	1.80	
High-level output voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} = -20 μA	2.0	1.9	—	V
				4.5	4.4	—	
				6.0	5.9	—	
High-level output voltage QH'			I_{OH} = -4 mA	4.5	4.13	—	
			I_{OH} = -5.2 mA	6.0	5.63	—	
High-level output voltage QA to QH			I_{OH} = -6 mA	4.5	4.13	—	
			I_{OH} = -7.8 mA	6.0	5.63	—	
Low-level output voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} = 20 μA	2.0	—	0.1	V
				4.5	—	0.1	
				6.0	—	0.1	
Low-level output voltage QH'			I_{OL} = 4 mA	4.5	—	0.33	
			I_{OL} = 5.2 mA	6.0	—	0.33	
Low-level output voltage QA to QH			I_{OL} = 6 mA	4.5	—	0.33	
			I_{OL} = 7.8 mA	6.0	—	0.33	
3-state output OFF-state leakage current	I_{OZ}	V_{IN} = V_{IH} or V_{IL} V_{OUT} = V_{CC} or GND		6.0	—	±5.0	μA
Input leakage current	I_{IN}	V_{IN} = V_{CC} or GND		6.0	—	±1.0	μA
Quiescent supply current	I_{CC}	V_{IN} = V_{CC} or GND		6.0	—	40.0	μA

13.3. DC Characteristics (Unless otherwise specified, T_a = -40 to 125 °C)

Characteristics	Symbol	Test Condition		V_{CC} (V)	Min	Max	Unit
High-level input voltage	V_{IH}	—		2.0	1.50	—	V
				4.5	3.15	—	
				6.0	4.20	—	
Low-level input voltage	V_{IL}	—		2.0	—	0.50	V
				4.5	—	1.35	
				6.0	—	1.80	
High-level output voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} = -20 μA	2.0	1.9	—	V
				4.5	4.4	—	
				6.0	5.9	—	
High-level output voltage QH'			I_{OH} = -4 mA	4.5	3.7	—	
			I_{OH} = -5.2 mA	6.0	5.2	—	
High-level output voltage QA to QH			I_{OH} = -6 mA	4.5	3.7	—	
			I_{OH} = -7.8 mA	6.0	5.2	—	
Low-level output voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} = 20 μA	2.0	—	0.1	V
				4.5	—	0.1	
				6.0	—	0.1	
Low-level output voltage QH'			I_{OL} = 4 mA	4.5	—	0.4	
			I_{OL} = 5.2 mA	6.0	—	0.4	
Low-level output voltage QA to QH			I_{OL} = 6 mA	4.5	—	0.4	
			I_{OL} = 7.8 mA	6.0	—	0.4	
3-state output OFF-state leakage current	I_{OZ}	V_{IN} = V_{IH} or V_{IL} V_{OUT} = V_{CC} or GND		6.0	—	±10.0	μA
Input leakage current	I_{IN}	V_{IN} = V_{CC} or GND		6.0	—	±1.0	μA
Quiescent supply current	I_{CC}	V_{IN} = V_{CC} or GND		6.0	—	160.0	μA

13.4. Timing Requirements (Unless otherwise specified, T_a = 25 °C, Input: $t_r = t_f$ = 6 ns)

Characteristics	Symbol	Test Condition	V_{CC} (V)	Limit	Unit
Minimum pulse width (SCK, RCK)	$t_{w(L)}$,$t_{w(H)}$	See 14. AC Waveform, Fig. 14.2	2.0	75	ns
			4.5	15	
			6.0	13	
Minimum pulse width ($\overline{SCLR}$)	$t_{w(L)}$	See 14. AC Waveform, Fig. 14.2	2.0	75	ns
			4.5	15	
			6.0	13	
Minimum setup time (SI-SCK)	t_S	See 14. AC Waveform, Fig. 14.2	2.0	50	ns
			4.5	10	
			6.0	9	
Minimum setup time (SCK - RCK)	t_S	See 14. AC Waveform, Fig. 14.2	2.0	75	ns
			4.5	15	
			6.0	13	
Minimum setup time ($\overline{SCLR}$ -RCK)	t_S	See 14. AC Waveform, Fig. 14.2	2.0	100	ns
			4.5	20	
			6.0	17	
Minimum hold time	t_h	See 14. AC Waveform, Fig. 14.2	2.0	0	ns
			4.5	0	
			6.0	0	
Minimum removal time ($\overline{SCLR}$)	t_{rem}	See 14. AC Waveform, Fig. 14.2	2.0	50	ns
			4.5	10	
			6.0	9	
Clock frequency	f	—	2.0	6	MHz
			4.5	30	
			6.0	35	

13.5. Timing Requirements (Unless otherwise specified, T_a = -40 to 85 °C, Input: $t_r = t_f$ = 6 ns)

Characteristics	Symbol	Test Condition	V_{CC} (V)	Limit	Unit
Minimum pulse width (SCK, RCK)	$t_{w(L)}$,$t_{w(H)}$	See 14. AC Waveform, Fig. 14.2	2.0	95	ns
			4.5	19	
			6.0	16	
Minimum pulse width ($\overline{SCLR}$)	$t_{w(L)}$	See 14. AC Waveform, Fig. 14.2	2.0	95	ns
			4.5	19	
			6.0	16	
Minimum setup time (SI-SCK)	t_S	See 14. AC Waveform, Fig. 14.2	2.0	65	ns
			4.5	13	
			6.0	11	
Minimum setup time (SCK - RCK)	t_S	See 14. AC Waveform, Fig. 14.2	2.0	95	ns
			4.5	19	
			6.0	16	
Minimum setup time ($\overline{SCLR}$ -RCK)	t_S	See 14. AC Waveform, Fig. 14.2	2.0	125	ns
			4.5	25	
			6.0	21	
Minimum hold time	t_h	See 14. AC Waveform, Fig. 14.2	2.0	0	ns
			4.5	0	
			6.0	0	
Minimum removal time ($\overline{SCLR}$)	t_{rem}	See 14. AC Waveform, Fig. 14.2	2.0	65	ns
			4.5	13	
			6.0	11	
Clock frequency	f	—	2.0	5	MHz
			4.5	25	
			6.0	28	

13.6. Timing Requirements (Unless otherwise specified, T_a = -40 to 125 °C, Input: $t_r = t_f$ = 6 ns)

Characteristics	Symbol	Test Condition	V_{CC} (V)	Limit	Unit
Minimum pulse width (SCK, RCK)	$t_{w(L)}$,$t_{w(H)}$	See 14. AC Waveform, Fig. 14.2	2.0	110	ns
			4.5	22	
			6.0	19	
Minimum pulse width ($\overline{SCLR}$)	$t_{w(L)}$	See 14. AC Waveform, Fig. 14.2	2.0	110	ns
			4.5	22	
			6.0	19	
Minimum setup time (SI-SCK)	t_S	See 14. AC Waveform, Fig. 14.2	2.0	75	ns
			4.5	15	
			6.0	13	
Minimum setup time (SCK - RCK)	t_S	See 14. AC Waveform, Fig. 14.2	2.0	110	ns
			4.5	22	
			6.0	19	
Minimum setup time ($\overline{SCLR}$ -RCK)	t_S	See 14. AC Waveform, Fig. 14.2	2.0	150	ns
			4.5	30	
			6.0	26	
Minimum hold time	t_h	See 14. AC Waveform, Fig. 14.2	2.0	0	ns
			4.5	0	
			6.0	0	
Minimum removal time ($\overline{SCLR}$)	t_{rem}	See 14. AC Waveform, Fig. 14.2	2.0	75	ns
			4.5	15	
			6.0	13	
Clock frequency	f	—	2.0	4	MHz
			4.5	20	
			6.0	24	

13.7. AC Characteristics (Unless otherwise specified, C_L = 15 pF, V_{CC} = 5 V, T_a = 25 °C, Input: $t_r = t_f$ = 6 ns)

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Output transition time (QH')	t_{TLH},t_{THL}	See 14. AC Waveform, Fig. 14.1	—	4	8	ns
Propagation delay time (SCK-QH')	t_{PLH},t_{PHL}	See 14. AC Waveform, Fig. 14.1	—	12	21	
Propagation delay time($\overline{SCLR}$-QH')	t_{PHL}	See 14. AC Waveform, Fig. 14.1	—	15	30	
Maximum clock frequency	f_{MAX}	—	35	55	—	MHz

13.8. AC Characteristics (Unless otherwise specified, T_a = 25 °C, Input: $t_r = t_f$ = 6 ns)

Characteristics	Symbol	Note	Test Condition	C_L (pF)	V_{CC} (V)	Min	Typ.	Max	Unit
Output transition time (Qn)	t_{TLH},t_{THL}		See 14. AC Waveform, Fig. 14.1	50	2.0	—	25	60	ns
					4.5	—	7	12	
					6.0	—	6	10	
Output transition time (QH')	t_{TLH},t_{THL}		See 14. AC Waveform, Fig. 14.1	50	2.0	—	30	75	ns
					4.5	—	8	15	
					6.0	—	7	13	
Propagation delay time (SCK-QH')	t_{PLH},t_{PHL}		See 14. AC Waveform, Fig. 14.1	50	2.0	—	45	125	ns
					4.5	—	15	25	
					6.0	—	13	21	
Propagation delay time ($\overline{SCLR}$ -QH')	t_{PHL}		See 14. AC Waveform, Fig. 14.1	50	2.0	—	60	175	ns
					4.5	—	18	35	
					6.0	—	15	30	
Propagation delay time (RCK-Q_n)	t_{PLH},t_{PHL}		See 14. AC Waveform, Fig. 14.1	50	2.0	—	60	150	ns
					4.5	—	20	30	
					6.0	—	17	26	
				150	2.0	—	75	190	
					4.5	—	25	38	
					6.0	—	22	32	
Output enable time	t_{PZL},t_{PZH}		R_L = 1 kΩ	50	2.0	—	45	135	ns
					4.5	—	15	27	
					6.0	—	13	23	
				150	2.0	—	60	175	
					4.5	—	20	35	
					6.0	—	17	30	
Output disable time	t_{PLZ},t_{PHZ}		R_L = 1 kΩ	50	2.0	—	30	150	ns
					4.5	—	15	30	
					6.0	—	14	26	
Maximum clock frequency	f_{MAX}		—	50	2.0	6	17	—	MHz
					4.5	30	50	—	
					6.0	35	59	—	
Input capacitance	C_{IN}		—			—	3	—	pF
Power dissipation capacitance	C_{PD}	(Note 1)	—			—	41	—	pF

Note 1: C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation.

$I_{CC(opr)} = C_{PD} \times V_{CC} \times f_{IN} + I_{CC}$

13.9. AC Characteristics
(Unless otherwise specified, T_a = -40 to 85 °C, Input: $t_r = t_f$ = 6 ns)

Characteristics	Symbol	Test Condition	C_L (pF)	V_{CC} (V)	Min	Max	Unit
Output transition time (Qn)	t_{TLH},t_{THL}	See 14. AC Waveform, Fig. 14.1	50	2.0	—	75	ns
				4.5	—	15	
				6.0	—	13	
Output transition time (QH')	t_{TLH},t_{THL}	See 14. AC Waveform, Fig. 14.1	50	2.0	—	95	ns
				4.5	—	19	
				6.0	—	16	
Propagation delay time (SCK-QH')	t_{PLH},t_{PHL}	See 14. AC Waveform, Fig. 14.1	50	2.0	—	155	ns
				4.5	—	31	
				6.0	—	26	
Propagation delay time ($\overline{SCLR}$ -QH')	t_{PHL}	See 14. AC Waveform, Fig. 14.1	50	2.0	—	220	ns
				4.5	—	44	
				6.0	—	37	
Propagation delay time (RCK-Q_n)	t_{PLH},t_{PHL}	See 14. AC Waveform, Fig. 14.1	50	2.0	—	190	ns
				4.5	—	38	
				6.0	—	32	
			150	2.0	—	240	
				4.5	—	48	
				6.0	—	41	
Output enable time	t_{PZL},t_{PZH}	R_L = 1 kΩ	50	2.0	—	170	ns
				4.5	—	34	
				6.0	—	29	
			150	2.0	—	220	
				4.5	—	44	
				6.0	—	37	
Output disable time	t_{PLZ},t_{PHZ}	R_L = 1 kΩ	50	2.0	—	190	ns
				4.5	—	38	
				6.0	—	33	
Maximum clock frequency	f_{MAX}	—	50	2.0	5	—	MHz
				4.5	25	—	
				6.0	28	—	

13.10. AC Characteristics
(Unless otherwise specified, T_a = -40 to 125 °C, Input: $t_r = t_f$ = 6 ns)

Characteristics	Symbol	Test Condition	C_L (pF)	V_{CC} (V)	Min	Max	Unit
Output transition time (Qn)	t_{TLH},t_{THL}	See 14. AC Waveform, Fig. 14.1	50	2.0	—	90	ns
				4.5	—	18	
				6.0	—	15	
Output transition time (QH')	t_{TLH},t_{THL}	See 14. AC Waveform, Fig. 14.1	50	2.0	—	115	ns
				4.5	—	23	
				6.0	—	20	
Propagation delay time (SCK-QH')	t_{PLH},t_{PHL}	See 14. AC Waveform, Fig. 14.1	50	2.0	—	240	ns
				4.5	—	48	
				6.0	—	31	
Propagation delay time ($\overline{SCLR}$ -QH')	t_{PHL}	See 14. AC Waveform, Fig. 14.1	50	2.0	—	265	ns
				4.5	—	53	
				6.0	—	45	
Propagation delay time (RCK-Q_n)	t_{PLH},t_{PHL}	See 14. AC Waveform, Fig. 14.1	50	2.0	—	265	ns
				4.5	—	53	
				6.0	—	45	
			150	2.0	—	285	
				4.5	—	57	
				6.0	—	48	
Output enable time	t_{PZL},t_{PZH}	R_L = 1 kΩ	50	2.0	—	225	ns
				4.5	—	45	
				6.0	—	38	
			150	2.0	—	265	
				4.5	—	53	
				6.0	—	45	
Output disable time	t_{PLZ},t_{PHZ}	R_L = 1 kΩ	50	2.0	—	225	ns
				4.5	—	45	
				6.0	—	38	
Maximum clock frequency	f_{MAX}	—	50	2.0	4	—	MHz
				4.5	20	—	
				6.0	24	—	

14. AC Waveform

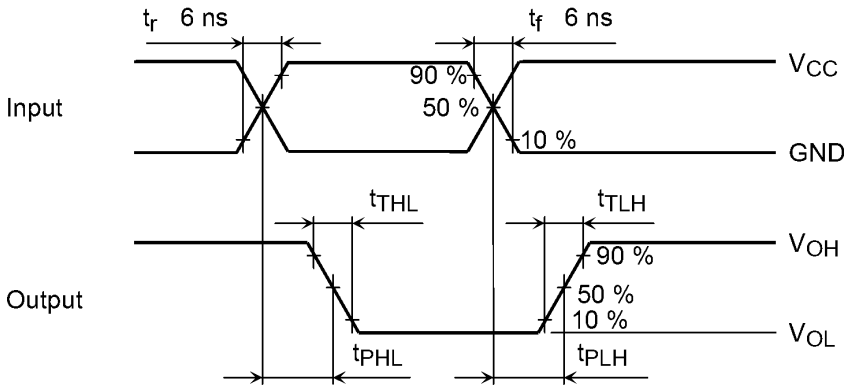


Fig. 14.1 t_{TLH}, t_{THL}, t_{PLH}, t_{PHL}

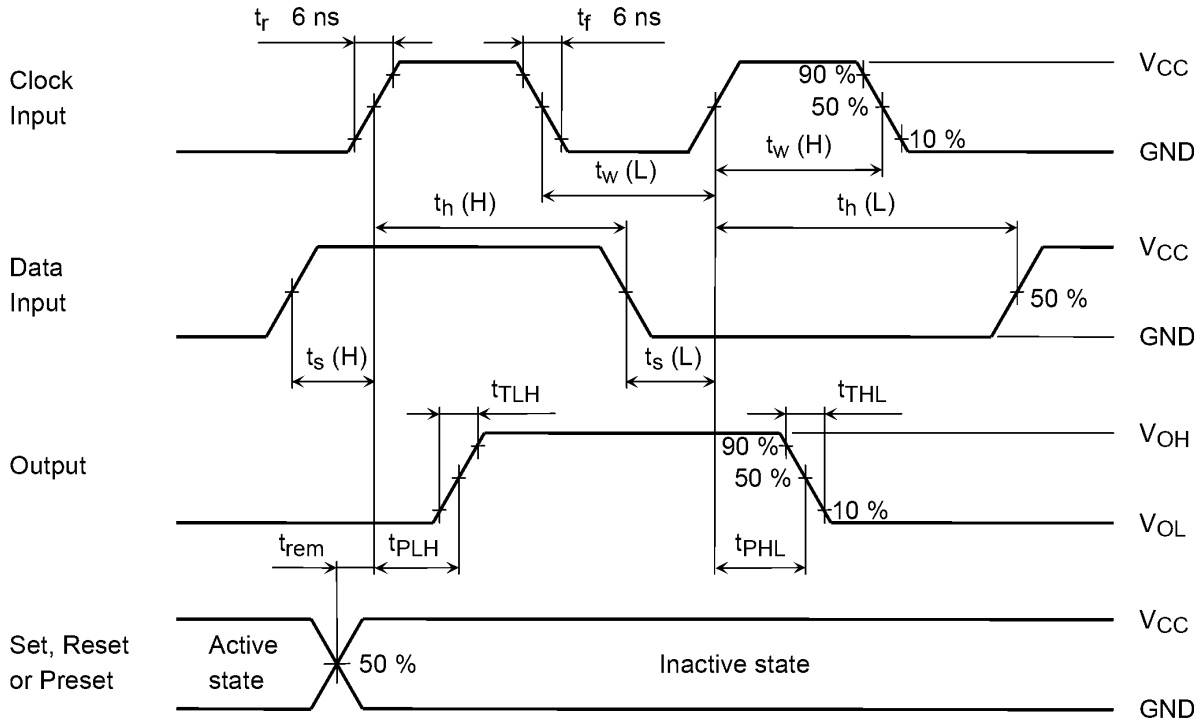
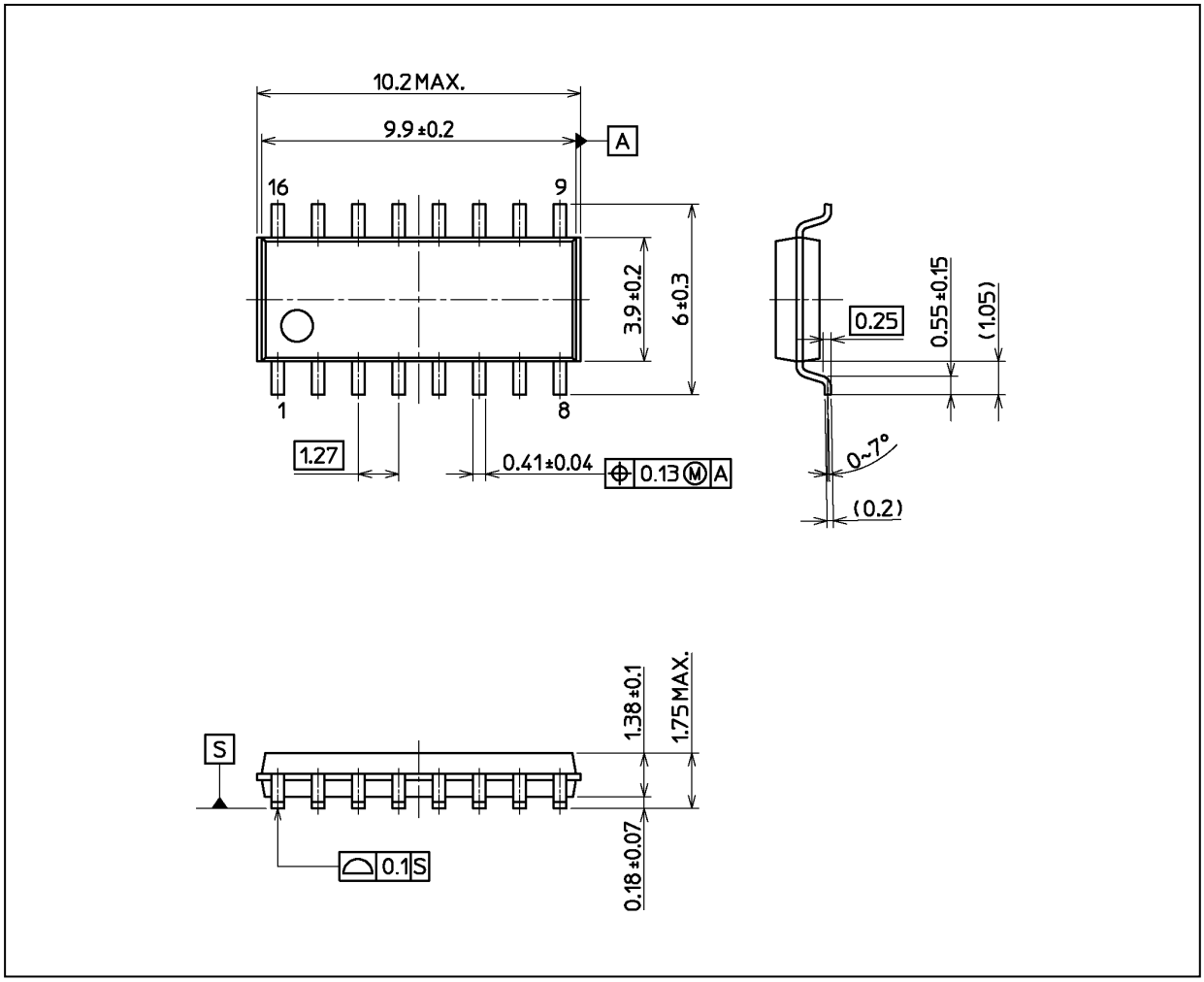


Fig. 14.2 t_w, t_s, t_h, t_{rem}

Package Dimensions

Unit: mm



Weight: 0.15 g (typ.)

Package Name(s)
Nickname: SOIC16

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