

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min	Max	Unit
Operating Temperature	T _A	-55	+125	°C
Storage Temperature	T _{STG}	-65	+150	°C
Signal Voltage Relative to GND	V _G	-0.5	4.6	V
Junction Temperature	T _J		150	°C
Supply Voltage	V _{CC}	-0.5	4.6	V

TRUTH TABLE

CS#	OE#	WE#	Mode	Data I/O	Power
H	X	X	Standby	High Z	Standby
L	L	H	Read	Data Out	Active
L	X	L	Write	Data In	Active
L	H	H	Out Disable	High Z	Active

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Max	Unit
Supply Voltage	V _{CC}	3.0	3.6	V
Input High Voltage	V _{IH}	2.2	V _{CC} + 0.3	V
Input Low Voltage	V _{IL}	-0.3	+0.8	V

CAPACITANCE

(T_A = +25°C)

Parameter	Symbol	Conditions	Max	Unit
OE# capacitance	C _{OE}	V _{IN} = 0 V, f = 1.0 MHz	30	pF
WE#1-4 capacitance	C _{WE}	V _{IN} = 0 V, f = 1.0 MHz	10	pF
CS#1-4 capacitance	C _{CS}	V _{IN} = 0 V, f = 1.0 MHz	10	pF
Data I/O capacitance	C _{I/O}	V _{I/O} = 0 V, f = 1.0 MHz	10	pF
Address input capacitance	C _{AD}	V _{IN} = 0 V, f = 1.0 MHz	30	pF

This parameter is guaranteed by design but not tested.

DC CHARACTERISTICS

(V_{CC} = 3.3V ± 0.3V, -55°C ≤ T_A ≤ 125°C)

Parameter	Sym	Conditions	Min	Max	Units
Input Leakage Current	I _{LI}	V _{IN} = GND to V _{CC}		10	μA
Output Leakage Current	I _{LO}	CS# = V _{IH} , OE# = V _{IH} , V _{OUT} = GND to V _{CC}		10	μA
Operating Supply Current (x 32 Mode)	I _{CC} x 32	CS# = V _{IL} , OE# = V _{IH} , f = 5MHz, V _{CC} = 3.6V		1100	mA
Standby Current	I _{SB}	CS# = V _{IH} , OE# = V _{IH} , f = 5MHz, V _{CC} = 3.6V		200	mA
Output Low Voltage	V _{OL}	I _{OL} = 8mA		0.4	V
Output High Voltage	V _{OH}	I _{OH} = -4.0mA	2.4		V

NOTE: DC test conditions: V_{IH} = V_{CC} - 0.3V, V_{IL} = 0.3V.

NOTE: Contact factory for low power option.

AC CHARACTERISTICS

(V_{CC} = 3.3V, -55°C ≤ TA ≤ +125°C)

Parameter Read Cycle	Symbol	-12		-15		-17		-20		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
Read Cycle Time	t _{RC}	12		15		17		20		ns
Address Access Time	t _{AA}		12		15		17		20	ns
Output Hold from Address Change	t _{OH}	3		3		3		3		ns
Chip Select Access Time	t _{ACS}		12		15		17		20	ns
Output Enable to Output Valid	t _{OE}		7		8		8		10	ns
Chip Select to Output in Low Z	t _{CLZ} ¹	3		3		3		3		ns
Output Enable to Output in Low Z	t _{OLZ} ¹	1		1		1		1		ns
Chip Disable to Output in High Z	t _{CHZ} ¹		7		8		8		10	ns
Output Disable to Output in High Z	t _{OHZ} ¹		7		8		8		10	ns.

1. This parameter is guaranteed by design but not tested

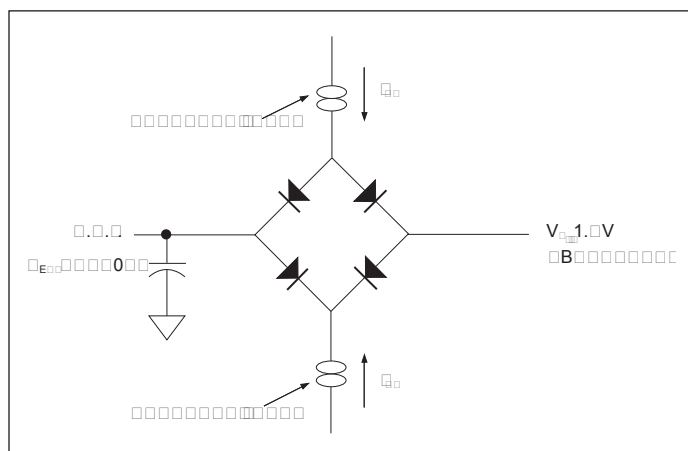
AC CHARACTERISTICS

(V_{CC} = 3.3V, -55°C ≤ TA ≤ +125°C)

Parameter Write Cycle	Symbol	-12		-15		-17		-20		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
Write Cycle Time	t _{WC}	12		15		17		20		ns
Chip Select to End of Write	t _{CW}	10		12		12		14		ns
Address Valid to End of Write	t _{AW}	10		12		12		14		ns
Data Valid to End of Write	t _{DW}	8		9		9		10		ns
Write Pulse Width	t _{WP}	10		12		14		14		ns
Address Setup Time	t _{AS}	0		0		0		0		ns
Address Hold Time	t _{AH}	0		0		0		0		ns
Output Active from End of Write	t _{OW} ¹	2		2		3		3		ns
Write Enable to Output in High Z	t _{WHZ} ¹		7		8		8		9	ns
Data Hold Time	t _{DH}	0		0		0		0		ns

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AC TEST CIRCUIT



AC TEST CONDITIONS

Parameter	Typ	Unit
Input Pulse Levels	V _{IL} = 0, V _{IH} = 2.5	V
Input Rise and Fall	5	ns
Input and Output Reference Level	1.5	V
Output Timing Reference Level	1.5	V

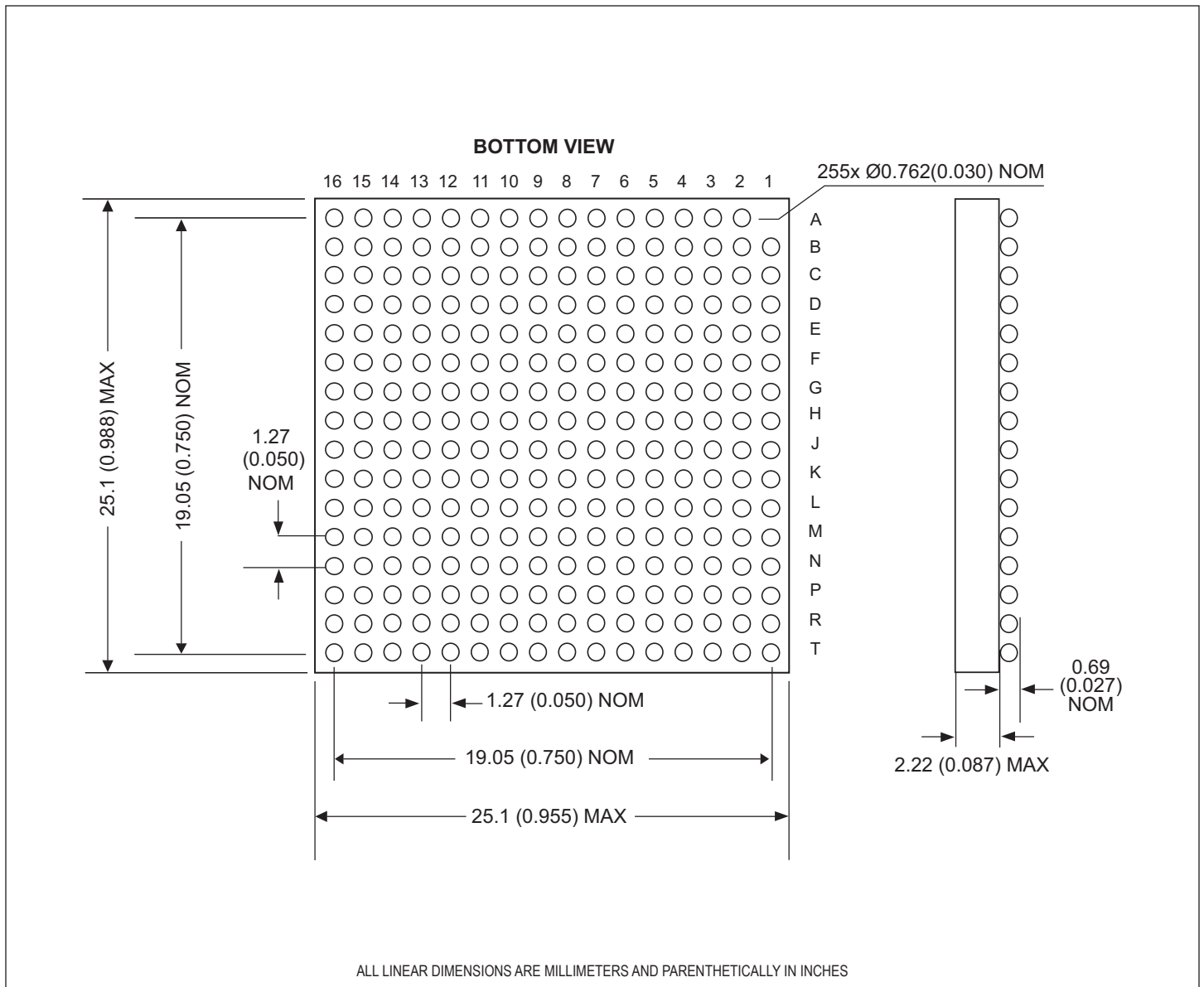
NOTES:

V_Z is programmable from -2V to +7V.I_{OL} & I_{OH} programmable from 0 to 16mA.Tester Impedance Z₀ = 75 Ω.V_Z is typically the midpoint of V_{OH} and V_{OL}.I_{OL} & I_{OH} are adjusted to simulate a typical resistive load circuit. ATE tester includes jig capacitance.

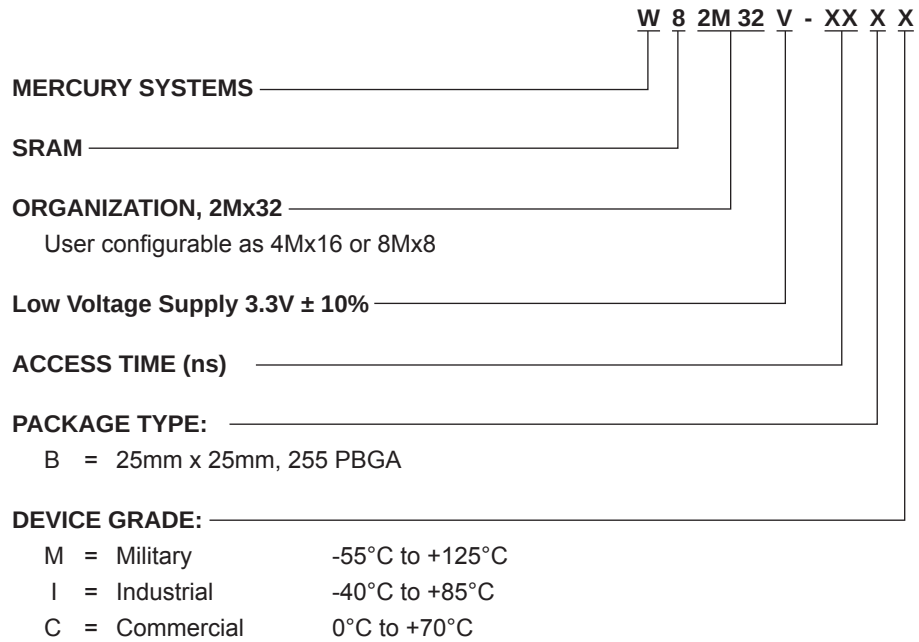
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WRITE CYCLE 1, WE# CONTROLLED

PACKAGE 781 – 255 BALL GRID ARRAY



ORDERING INFORMATION



Document Title

2M x 32 Asynchronous SRAM

Revision History

Rev #	History	Release Date	Status
Rev 0	Initial Release	July 2002	Advanced
Rev 1	Changes 1.1 Add AC/DC Electricals & Timing Diagrams (Pg. 1-7) 1.2 Change Pinout to full 255 (16x16) array 1.3 Change Package Dimension to full 255 (16x16) array	October 2002	Advanced
Rev 2	Changes (Pg.1,5,6,7) 2.1 Change package dimension from 27mm square to 25mm square 2.2 Change package height from 2.20mm to 2.70mm Max	May 2002	Advanced
Rev 3	Changes (Pg.1,5,7) 3.1 Change package mechanical drawing to new format.	November 2003	Advanced
Rev 4	Changes (Pg.1,7) 4.1 Change status to preliminary.	May 2004	Preliminary
Rev 5	Changes (Pg. 1, 7) 5.1 Change status to Final	April 2006	Final
Rev 6	Change (Pg. 5) 6.1 Change max height dimension to 2.21mm/0.087in	October 2008	Final
Rev 7	Change (Pg. 5) 7.1 Change standby current (I _{SB}) from 400 to 200mA	May 2009	Final
Rev 8	Changes (Pg. 1-7) 8.1 Change document layout from White Electronic Designs to Microsemi	April 2011	Final
Rev 9	Changes (Pg. All) (ECN 10156) 9.1 Change document layout from Microsemi to Mercury Systems	August 2016	Final