Features

- Industry's first IC with six Port Bypass Circuits (PBC) supporting both 1.0625 Gbps and 2.125 Gbps
 Fibre Channel data rates – dual mode provides flexibility by having one device for new and legacy designs
- Two FibreTimer[™] cells configurable as:
 - Repeaters for low latency
 - Retimers for true Fibre Channel compliance
 - Reduces external retimer components, provides design flexibility by allowing mixing and matching of the functions for design optimization
- Digital design of the FibreTimers produce a device that is well controlled over voltage, process and temperature variations provides a more robust and reliable design
- User-selectable, on-chip receive termination at either 100Ω or 150Ω
- Speed independent Tx and Rx paths aid in Fibre Channel auto-speed negotiation – allows the device to migrate as the specification evolves
- Device can be strapped for 1 or 2 Gbps operation supports dual speed storage applications
- World-class signal integrity for jitter compliance reduces debug and redesign efforts
- Two digital signal detect units to detect the presence of valid Fibre Channel encoded serial data - improves signal detect reliability
- User selectable pre-emphasis on all high-speed outputs - distorts outputs signal for improved signal driving over long trace and cable distances
- 106.25 MHz reference clock
- 5V-tolerant LVTTL inputs provides design flexibility and backward compatibility
- Cable equalization on all high-speed inputs Manages and corrects signal latency and distortion
- Single 2.5V supply reduces wiring complexity
- 100-pin, 14mm exposed pad TQFP package ideal for compact JBOD designs



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