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1 Block diagram and pin description

Figure 1. Block diagram

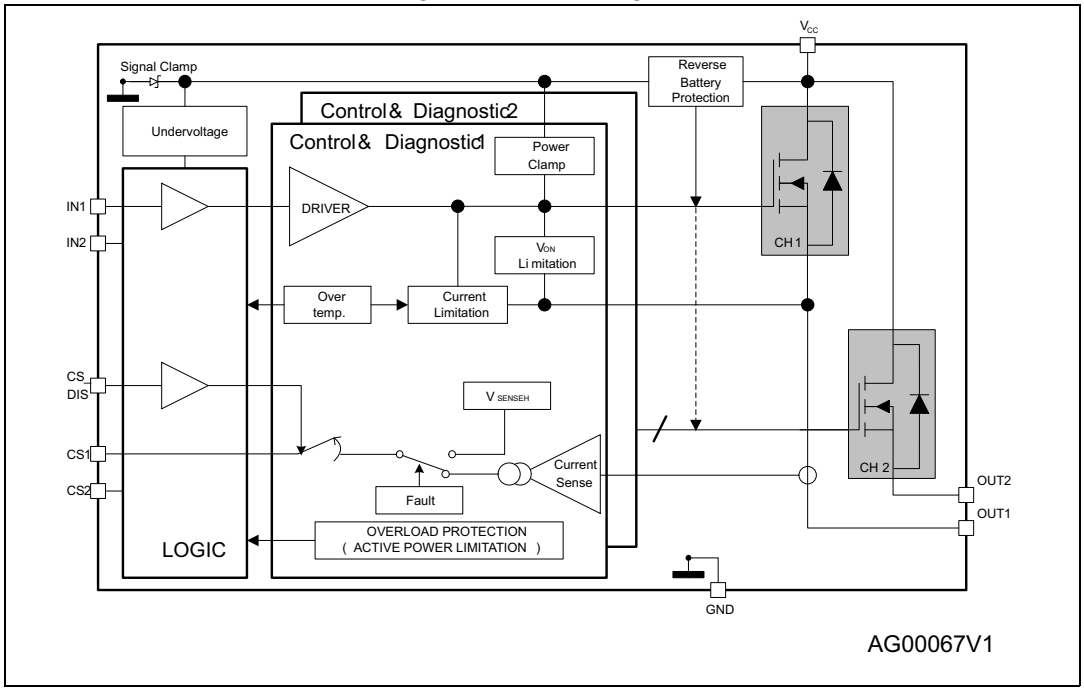


Table 1. Pin function

Name	Function
V_{CC}	Battery connection.
OUTn	Power output.
GND	Ground connection.
INn	Voltage controlled input pin with hysteresis, CMOS compatible. Controls output switch state.
CSn	Analog current sense pin, delivers a current proportional to the load current.
CS_DIS	Active high CMOS compatible pin, to disable the current sense pin.

Figure 2. Configuration diagram (top view)

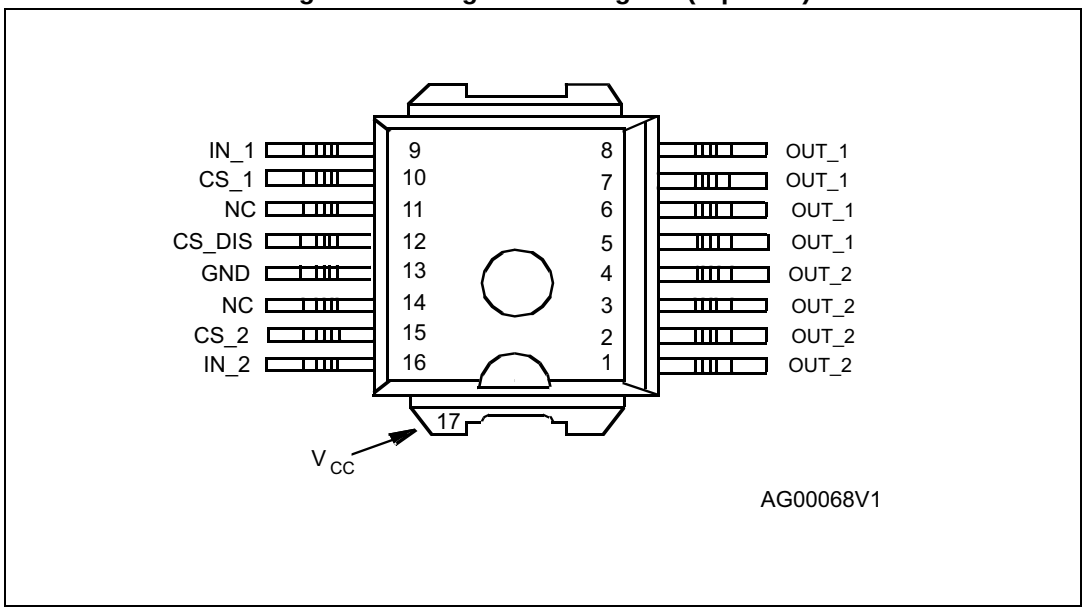
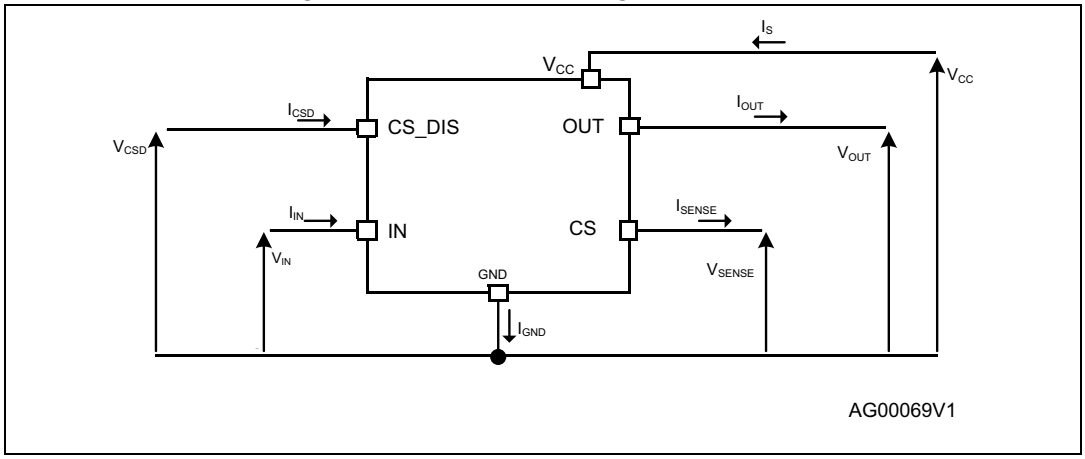


Table 2. Suggested connections for unused and not connected pins

Connection / pin	Current sense	N.C.	Output	Input	CS_DIS
Floating	Not allowed	X	X	X	X
To ground	Through 1 KΩ resistor	X	Not allowed	Through 10 KΩ resistor	Through 10 KΩ resistor

2 Electrical specifications

Figure 3. Current and voltage conventions



2.1 Absolute maximum ratings

Stressing the device above the ratings listed in the “Absolute maximum ratings” tables may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to the conditions in this section for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality documents.

Table 3. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CC}	DC supply voltage	28	V
V_{CCPK}	Transient supply voltage (T < 400 ms, R_{LOAD} > 0.5 Ω)	41	V
$-V_{CC}$	Reverse DC supply voltage	16	V
I_{OUT}	DC output current	Internally limited	A
$-I_{OUT}$	Reverse DC output current	60	A
I_{IN}	DC input current	-1 to 10	mA
I_{CSD}	DC current sense disable input current	-1 to 10	mA
V_{CSENSE}	Current sense maximum voltage	V_{CC}-41 +V_{CC}	V V
E_{MAX}	Maximum switching energy (single pulse) (L = 1.4 mH; R_L = 0 Ω; V_{bat} = 13.5 V; T_{jstart} = 150 °C; I_{OUT} = I_{limL}*(Typ.)*)	600	mJ

Table 3. Absolute maximum ratings (continued)

Symbol	Parameter	Value	Unit
V_{ESD}	Electrostatic discharge (Human Body Model: R = 1.5 KΩ; C = 100 pF) – Input – Current sense – CS_DIS – Output – V_{CC}	 4000 2000 4000 5000 5000	V
V_{ESD}	Charge device model (CDM-AEC-Q100-011)	750	V
T_j	Junction operating temperature	-40 to 150	°C
T_{stg}	Storage temperature	-55 to 150	°C

2.2 Thermal data

Table 4. Thermal data

Symbol	Parameter	Maximum value	Unit
$R_{thj\text{-}case}$	Thermal resistance junction-case (MAX) (with one channel ON)	0.4	°C/W
$R_{thj\text{-}amb}$	Thermal resistance junction-ambient	See *Figure 36*	°C/W

2.3 Electrical characteristics

8 V < V_{CC} < 28 V; -40 °C < T_j < 150 °C, unless otherwise specified.

Table 5. Power section

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{CC}	Operating supply voltage		4.5	13	28	V
V_{USD}	Undervoltage shutdown			3.5	4.5	V
$V_{USDhyst}$	Undervoltage shutdown hysteresis			0.5		V
R_{ON}	On-state resistance	I_{OUT} = 10 A; T_j = 25 °C		5		mΩ
		I_{OUT} = 10 A; T_j = 150 °C			10	mΩ
		I_{OUT} = 10 A; V_{CC} = 5 V; T_j = 25 °C			8	mΩ
$R_{ON\ REV}$	Reverse battery on-state resistance	V_{CC} = -13 V; I_{OUT} = -10 A; T_j = 25 °C			6	mΩ
V_{clamp}	Clamp voltage	I_S = 20 mA	41	46	52	V
I_S	Supply current	Off-state; V_{CC} = 13 V; T_j = 25 °C; V_{IN} = V_{OUT} = V_{SENSE} = V_{CSD} = 0 V		2 (1)	5(1)	µA
		On-state; V_{CC} = 13 V; V_{IN} = 5 V; I_{OUT} = 0 A		3.5	6.5	mA
$I_{L(off1)}$	Off-state output current (2)	V_{IN}=V_{OUT}=0V; V_{CC}=13V; T_j=25°C	0	0.01	3	µA
		V_{IN}=V_{OUT}=0V; V_{CC}=13V; T_j=125°C	0		5	µA

1. PowerMOS leakage included.
2. For each channel.

Table 6. Switching (V_{CC} = 13 V; T_j = 25 °C)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	R_L = 1.3 Ω (see *Figure 6*)	—	35	—	µs
$t_{d(off)}$	Turn-off delay time	R_L = 1.3 Ω (see *Figure 6*)	—	20	—	µs
$(dV_{OUT}/dt)_{on}$	Turn-on voltage slope	R_L = 1.3 Ω	—	See *Figure 27*	—	V/µs
$(dV_{OUT}/dt)_{off}$	Turn-off voltage slope	R_L = 1.3 Ω	—	See *Figure 28*	—	V/µs
W_{ON}	Switching energy losses during t_{won}	R_L = 1.3 Ω (see *Figure 6*)	—	2.5	—	mJ
W_{OFF}	Switching energy losses during t_{woff}	R_L = 1.3 Ω (see *Figure 6*)	—	1.2	—	mJ

Table 7. Logic inputs

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{IL}	Input low level voltage				0.9	V
I_{IL}	Low level input current	V_{IN} = 0.9 V	1			µA
V_{IH}	Input high level voltage		2.1			V
I_{IH}	High level input current	V_{IN} = 2.1 V			10	µA
$V_{I(hyst)}$	Input hysteresis voltage		0.25			V
V_{ICL}	Input clamp voltage	I_{IN} = 1 mA	5.5		7	V
		I_{IN} = -1 mA		-0.7		V
V_{CSDL}	CS_DIS low level voltage				0.9	V
I_{CSDL}	Low level CS_DIS current	V_{CSD} = 0.9 V	1			µA
V_{CSDH}	CS_DIS high level voltage		2.1			V
I_{CSDH}	High level CS_DIS current	V_{CSD} = 2.1 V			10	µA
$V_{CSD(hyst)}$	CS_DIS hysteresis voltage		0.25			V
V_{CSCL}	CS_DIS clamp voltage	I_{CSD} = 1 mA	5.5		7	V
		I_{CSD} = -1 mA		-0.7		V

Table 8. Protections and diagnostics(1)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{limH}	DC short circuit current	V_{CC} = 13 V	70	100	140	A
		5 V < V_{CC} < 24 V			140	A
I_{limL}	Short circuit current during thermal cycling	V_{CC} = 13 V; T_R < T_j < T_{TSD}		25		A
T_{TSD}	Shutdown temperature		150	175	200	°C
T_R	Reset temperature		T_{RS} + 1	T_{RS} + 5		°C
T_{RS}	Thermal reset of status		135			°C
T_{HYST}	Thermal hysteresis (T_{TSD}-T_R)			7		°C
V_{DEMAG}	Turn-off output voltage clamp	I_{OUT} = 2 A; V_{IN} = 0; L = 6 mH	V_{CC}-28	V_{CC}-31	V_{CC}-35	V
V_{ON}	Output voltage drop limitation	I_{OUT} =1 A; T_j = -40 °C...150 °C (see *Figure 8*)		25		mV

1. To ensure long term reliability under heavy overload or short circuit conditions, protection and related diagnostic signals must be used together with a proper software strategy. If the device is subjected to abnormal conditions, this software must limit the duration and number of activation cycles.

Table 9. Current sense (8 V < V_{CC} < 18 V)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
K_0	I_{OUT}/I_{SENSE}	I_{OUT} = 5 A; V_{SENSE} = 0.5 V T_j = -40 °C...150 °C	8300	12640	17600	
K_1	I_{OUT}/I_{SENSE}	I_{OUT} = 10 A; V_{SENSE} = 0.5 V T_j = -40 °C...150 °C T_j = 25 °C...150 °C	9200 9602	13220 13220	17300 16703	
dK_1/K_1 (1)	Current sense ratio drift	I_{OUT} = 10 A; V_{SENSE} = 0.5 V; V_{CSD} = 0 V; T_j = -40 °C...150 °C	-13		13	%
K_2	I_{OUT}/I_{SENSE}	I_{OUT} = 15 A; V_{SENSE} = 4 V T_j = -40 °C...150 °C T_j = 25 °C...150 °C	9500 10408	13120 13120	16900 15907	
dK_2/K_2 (1)	Current sense ratio drift	I_{OUT} = 15 A; V_{SENSE} = 4 V; V_{CSD} = 0 V; T_j = -40 °C...150 °C	-10		10	%
K_3	I_{OUT}/I_{SENSE}	I_{OUT} = 25 A; V_{SENSE} = 4 V T_j = -40 °C...150 °C T_j = 25 °C...150 °C	10600 11278	12920 12920	15600 14644	
dK_3/K_3 (1)	Current sense ratio drift	I_{OUT} = 25 A; V_{SENSE} = 4 V; V_{CSD} = 0 V; T_j = -40 °C...150 °C	-7		7	%
I_{SENSE0}	Analog sense leakage current	I_{OUT} = 0 A; V_{SENSE} = 0 V; V_{CSD} = 5 V; V_{IN} = 0 V; T_j = -40 °C...150 °C	0		1	µA
		V_{CSD} = 0 V; V_{IN} = 5 V; T_j = -40 °C...150 °C	0		2	µA
		I_{OUT} = 10 A; V_{SENSE} = 0 V; V_{CSD} = V_{IN} = 5 V	0		1	µA
V_{SENSE}	Max analog sense output voltage	I_{OUT} = 25 A; V_{CSD} = 0 V	5			V
V_{SENSEH} (2)	Analog sense output voltage in fault conditions	V_{CC} = 13 V; R_{SENSE} = 10 KΩ		8		V
I_{SENSEH} (2)	Analog sense output current in fault conditions	V_{CC} = 13 V; V_{SENSE} = 5 V		7		mA
$t_{DSENSE1H}$	Delay response time from falling edge of CS_DIS pin	V_{SENSE} < 4 V, 5 A < I_{out} < 25 A I_{SENSE} = 90 % of $I_{SENSE\ max}$ (see *Figure 4*)		50	100	µs
$t_{DSENSE1L}$	Delay response time from rising edge of CS_DIS pin	V_{SENSE} < 4 V, 5 A < I_{out} < 25 A I_{SENSE} = 10 % of $I_{SENSE\ max}$ (see *Figure 4*)		5	20	µs

Table 9. Current sense (8 V < V_{CC} < 18 V) (continued)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{DSENSE2H}$	Delay response time from rising edge of INPUT pin	V_{SENSE} < 4 V, 5 A < I_{out} < 25 A I_{SENSE} = 90 % of $I_{SENSE\ max}$ (see *Figure 4*)		110	600	µs
$\Delta t_{DSENSE2H}$	Delay response time between rising edge of output current and rising edge of current sense	V_{SENSE} < 4V, I_{SENSE} = 90 % of $I_{SENSEMAX}$, I_{OUT} = 90 % of I_{OUTMAX} I_{OUTMAX} =10 (see *Figure 7*)			300	µs
$t_{DSENSE2L}$	Delay response time from falling edge of INPUT pin	V_{SENSE} < 4 V, 5 A < I_{out} < 25 A I_{SENSE} = 10 % of $I_{SENSE\ max}$ (see *Figure 4*)		100	250	µs

1. Parameter guaranteed by design; it is not tested.
2. Fault conditions includes: power limitation, overtemperature and open-load off-state detection.

Table 10. Open-load detection (8 V < V_{CC} < 18 V)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{OL}	Open-load off-state voltage detection threshold	V_{IN} = 0 V, 8 V < V_{CC} < 18 V	2	—	4	V
I_{OL}	Open-load on-state current detection threshold	V_{IN} = 5 V, 8 V < V_{CC} < 18 V I_{SENSE} = 5 µA	10	—	100	mA
t_{DSTKON}	Output short circuit to V_{CC} detection delay at turn off	See *Figure 5*	180	—	1200	µs
$I_{L(off2)}$	Off-state output current at V_{OUT} = 4 V	V_{IN} = 0 V; V_{SENSE} = 0 V V_{OUT} rising from 0 V to 4 V	-120	—	0	µA
td_vol	Delay response from output rising edge to V_{SENSE} rising edge in open-load	V_{IN} = 0 V; V_{OUT} = 4 V V_{SENSE} = 90 % of V_{SENSEH}		—	20	µs

Figure 4. Current sense delay characteristics

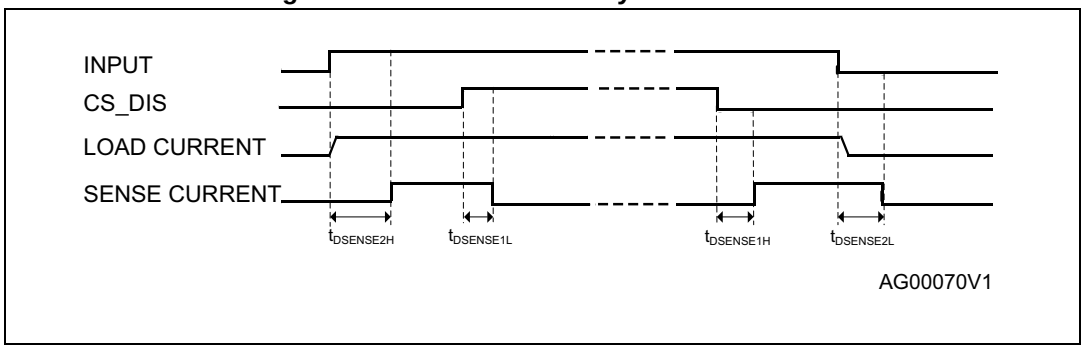


Figure 5. Open-load off-state delay timing

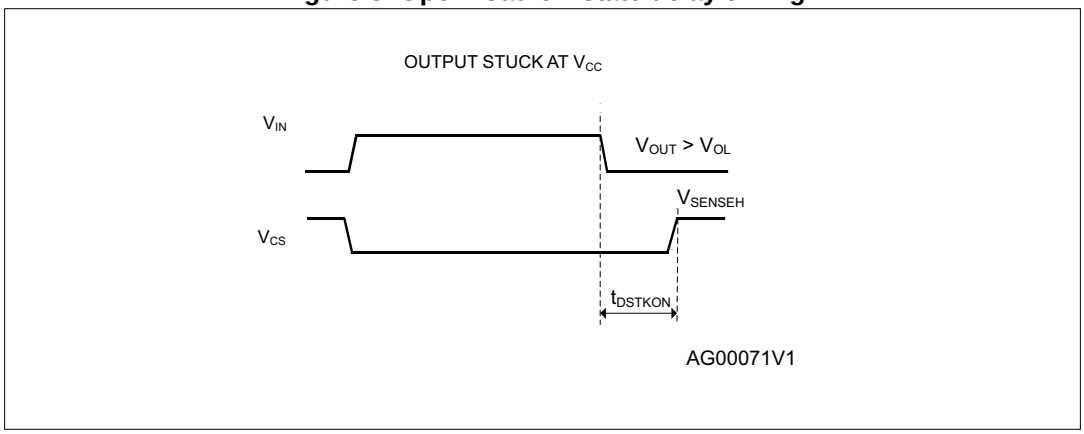


Figure 6. Switching characteristics

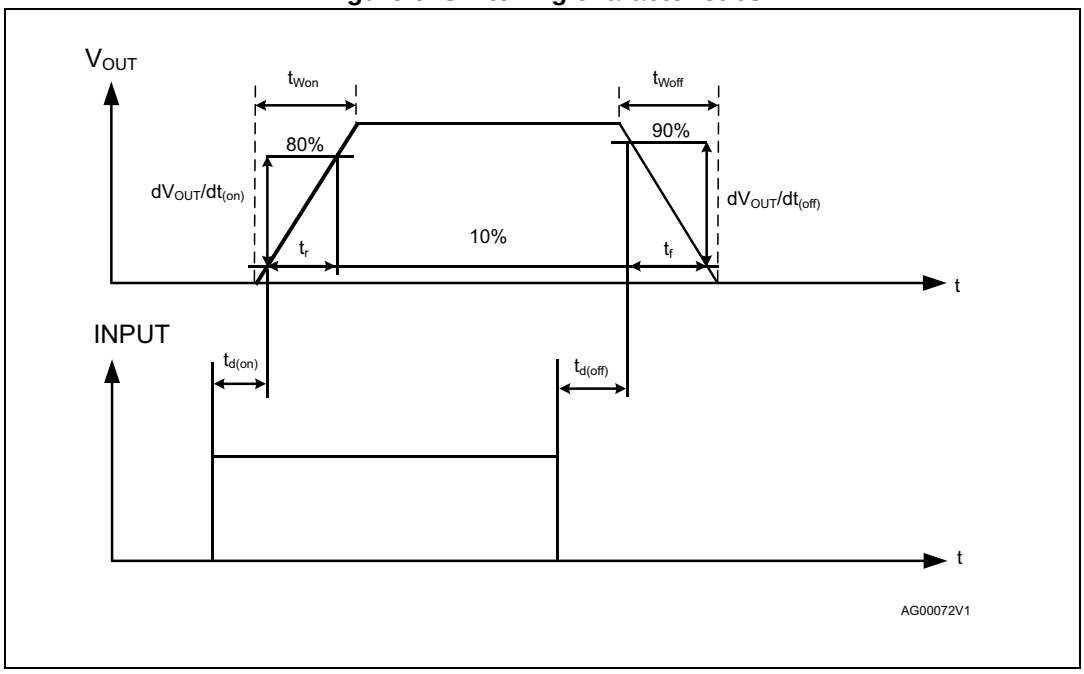


Figure 7. Delay response time between rising edge of output current and rising edge of current sense (CS enabled)

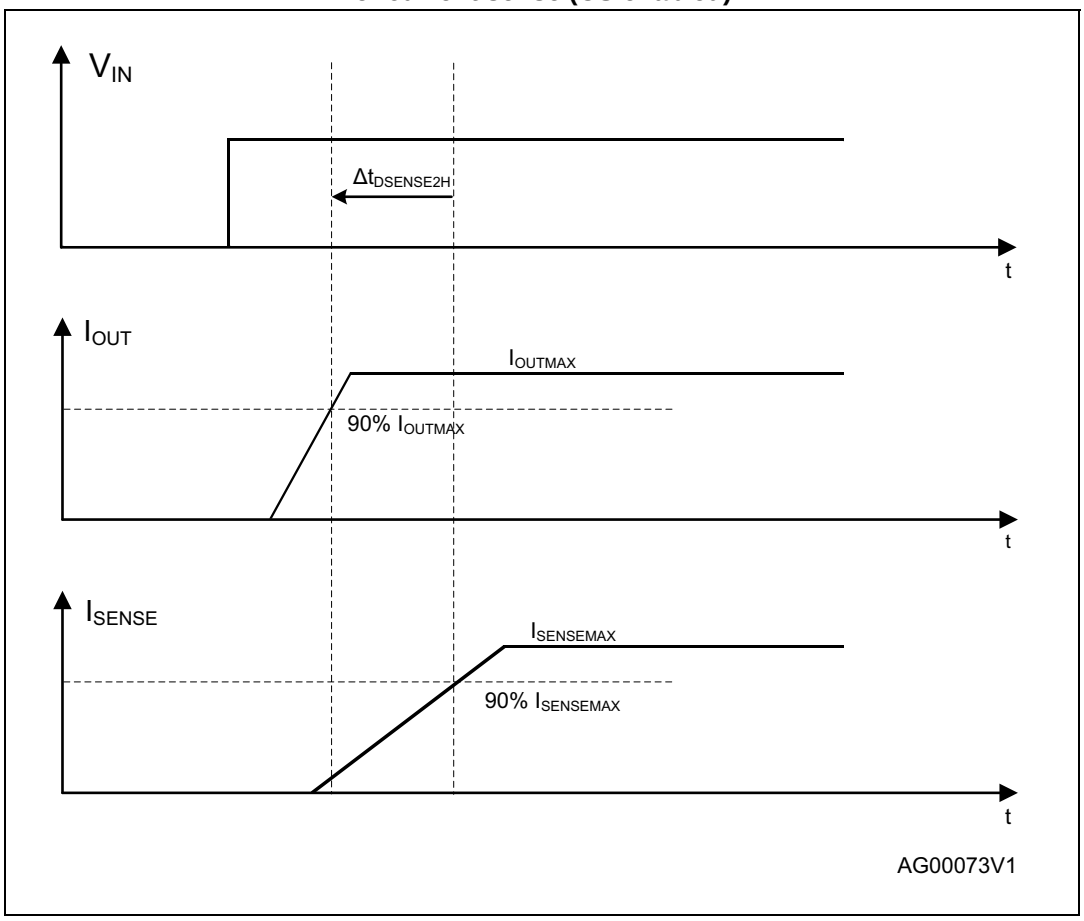


Figure 8. Output voltage drop limitation

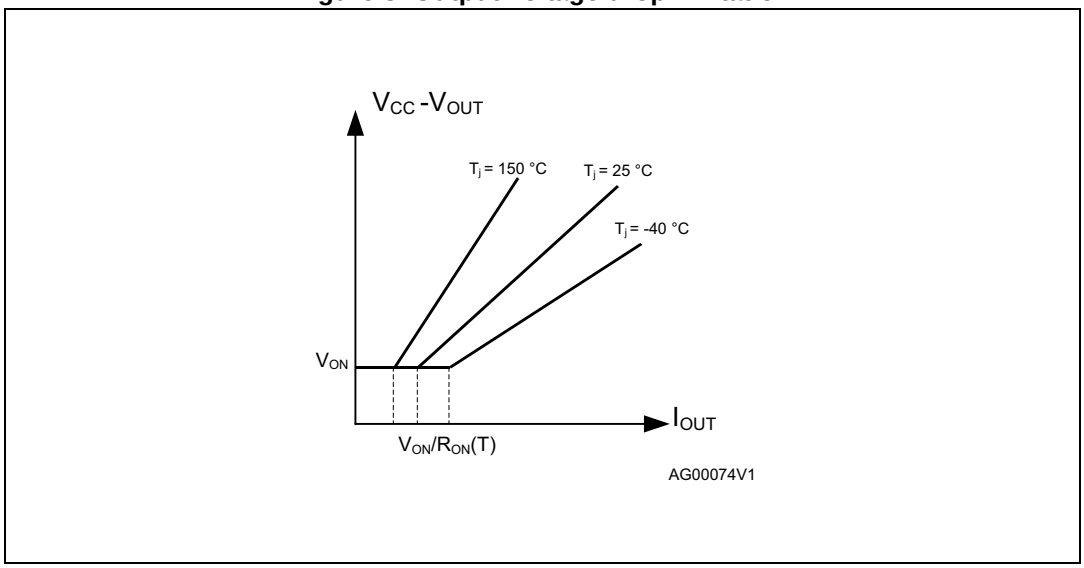
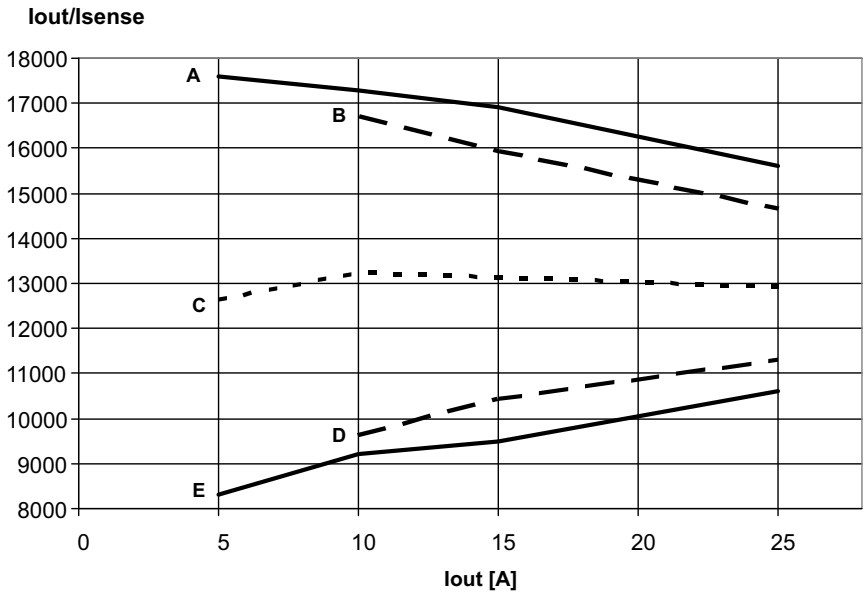


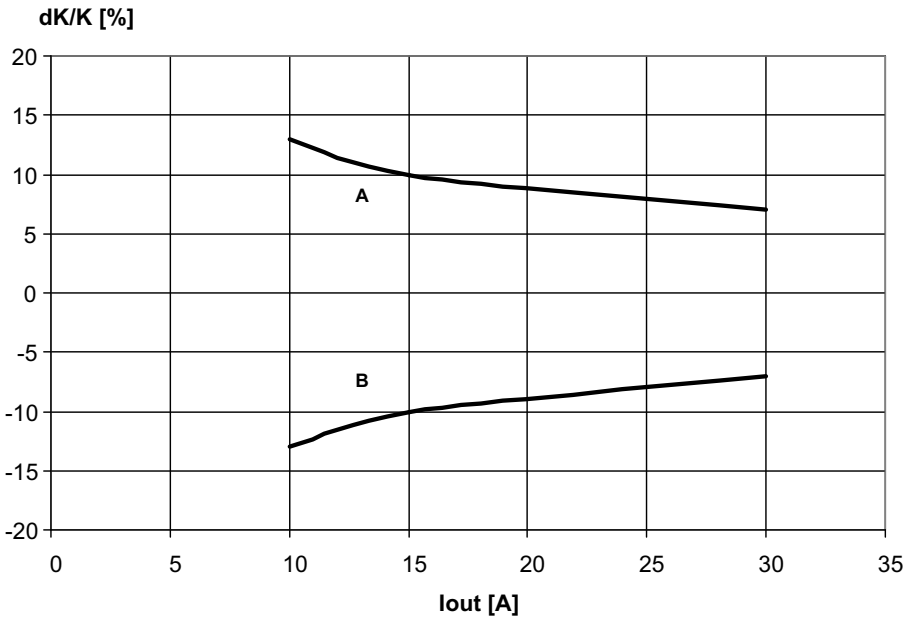
Figure 9. I_{OUT}/I_{SENSE} vs I_{OUT}



A: Max, Tj = -40 °C to 150 °C
B: Max, Tj = 25 °C to 150 °C
C: Typical, Tj = -40 °C to 150 °C
D: Min, Tj = 25 °C to 150 °C
E: Min, Tj = -40 °C to 150 °C

AG00075V1

Figure 10. Maximum current sense ratio drift vs load current(1)



A: Max, Tj = -40 °C to 150 °C
B: Min, Tj = -40 °C to 150 °C

AG00076V1

1. Parameter guaranteed by design; it is not tested.

Table 11. Truth table

Conditions	Input	Output	Sense (V_{CSD} = 0 V)(1)
Normal operation	L H	L H	0 Nominal
Overtemperature	L H	L L	0 V_{SENSEH}
Undervoltage	L H	L L	0 0
Overload	H H	X (no power limitation) Cycling (power limitation)	Nominal V_{SENSEH}
Short circuit to GND (Power limitation)	L H	L L	0 V_{SENSEH}
Open-load off-state (with external pull up)	L	H	V_{SENSEH}
Short circuit to V_{CC} (external pull up disconnected)	L H	H H	V_{SENSEH} < Nominal
Negative output voltage clamp	L	L	0

1. If the V_{CSD} is high, the SENSE output is at a high impedance, its potential depends on leakage currents and external circuit.

Table 12. Electrical transient requirements (part 1/3)

ISO 7637-2: 2004(E) Test Pulse	Test levels(1)		Number of pulses or test times	Burst cycle/pulse repetition time		Delays and impedance
	III	IV				
1	-75 V	-100 V	5000 pulses	0.5 s	5 s	2 ms, 10 Ω
2a	+37 V	+50 V	5000 pulses	0.2 s	5 s	50 µs, 2 Ω
3a	-100 V	-150 V	1h	90 ms	100 ms	0.1 µs, 50 Ω
3b	+75 V	+100 V	1h	90 ms	100 ms	0.1 µs, 50 Ω
4	-6 V	-7 V	1 pulse			100 ms, 0.01 Ω
5b(2)	+65 V	+87 V	1 pulse			400 ms, 2 Ω

1. The above test levels must be considered referred to V_{CC} = 13.5 V except for pulse 5b.
2. Valid in case of external load dump clamp: 40V maximum referred to ground. The protection strategy allows PowerMOS to be cyclically switched on during load dump, so distributing the load dump energy along the time and to transfer a part of it to the load.

Table 13. Electrical transient requirements (part 2/3)

ISO 7637-2: 2004(E) Test Pulse	Test level results(1)	
	III	IV
1	C	C
2a	C	C
3a	C	C
3b	C	C
4	C	C
5b(2)(3)	C	C

1. The above test levels must be considered referred to V_{CC} = 13.5 V except for pulse 5b.
2. Valid in case of external load dump clamp: 40V maximum referred to ground. The protection strategy allows PowerMOS to be cyclically switched on during load dump, so distributing the load dump energy along the time and to transfer a part of it to the load.
3. Suppressed load dump (pulse 5b) is withstood with a minimum load connected as specified in *Table 3: Absolute maximum ratings*.

Table 14. Electrical transient requirements (part 3/3)

Class	Contents
C	All functions of the device are performed as designed after exposure to disturbance.
E	One or more functions of the device are not performed as designed after exposure to disturbance and cannot be returned to proper operation without replacing the

2.4 Waveforms

Figure 11. Normal operation

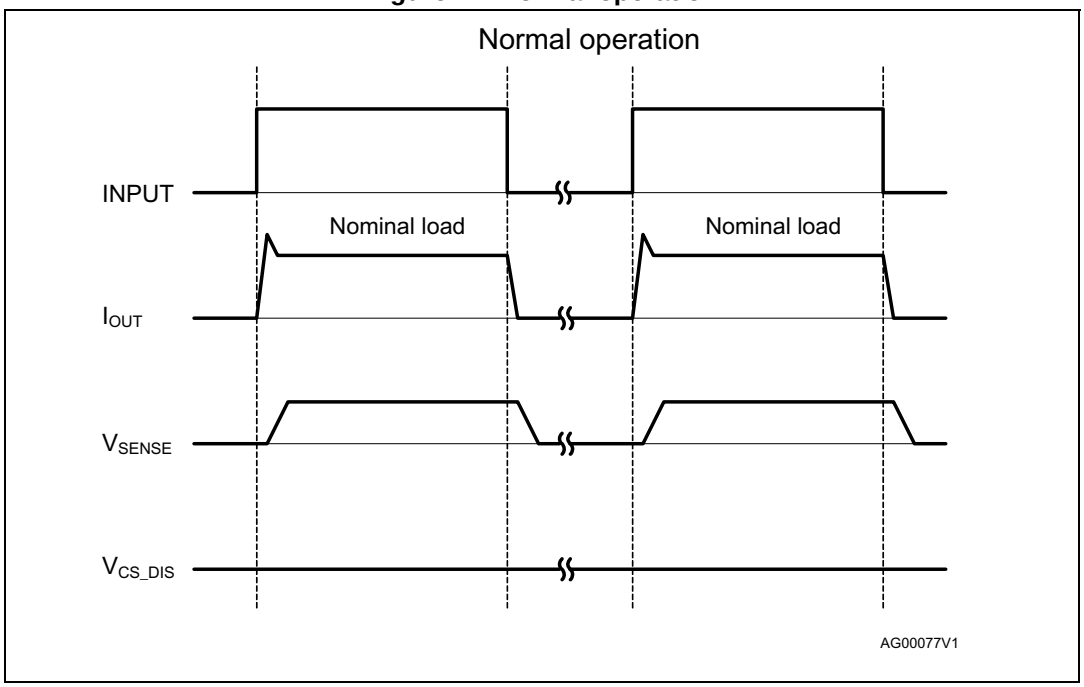


Figure 12. Overload or short to GND

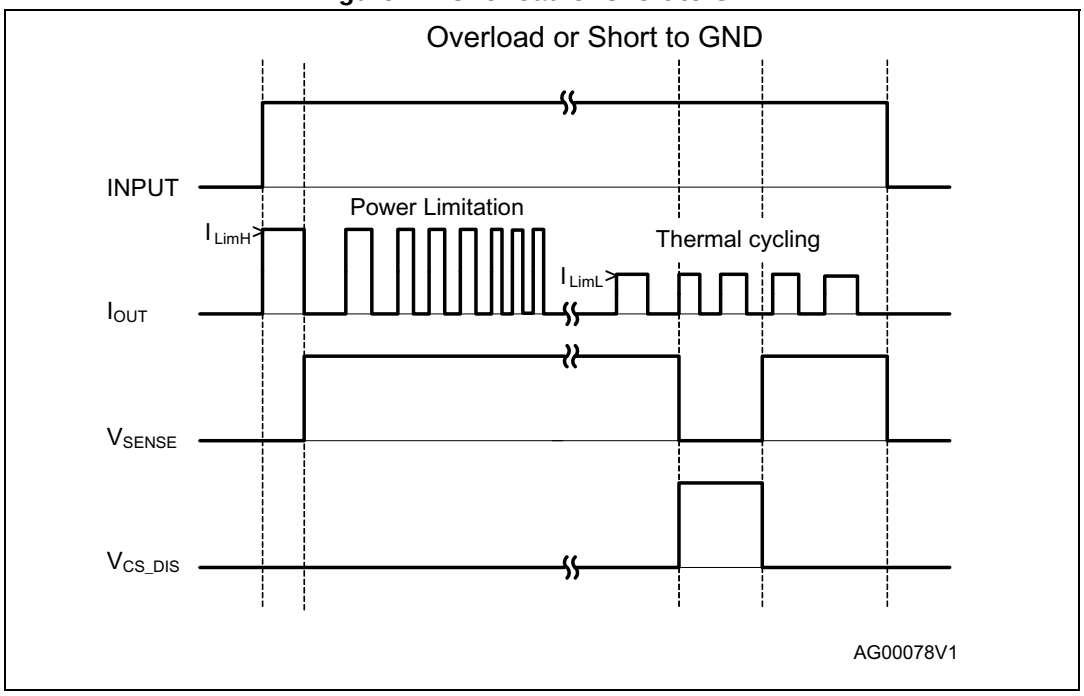


Figure 13. Intermittent overload

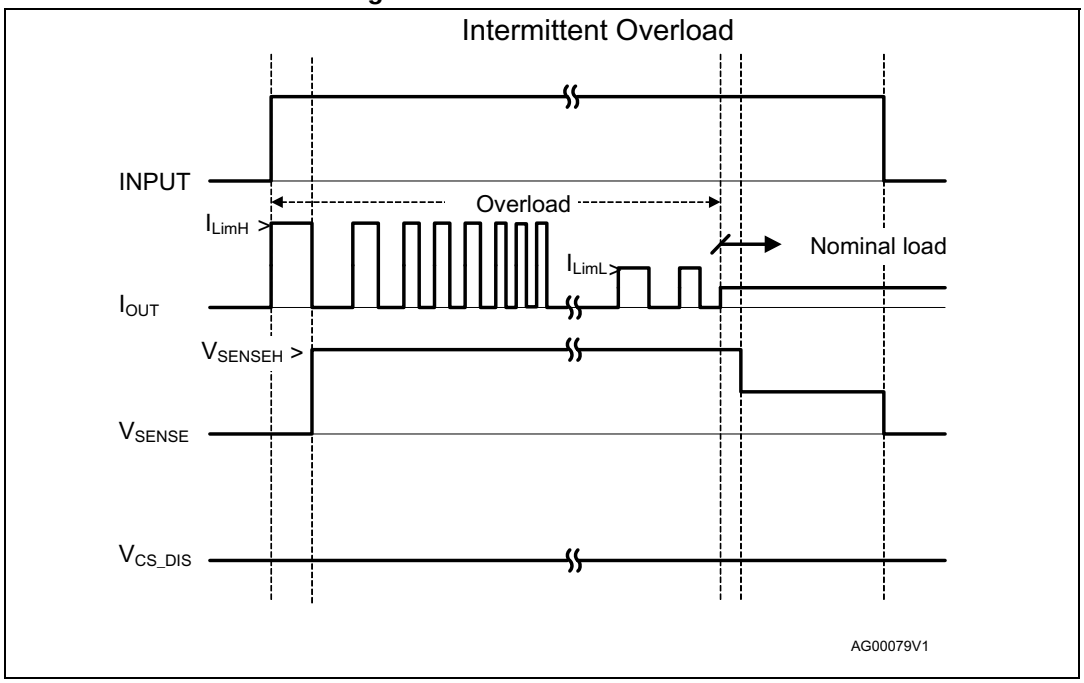


Figure 14. Off-state open-load with external circuitry

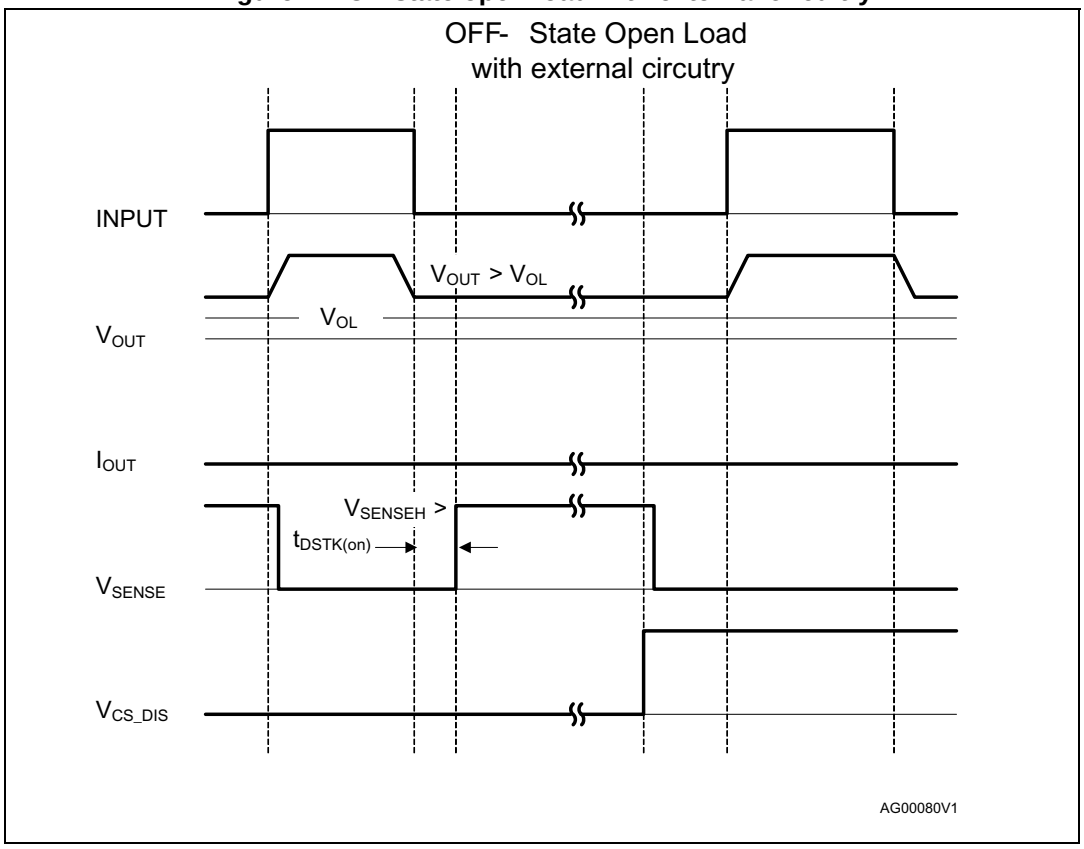


Figure 15. Short to V_{CC}

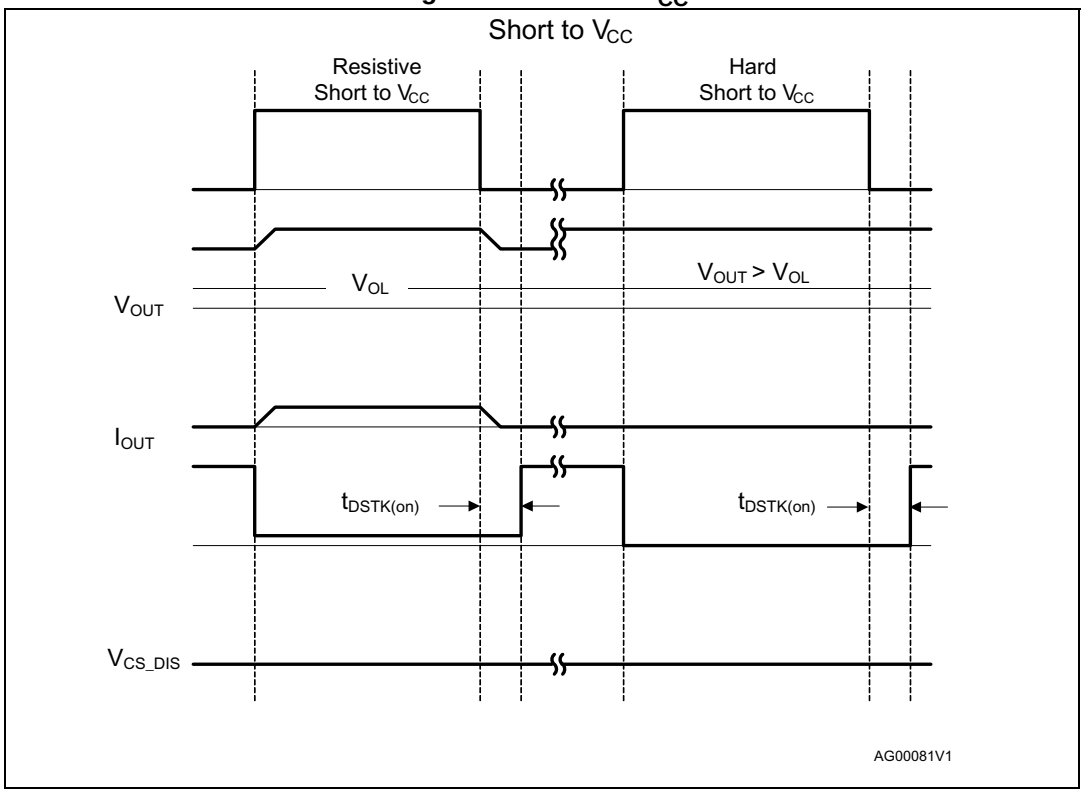
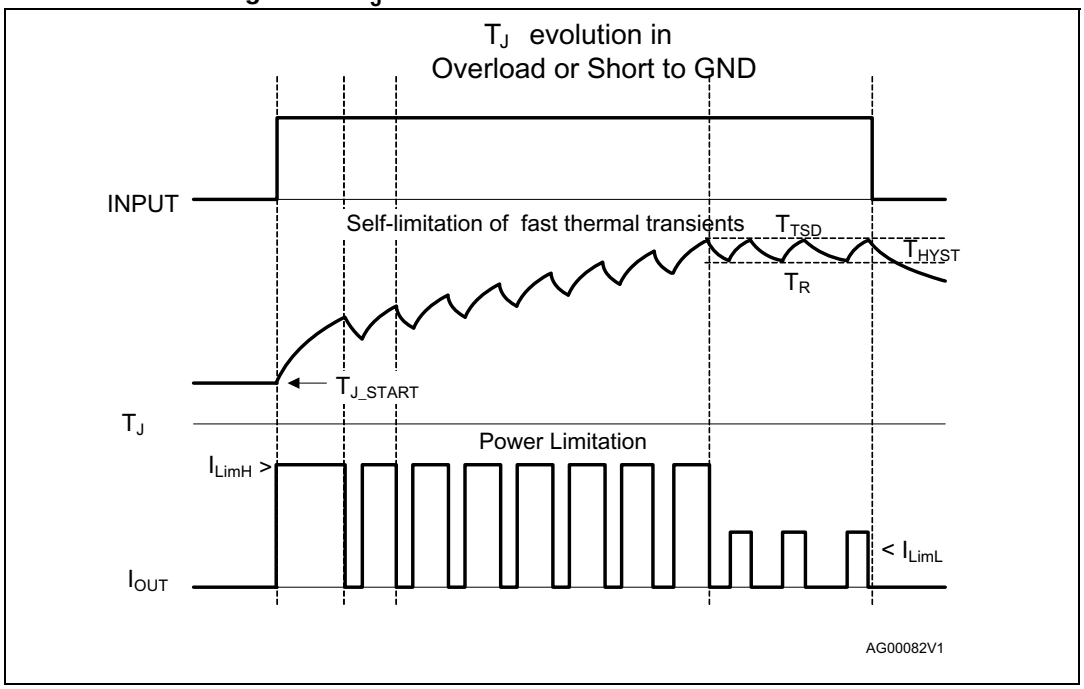


Figure 16. T_J evolution in overload or short to GND



2.5 Electrical characteristics curves

Figure 17. Off-state output current

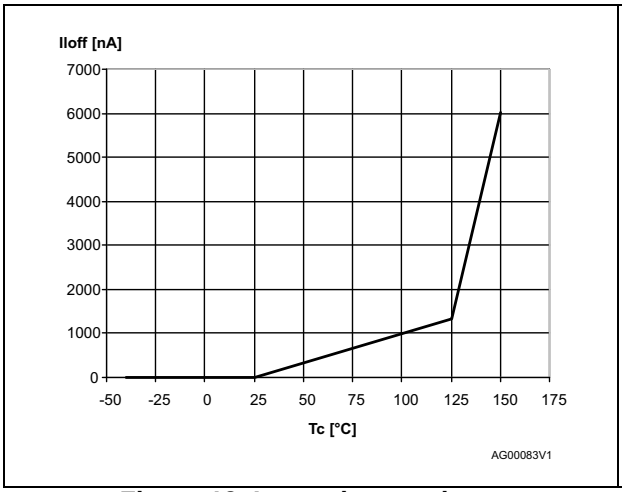


Figure 18. High level input current

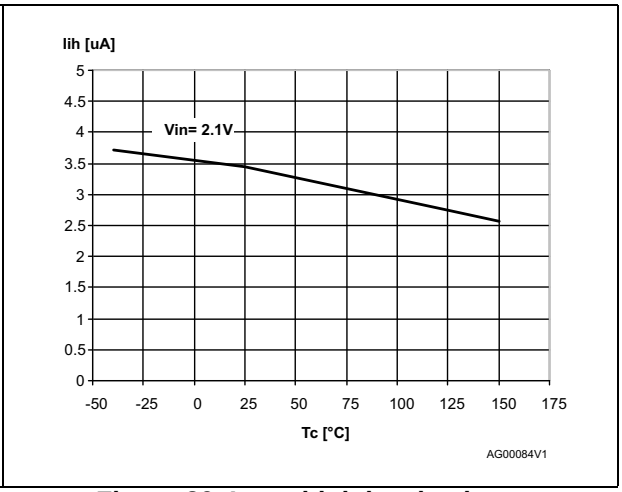


Figure 19. Input clamp voltage

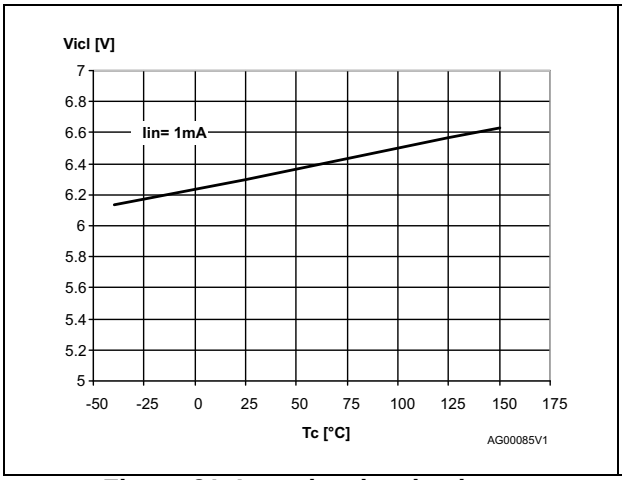


Figure 20. Input high level voltage

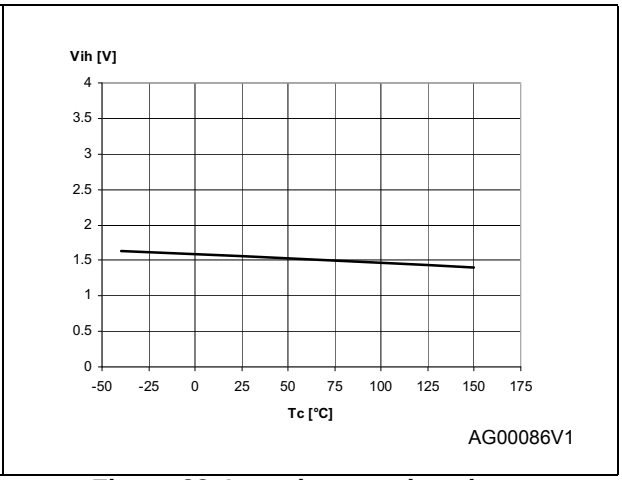


Figure 21. Input low level voltage

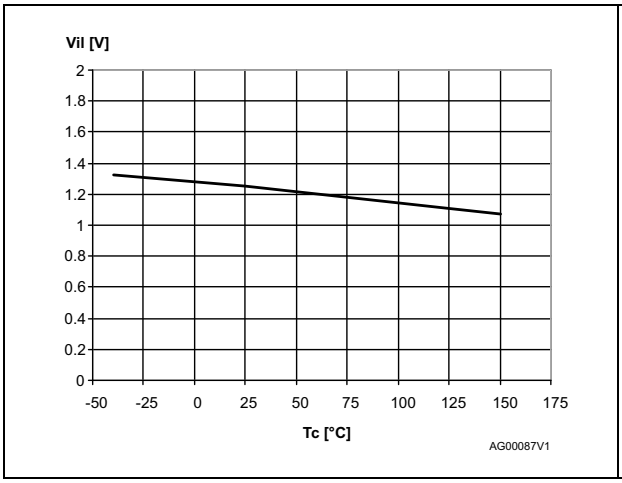


Figure 22. Input hysteresis voltage

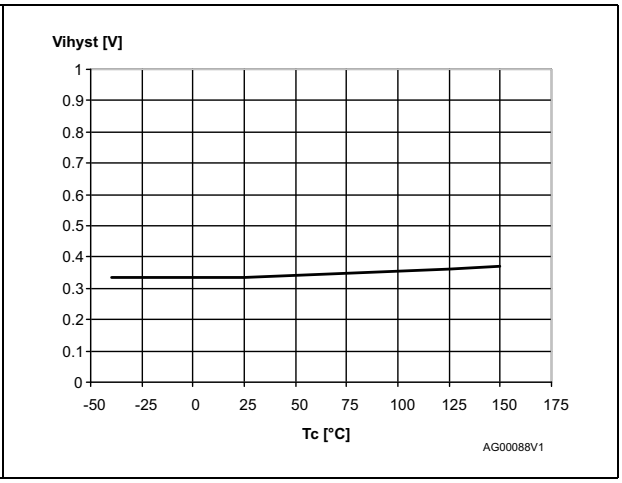


Figure 23. On-state resistance vs T_{case}

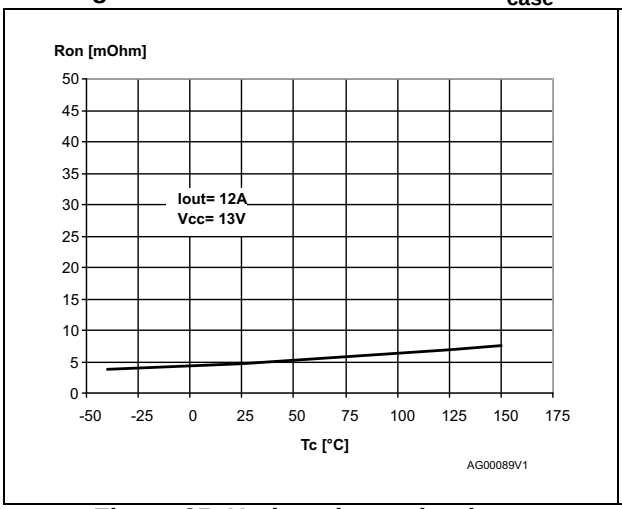


Figure 24. On-state resistance vs V_{CC}

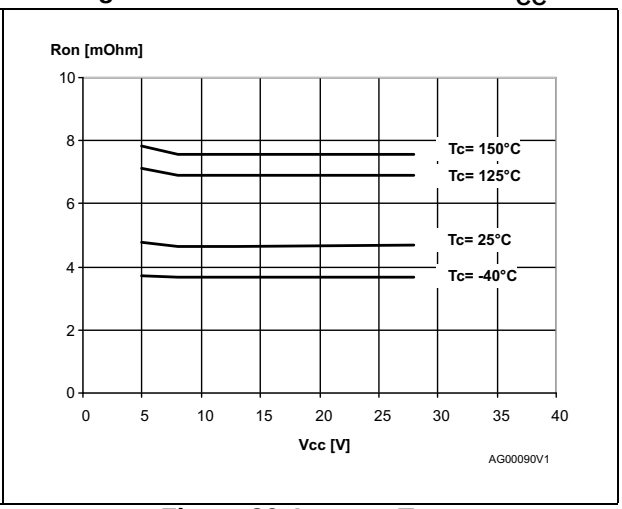


Figure 25. Undervoltage shutdown

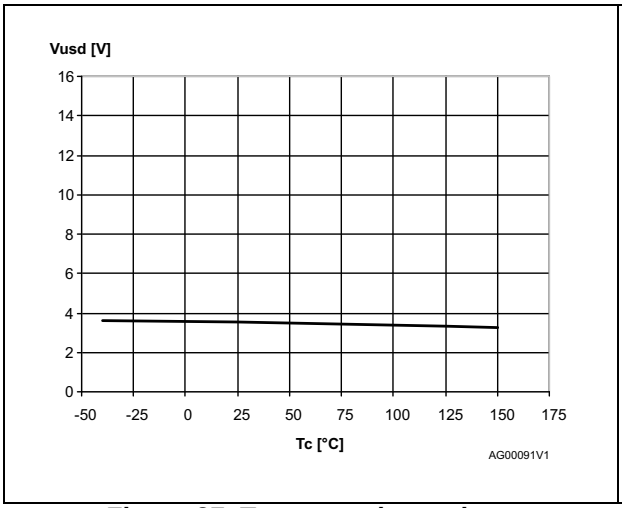


Figure 26. I_{LIMH} vs T_{case}

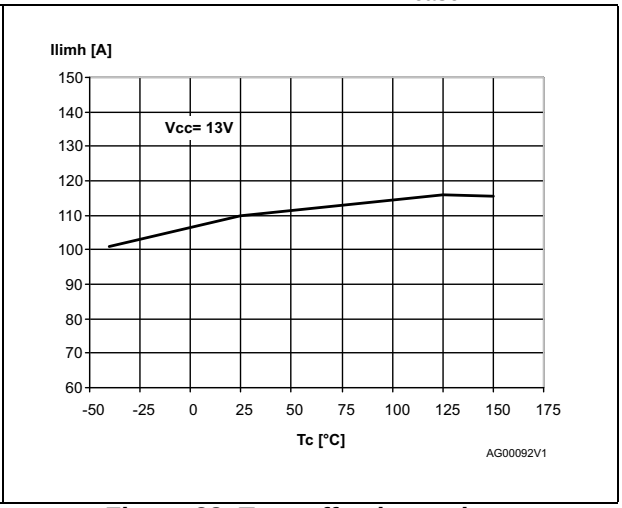


Figure 27. Turn-on voltage slope

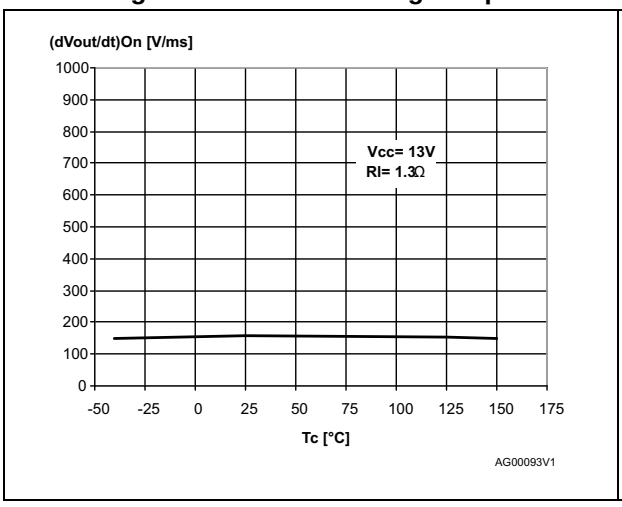


Figure 28. Turn-off voltage slope

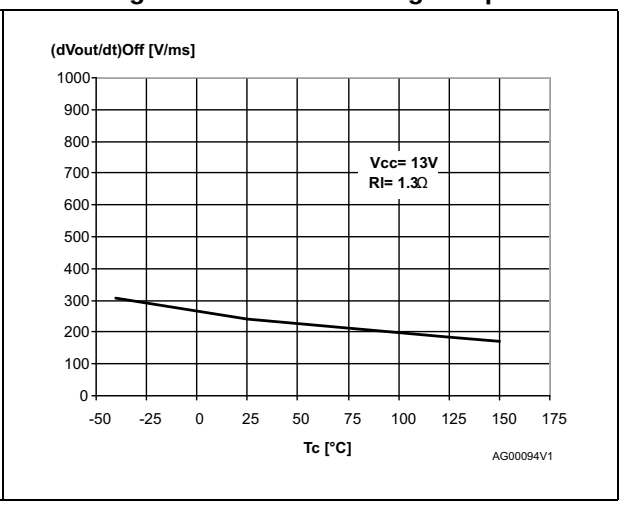


Figure 29. CS_DIS clamp voltage

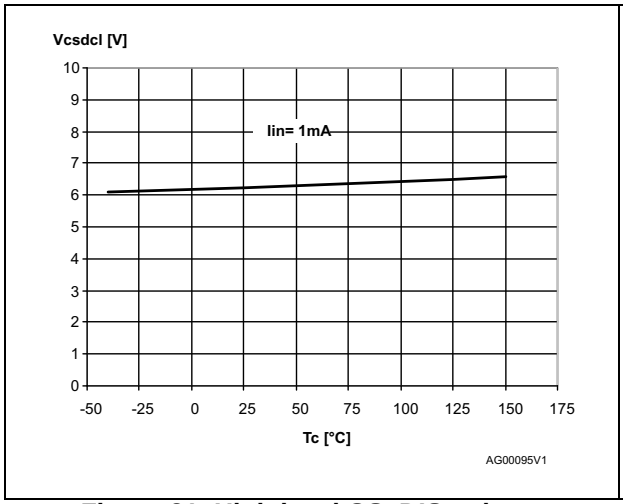


Figure 30. Low level CS_DIS voltage

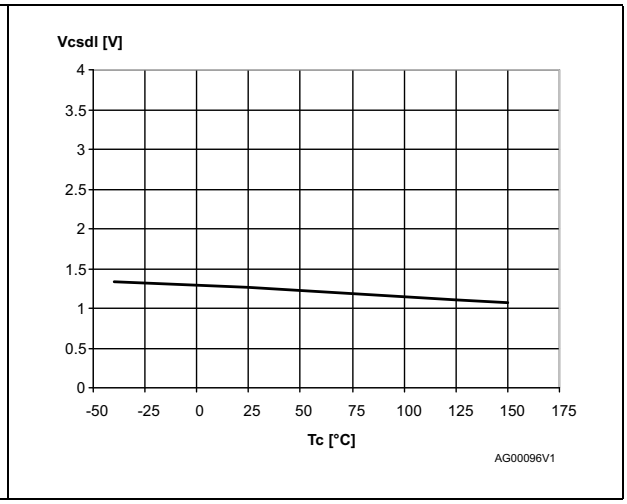
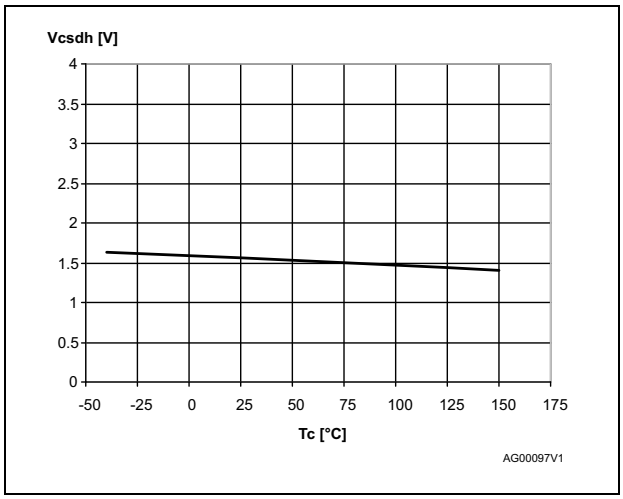
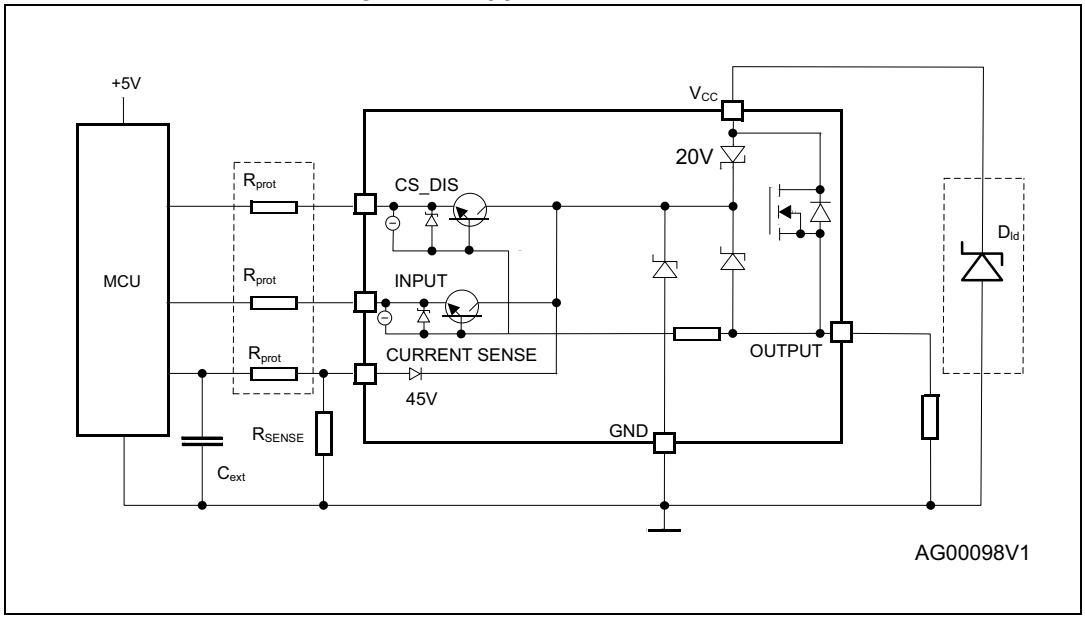


Figure 31. High level CS_DIS voltage



3 Application information

Figure 32. Application schematic



Note: Channel 2 has the same internal circuit as channel 1.

3.1 Load dump protection

D_{ld} is necessary (voltage transient suppressor) if the load dump peak voltage exceeds the V_{CC} max DC rating. The same applies if the device is subject to transients on the V_{CC} line that are greater than the ones shown in the ISO 7637-2 2004 (E) table.

3.2 MCU I/Os protection

When negative transients are present on the V_{CC} line, the control pins are pulled negative to approximately -1.5 V. ST suggests to insert a resistor (R_{prot}) in line to prevent the microcontroller I/O pins from latching-up.

The value of these resistors is a compromise between the leakage current of microcontroller and the current required by the HSD I/Os (Input levels compatibility) with the latch-up limit of microcontroller I/Os.

Equation 1

$$-V_{CCpeak}/I_{latchup} \leq R_{prot} \leq (V_{OH\mu C} - V_{IH}) / I_{IHmax}$$

Calculation example:

For V_{CCpeak} = -1.5 V and $I_{latchup} \geq$ 20 mA; $V_{OH\mu C} \geq$ 4.5 V

75 Ω ≤ R_{prot} ≤ 240 kΩ.

Recommended values: R_{prot} = 10 kΩ, C_{EXT} = 10 nF.

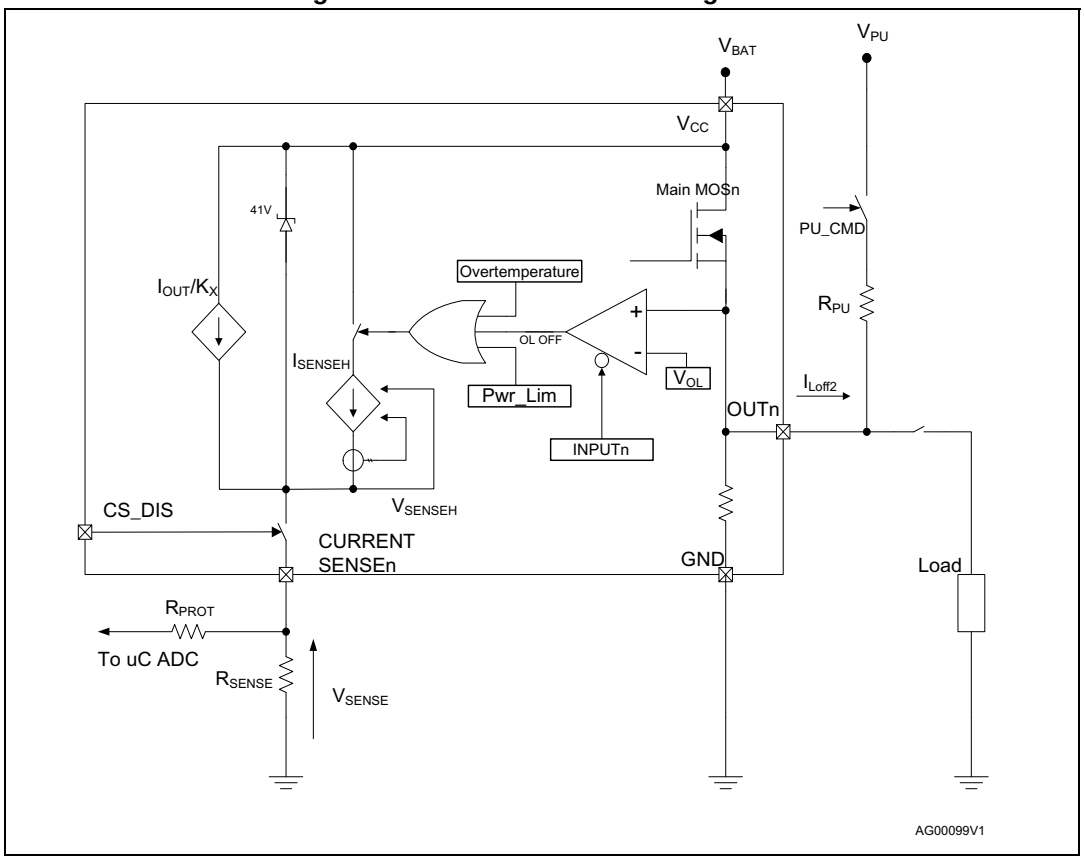
3.3 Current sense and diagnostic

The current sense pin performs a double function (see *Figure 33: Current sense and diagnostic*):

- **Current mirror of the load current in normal operation,** delivering a current proportional to the load one according to a known ratio $\mathbf{K_X}$.
  The current I_{SENSE} can be easily converted to a voltage V_{SENSE} by means of an external resistor R_{SENSE}. Linearity between I_{OUT} and V_{SENSE} is ensured up to 5V minimum (see parameter V_{SENSE} in *Table 9: Current sense (8 V < VCC < 18 V)*). The current sense accuracy depends on the output current (refer to current sense electrical characteristics *Table 9: Current sense (8 V < VCC < 18 V)*).
- **Diagnostic flag in fault conditions**, delivering a fixed voltage V_{SENSEH} up to a maximum current I_{SENSEH} in case of the following fault conditions (refer to *Truth table*):
  - Power limitation activation
  - Overtemperature
  - Short to V_{CC} in off-state
  - Open-load in off-state with additional external components.

A logic level high on CS_DIS pin sets at the same time all the current sense pins of the device in a high impedance state, thus disabling the current monitoring and diagnostic detection. This feature allows multiplexing of the microcontroller analog inputs by sharing of sense resistance and ADC line among different devices.

Figure 33. Current sense and diagnostic



3.3.1 Short to V_{CC} and off-state open-load detection

Short to V_{CC}

A short circuit between V_{CC} and output is indicated by the relevant current sense pin set to V_{SENSEH} during the device off-state. Small or no current is delivered by the current sense during the on-state depending on the nature of the short circuit.

Off-state open-load with external circuitry

Detection of an open-load in off mode requires an external pull-up resistor R_{PU} connecting the output to a positive supply voltage V_{PU}.

It is preferable V_{PU} to be switched off during the module standby mode in order to avoid the overall standby current consumption to increase in normal conditions, i.e. when load is connected.

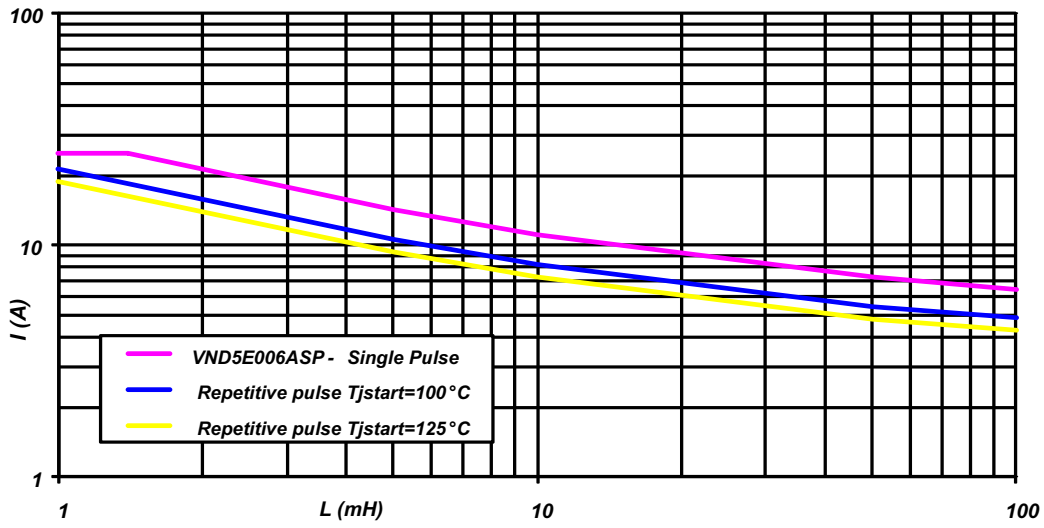
For proper open-load detection in off-state, the external pull-up resistor must be selected according to the following formula:

$$V_{OUT}\big|_{Pull-up\_ON} = \frac{R_{PD} \cdot V_{PU} - R_{PU} \cdot R_{PD} \cdot I_{L(off\,2)}}{R_{PU} + R_{PD}} > V_{OL\,\max} = 4V$$

For the values of V_{OLmin},V_{OLmax}, and $I_{L(off2)}$ see *Table 10: Open-load detection (8 V < VCC < 18 V)*.

3.4 Maximum demagnetization energy (V_{CC} = 13.5 V)

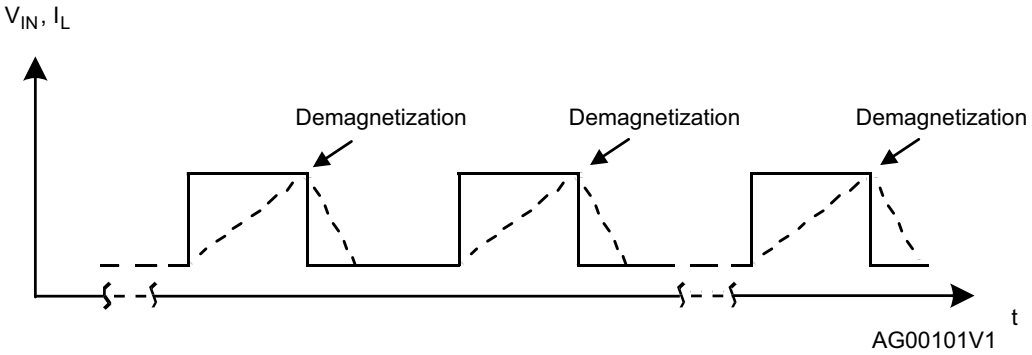
Figure 34. Maximum turn-off current versus inductance



A: T_{jstart} = 150°C single pulse

B: T_{jstart} = 100°C repetitive pulse

C: T_{jstart} = 125°C repetitive pulse

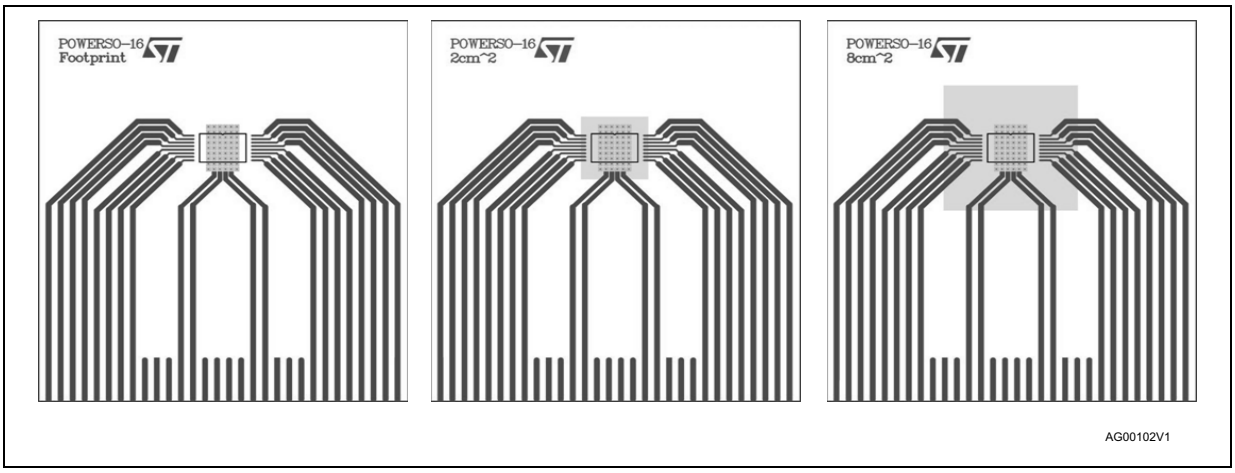


Note: Values are generated with R_L = 0 Ω
In case of repetitive pulses, Tjstart (at beginning of each demagnetization) of every pulse must not exceed the temperature specified above for curves A and B.

4 Package and PCB thermal data

4.1 PowerSO-16 thermal data

Figure 35. PowerSO-16 PC board(1)



1. Layout condition of R_{th} and Z_{th} measurements (PCB: Double layer, Thermal Vias, FR4 area= 77mm x 86mm, PCB thickness=1.6mm, Cu thickness=70µm (front and back side), Copper areas: from minimum pad lay-out to 8cm^2).

Figure 36. $R_{thj\text{-}amb}$ vs PCB copper area in open box free air condition (one channel ON)

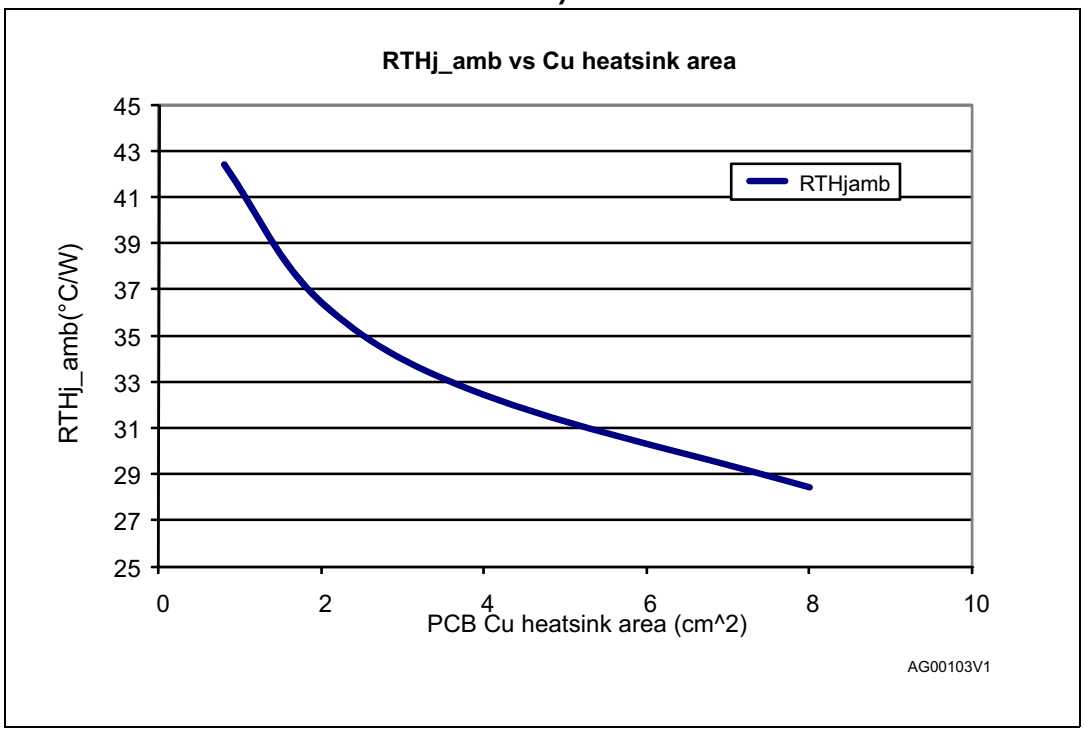


Figure 37. PowerSO-16 thermal impedance junction ambient single pulse (one channel ON)

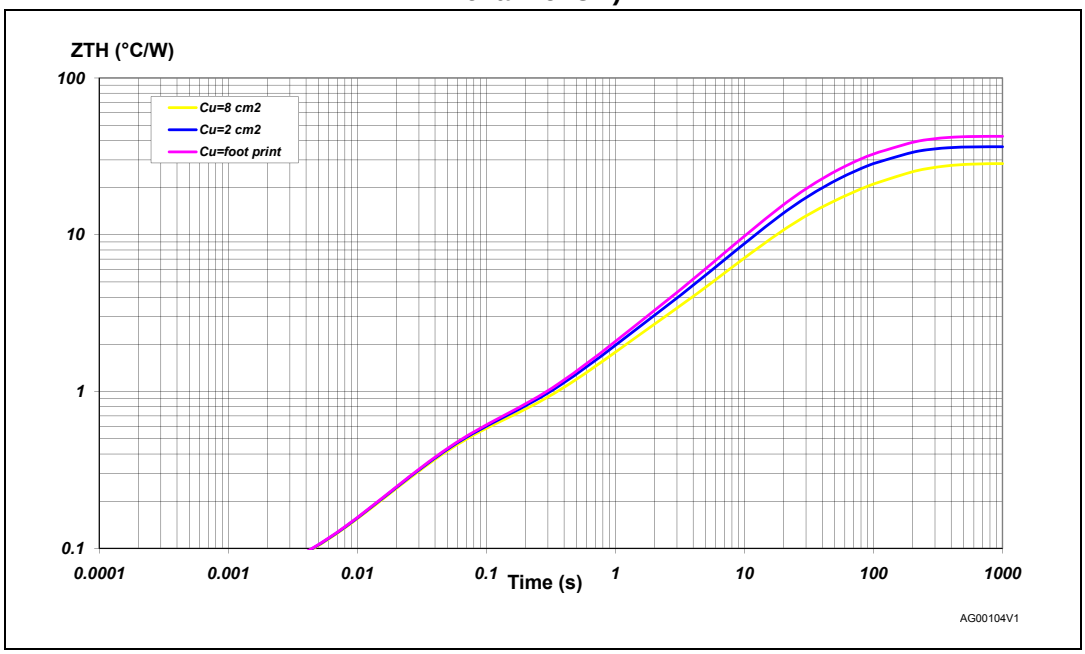
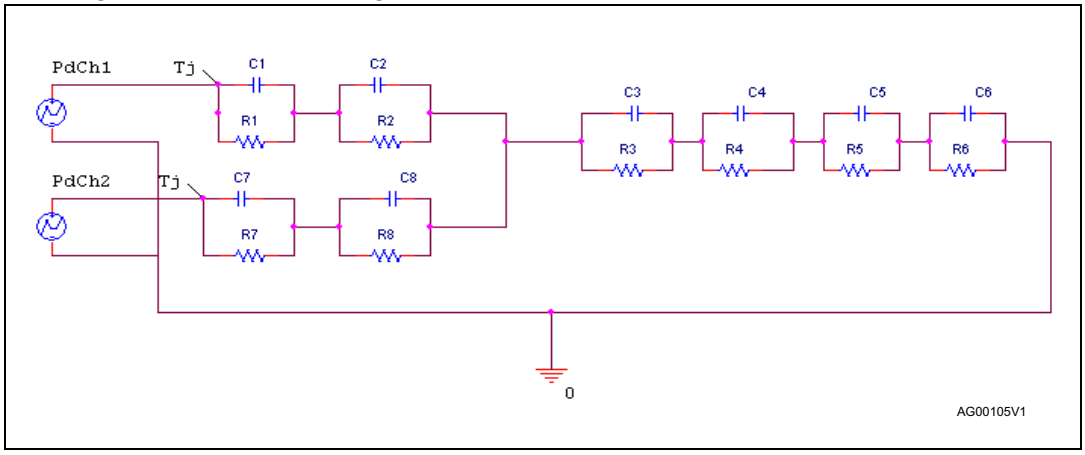


Figure 38. Thermal fitting model of a double channel HSD in PowerSO-16(1)



1. The fitting model is a semplified thermal tool and is valid for transient evolutions where the embedded protections (power limitation or thermal cycling during thermal shutdown) are not triggered.

Equation 2: pulse calculation formula

$$Z_{TH\delta} = R_{TH} \cdot \delta + Z_{THtp}(1 - \delta)$$

where $\delta = t_p / T$

Table 15. Thermal parameters

Area/island (cm^2)	Footprint	2	8
R1=R7 (°C/W)	0.05		
R2=R8 (°C/W)	0.4		
R3 (°C/W)	1		
R4 (°C/W)	7		
R5 (°C/W)	12	10	8
R6 (°C/W)	22	18	12
C1=C7 (W.s/°C)	0.01		
C2=C8 (W.s/°C)	0.1		
C3 (W.s/°C)	1		
C4 (W.s/°C)	2		
C5 (W.s/°C)	3	4	7
C6 (W.s/°C)	5	6	12

5 Package information

5.1 ECOPACK® packages

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

5.2 PowerSO-16 mechanical data

Figure 39. PowerSO-16 package dimensions

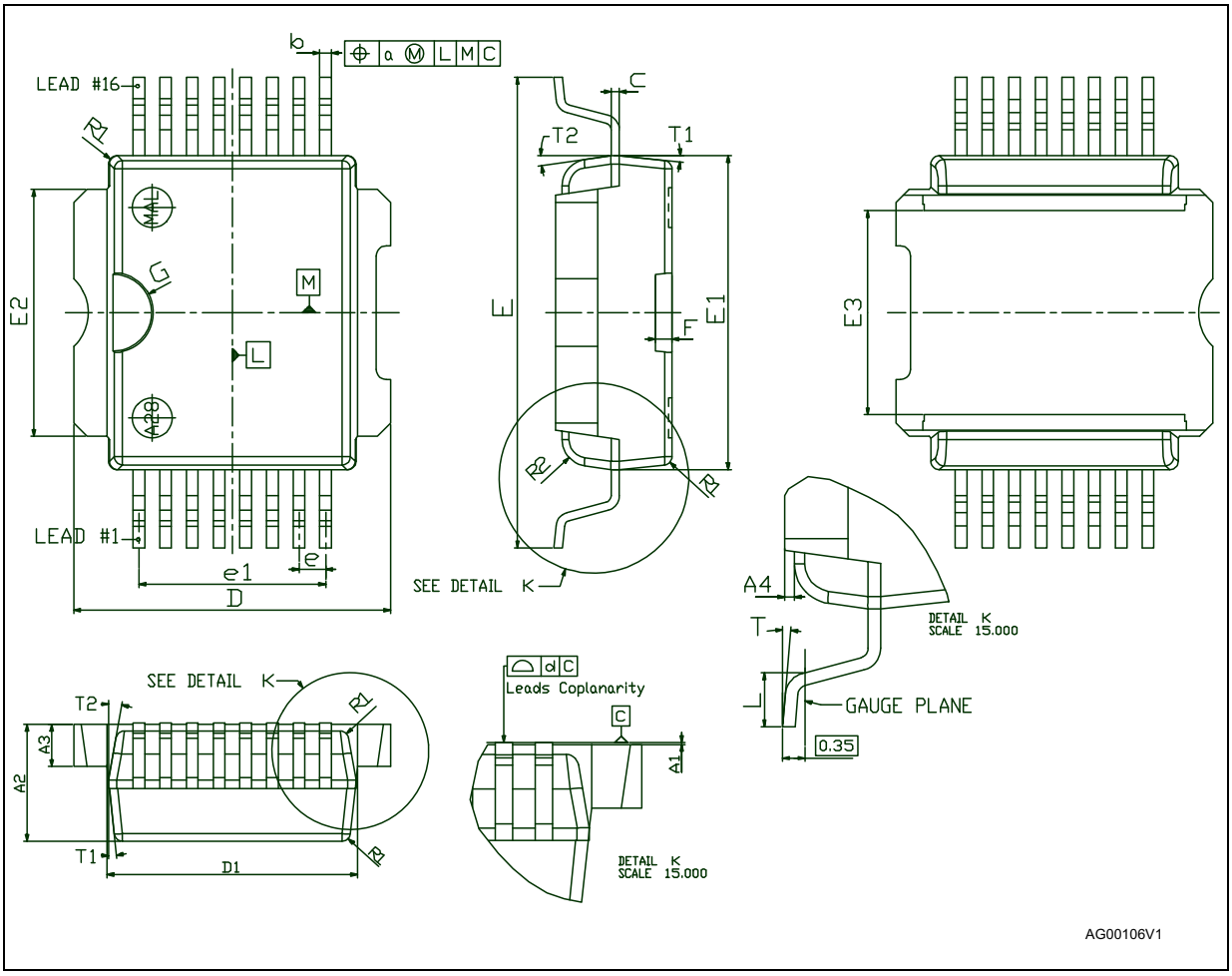
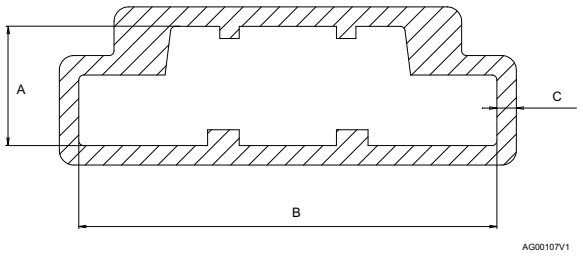


Table 16. PowerSO-16 mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A1	0	0.05	0.1
A2	3.4	3.5	3.6
A3	1.2	1.3	1.4
A4	0.15	0.2	0.25
a		0.2	
b	0.27	0.35	0.43
c	0.23	0.27	0.32
D	9.4	9.5	9.6
D1	7.4	7.5	7.6
d	0	0.05	0.1
E (1)	13.85	14.1	14.35
E1	9.3	9.4	9.5
E2	7.3	7.4	7.5
E3	5.9	6.1	6.3
e		0.8	
e1		5.6	
F		0.5	
G		1.2	
L	0.8	1	1.1
R1			0.25
R2		0.8	
T	2°	5°	8°
T1	6° (typ.)		
T2	10° (typ.)		

5.3 Packing information

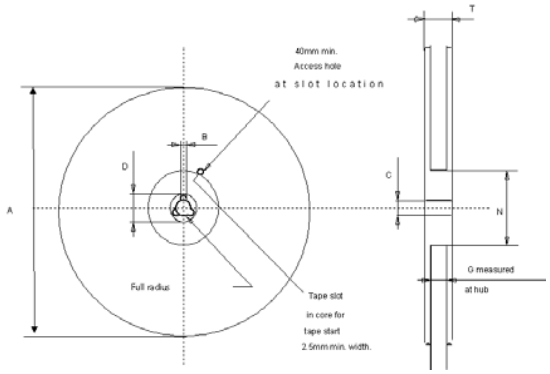
Figure 40. PowerSO-16 tube shipment (no suffix)



Base Q.ty	50
Bulk Q.ty	1000
A	4.9
B	17.2
C (± 0.1)	0.8
Tube length (± 0.5)	532

All dimensions are in mm.

Figure 41. PowerSO-16 tape and reel shipment (suffix "TR")



REEL DIMENSIONS

Base Q.ty	600
Bulk Q.ty	600
A (max)	330
B (min)	1.5
C (± 0.2)	13
F	20.2
G (+ 2 / -0)	24.4
N (min)	60
T (max)	30.4

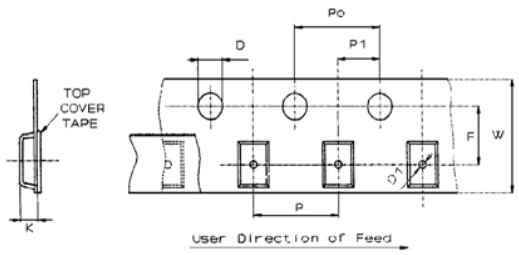
All dimensions are in mm.

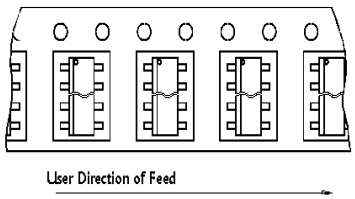
TAPE DIMENSIONS

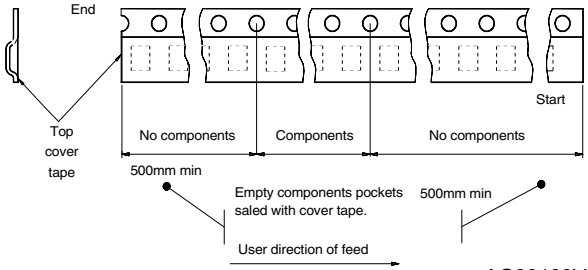
According to Electronic Industries Association (EIA) Standard 481 rev. A, Feb. 1986

Tape width	**W**	24
Tape Hole Spacing	**P0 (± 0.1)**	4
Component Spacing	**P**	24
Hole Diameter	**D (+ 0.1/-0)**	1.5
Hole Diameter	**D1 (min)**	1.5
Hole Position	**F (± 0.05)**	11.5
Compartment Depth	**K (max)**	6.5
Hole Spacing	**P1 (± 0.1)**	2

All dimensions are in mm.

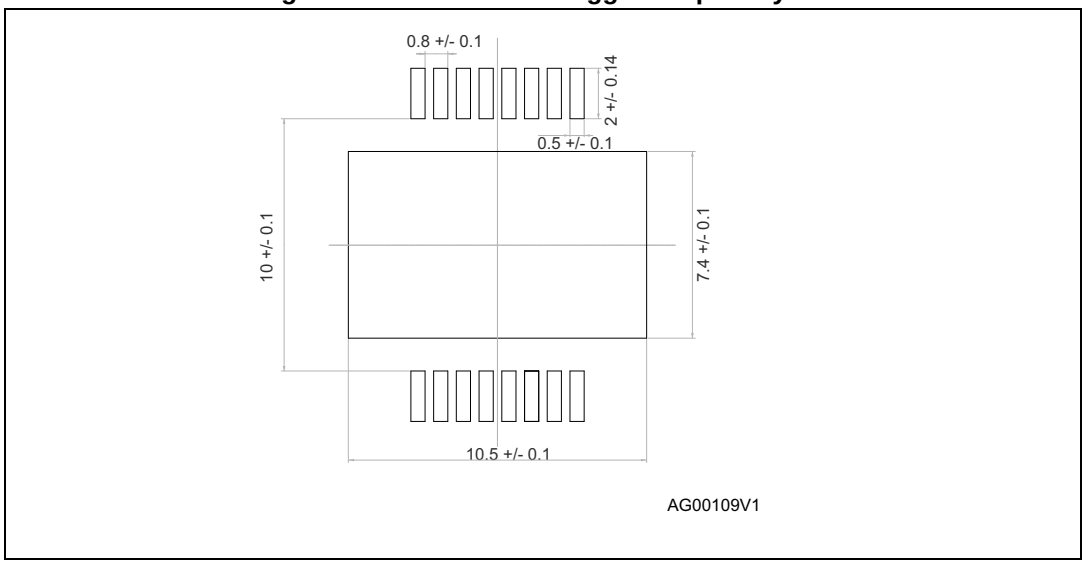






AG00108V1

Figure 42. PowerSO-16 suggested pad layout



6 Order codes

Table 17. Device summary

Package	Order codes	
	Tube	Tape and reel
PowerSO-16	VND5E006ASP-E	VND5E006ASPTR-E

7 Revision history

Table 18. Document revision history

Date	Revision	Changes
18-Apr-2010	1	Initial release.
02-Jul-2010	2	Updated *Features* list.
21-Jul-2010	3	Updated *Table 9: Current sense (8 V < VCC < 18 V)*.
19-Jan-2011	4	Added *Section 3.4: Maximum demagnetization energy (VCC = 13.5 V)* *Table 3: Absolute maximum ratings*: – E_{MAX}: updated value and test condition *Table 4: Thermal data* – Added $R_{thj\text{-}case}$ row
19-Sep-2013	5	Updated Disclaimer.
28-Oct-2013	6	Updated footnote 2 into the *Table 12: Electrical transient requirements (part 1/3)* and *Table 13: Electrical transient requirements (part 2/3)*.

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