Contents

List of tables

List of figures

1 Block diagram and pin description

Figure 1. Block diagram

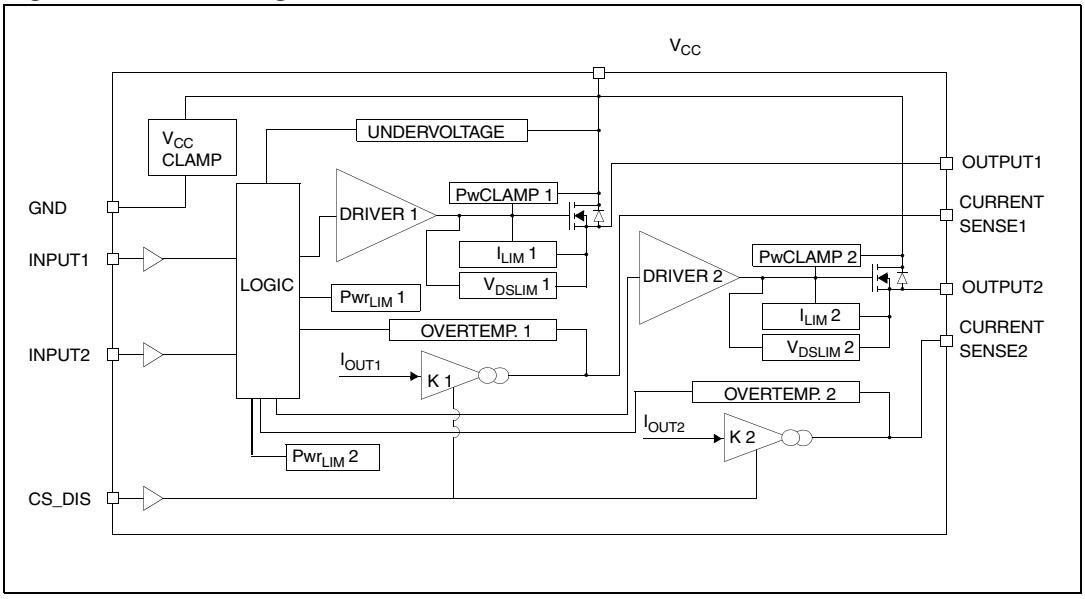
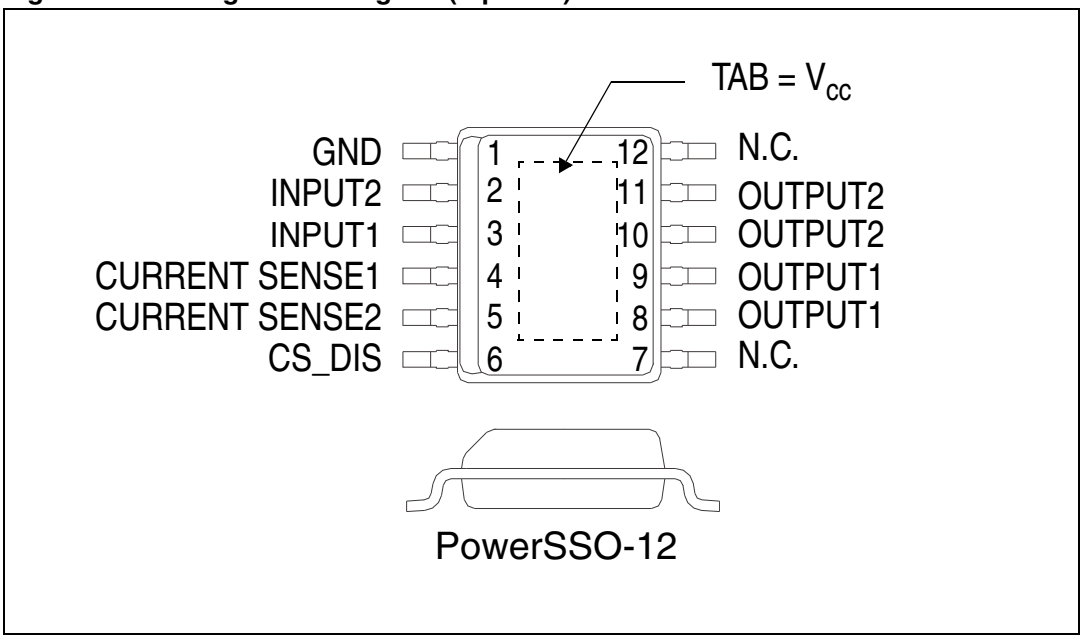


Table 2. Pin function

Name	Function
V_{CC}	Battery connection.
$OUTPUT_n$	Power output.
GND	Ground connection. Must be reverse battery protected by an external diode/resistor network.
$INPUT_n$	Voltage controlled input pin with hysteresis, CMOS compatible. Controls output switch state.
$CURRENT\ SENSE_n$	Analog current sense pin, delivers a current proportional to the load current.
CS_DIS	Active high CMOS compatible pin, to disable the current sense pin.

Figure 2. Configuration diagram (top view)



Note: The above pin configuration reflects the changes notified with PCN-APG-BOD/07/2886. The new pinout is backaward compatible with existing PCB layouts where pins #7 and 12 are connected to Vcc. For new PCB designs, these pins should be left unconnected.

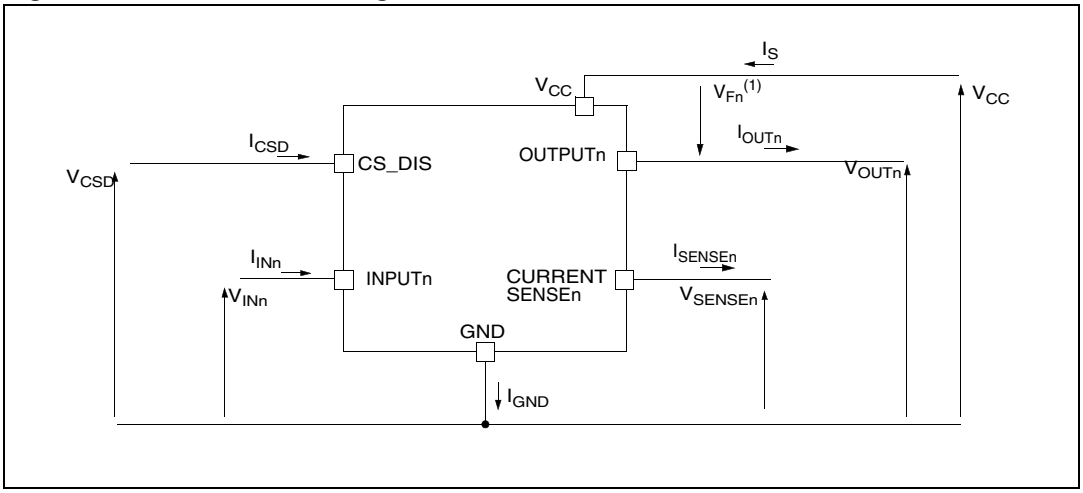
Table 3. Suggested connections for unused and N.C. pins

Connection / Pin	Current Sense	N.C.	Output	Input	CS_DIS
Floating	N.R.(1)	X	X	X	X
To ground	Through 1kΩ resistor	X	N.R.(1)	Through 10kΩ resistor	Through 10kΩ resistor

1. Not recommended.

2 Electrical specifications

Figure 3. Current and voltage conventions



Note: $V_{Fn} = V_{OUTn} - V_{CC}$ during reverse battery condition.

2.1 Absolute maximum ratings

Stressing the device above the rating listed in the “Absolute maximum ratings” table may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to the conditions in table below for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality document.

Table 4. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CC}	DC supply voltage	41	V
$-V_{CC}$	Reverse DC supply voltage	0.3	V
$- I_{GND}$	DC reverse ground pin current	200	mA
I_{OUT}	DC output current	Internally limited	A
$- I_{OUT}$	Reverse DC output current	6	A
I_{IN}	DC input current	-1 to 10	mA
I_{CSD}	DC current sense disable input current	-1 to 10	mA
$-I_{CSENSE}$	DC reverse CS pin current	200	mA
V_{CSENSE}	Current sense maximum voltage	V_{CC}-41 $+V_{CC}$	V V
E_{MAX}	Maximum switching energy (single pulse) (L=12mH; R_L=0Ω; V_{bat}=13.5V; T_{jstart}=150ºC; I_{OUT} = I_{limL}*(Typ.)*)	34	mJ

Table 4. Absolute maximum ratings (continued)

Symbol	Parameter	Value	Unit
V_{ESD}	Electrostatic discharge (Human Body Model: R=1.5KΩ; C=100pF) - INPUT - CURRENT SENSE - CS_DIS - OUTPUT - V_{CC}	 4000 2000 4000 5000 5000	 V V V V V
V_{ESD}	Charge device model (CDM-AEC-Q100-011)	750	V
T_j	Junction operating temperature	-40 to 150	°C
T_{stg}	Storage temperature	-55 to 150	°C

2.2 Thermal data

Table 5. Thermal data

Symbol	Parameter	Max value	Unit
$R_{thj\text{-}case}$	Thermal resistance junction-case (MAX) (With one channel ON)	8	°C/W
$R_{thj\text{-}amb}$	Thermal resistance junction-ambient (MAX)	See *Figure 29*	°C/W

2.3 Electrical characteristics

The values specified in this section are for 8V<V_{CC}<36V; -40°C<T_j<150°C, unless otherwise stated.

Table 6. Power section

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{CC}	Operating supply voltage		4.5	13	36	V
V_{USD}	Undervoltage shutdown			3.5	4.5	V
$V_{USDhyst}$	Undervoltage shut-down hysteresis			0.5		V
R_{ON}	On state resistance (1)	I_{OUT}= 0.5A; T_j= 25°C I_{OUT}= 0.5A; T_j= 150°C I_{OUT}= 0.5A; V_{CC}= 5V; T_j= 25°C			160 320 210	mΩ mΩ mΩ
V_{clamp}	Clamp voltage	I_S= 20 mA	41	46	52	V
I_S	Supply current	Off State; V_{CC}= 13V; T_j= 25°C; V_{IN}=V_{OUT}=V_{SENSE}=V_{CSD}=0V On State; V_{CC}=13V; V_{IN}=5V; I_{OUT}=0A		 2(2) 3	 5(2) 6	 µA mA
$I_{L(off)}$	Off state output current (1)	V_{IN}=V_{OUT}=0V; V_{CC}=13V; T_j=25°C V_{IN}=V_{OUT}=0V; V_{CC}=13V; T_j=125°C	0 0	0.01	3 5	µA
V_F	Output - V_{CC} diode voltage (1)	-I_{OUT}= 0.6A; T_j=150°C			0.7	V

1. For each channel.
2. PowerMOS leakage included.

Table 7. Switching (V_{CC}=13V, T_j=25°C)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn- On delay time	R_L= 26Ω (see *Figure 8.*)		10		µs
$t_{d(off)}$	Turn- Off delay time	R_L= 26Ω (see *Figure 8.*)		15		µs
$(dV_{OUT}/dt)_{on}$	Turn- On voltage slope	R_L= 26Ω		See *Figure 20.*		V/µs
$(dV_{OUT}/dt)_{off}$	Turn- Off voltage slope	R_L= 26Ω		See *Figure 22.*		V/µs
W_{ON}	Switching energy losses during t_{won}	R_L= 26Ω (see *Figure 8.*)		0.03		mJ
W_{OFF}	Switching energy losses during t_{woff}	R_L= 26Ω (see *Figure 8.*)		0.02		mJ

Table 8. Logic input

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{IL}	Input low level voltage				0.9	V
I_{IL}	Low level input current	V_{IN}= 0.9V	1			µA
V_{IH}	Input high level voltage		2.1			V
I_{IH}	High level input current	V_{IN}= 2.1V			10	µA
$V_{I(hyst)}$	Input hysteresis voltage		0.25			V
V_{ICL}	Input clamp voltage	I_{IN}= 1mA I_{IN}= -1mA	5.5	 -0.7	7	V V
V_{CSDL}	CS_DIS low level voltage				0.9	V
I_{CSDL}	Low level CS_DIS current	V_{CSD}= 0.9V	1			µA
V_{CSDH}	CS_DIS high level voltage		2.1			V
I_{CSDH}	High level CS_DIS current	V_{CSD}= 2.1V			10	µA
$V_{CSD(hyst)}$	CS_DIS hysteresis voltage		0.25			V
V_{CSCL}	CS_DIS clamp voltage	I_{CSD}= 1mA I_{CSD}= -1mA	5.5	 -0.7	7	V V

Table 9. Protection and diagnostics(1)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{limH}	DC short circuit current	V_{CC}= 13V 5V<V_{CC}<36V	3.8	5	7.5 7.5	A A
I_{limL}	Short circuit current during thermal cycling	V_{CC}= 13V; T_R<T_j<T_{TSD}		2		A
T_{TSD}	Shutdown temperature		150	175	200	°C
T_R	Reset temperature		T_{RS} + 1	T_{RS} + 5		°C
T_{RS}	Thermal reset of STATUS		135			°C
T_{HYST}	Thermal hysteresis (T_{TSD}-T_R)			7		°C
V_{DEMAG}	Turn-Off output voltage clamp	I_{OUT}= 1A; V_{IN}= 0; L= 20mH	V_{CC}-41	V_{CC}-46	V_{CC}-52	V
V_{ON}	Output voltage drop limitation	I_{OUT}= 0.03A; T_j= -40°C...150°C (see *Figure 9*.)		25		mV

1. To ensure long term reliability under heavy overload or short circuit conditions, protection and related diagnostic signals must be used together with a proper software strategy. If the device is subjected to abnormal conditions, this software must limit the duration and number of activation cycles.

Table 10. Current sense (8V<VCC<16V)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
K_0	I_{OUT}/I_{SENSE}	I_{OUT}= 0.025A; V_{SENSE}= 0.5V; V_{CSD}=0V; T_j= -40°C...150°C	260	500	750	
K_1	I_{OUT}/I_{SENSE}	I_{OUT}= 0.35A; V_{SENSE}=0.5V; V_{CSD}=0V; T_j= -40°C...150°C I_{OUT}=0.35A; V_{SENSE}=0.5V; V_{CSD}=0V; T_j= 25°C...150°C	320 360	450 450	590 540	
dK_1/K_1 (1)	Current sense ratio drift	I_{OUT}= 0.35A; V_{SENSE}= 0.5V; V_{CSD}=0V; T_J= -40 °C to 150 °C	-13		+13	%
K_2	I_{OUT}/I_{SENSE}	I_{OUT}= 0.5A; V_{SENSE}= 4V; V_{CSD}= 0V; T_j= -40°C...150°C I_{OUT}= 0.5A; V_{SENSE}= 4V; V_{CSD}= 0V; T_j= 25°C...150°C	360 380	440 440	540 510	
dK_2/K_2 (1)	Current sense ratio drift	I_{OUT}= 0.5 A; V_{SENSE}= 4 V; V_{CSD}= 0V; T_J= -40 °C to 150 °C	-8		+8	%
K_3	I_{OUT}/I_{SENSE}	I_{OUT}= 1.5A; V_{SENSE}=4V; V_{CSD}=0V; T_j= -40°C...150°C I_{OUT}=1.5A; V_{SENSE}=4V; V_{CSD}=0V; T_j= 25°C...150°C	410 420	440 440	480 460	
dK_3/K_3 (1)	Current sense ratio drift	I_{OUT}= 1.5 A; V_{SENSE}= 4 V; V_{CSD}=0V; T_J= -40 °C to 150 °C	-4		+4	%
I_{SENSE0}	Analog sense leakage current	I_{OUT}=0A; V_{SENSE}=0V; V_{CSD}=5V; V_{IN}=0V; T_j=-40°C...150°C V_{CSD}=0V; V_{IN}=5V; T_j=-40°C...150°C I_{OUT}=0.6A; V_{SENSE}=0V; V_{CSD}=5V; V_{IN}=5V; T_j= -40°C...150°C	0 0 0		1 2 1	µA µA µA
I_{OL}	Openload ON state current detection threshold	V_{IN} = 5V, I_{SENSE}= 5 µA	1		5	mA
V_{SENSE}	Max analog senseoutput voltage	I_{OUT}=1.5A; V_{CSD}=0V;	5			V
V_{SENSEH}	Analog sense output voltage in overtemperature condition	V_{CC}=13V; R_{SENSE}= 3.9KΩ;		9		V
I_{SENSEH}	Analog sense output current in overtemperature condition	V_{CC}=13V; V_{SENSE}= 5V;		8		mA

Table 10. Current sense (8V<VCC<16V) (continued)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{DSENSE1H}$	Delay response time from falling edge of CS_DIS pin	V_{SENSE}<4V, 0.08A<Iout<1.5A I_{SENSE}=90% of $I_{SENSE\ max}$ (see *Figure 4.*)		50	100	µs
$t_{DSENSE1L}$	Delay response time from rising edge of CS_DIS pin	V_{SENSE}<4V, 0.08A<Iout<1.5A I_{SENSE}=10% of $I_{SENSE\ max}$ (see *Figure 4.*)		5	20	µs
$t_{DSENSE2H}$	Delay response time from rising edge of INPUT pin	V_{SENSE}<4V, 0.08A<Iout<1.5A I_{SENSE}=90% of $I_{SENSE\ max}$ (see *Figure 4.*)		80	150	µs
$\Delta t_{DSENSE2H}$	Delay response time between rising edge of output current and rising edge of current sense	V_{SENSE} < 4V, I_{SENSE} = 90% of $I_{SENSEMAX}$, I_{OUT} = 90% of I_{OUTMAX} I_{OUTMAX}=2A (see *Figure 5*)			20	□□µs
$t_{DSENSE2L}$	Delay response time from falling edge of INPUT pin	V_{SENSE}<4V, 0.08A<Iout<1.5A I_{SENSE}=10% of $I_{SENSE\ max}$ (see *Figure 4.*)		100	250	µs

1. Parameter guaranteed by design; it is not tested.

Figure 4. Current sense delay characteristics

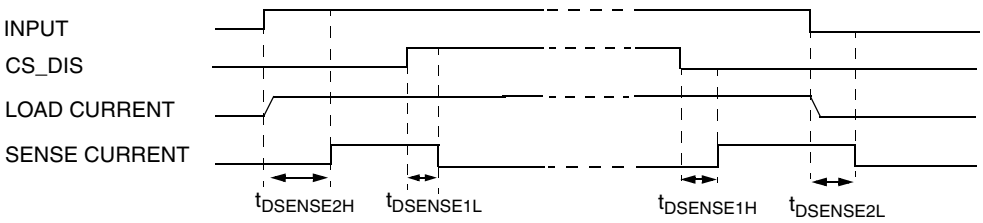


Figure 5. Delay response time between rising edge of ouput current and rising edge of current sense (CS enabled)

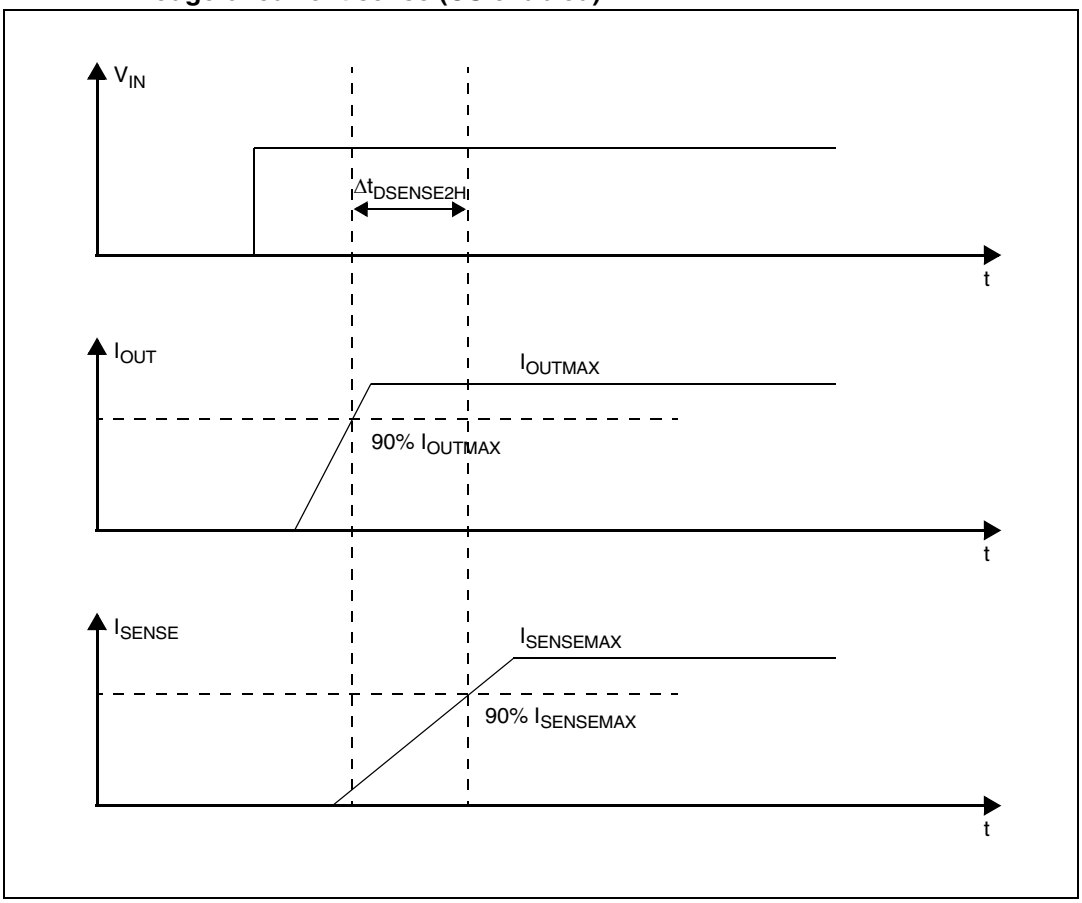


Figure 6. I_{out}/ I_{sense} vs. I_{out} (see *Table 10* for details)

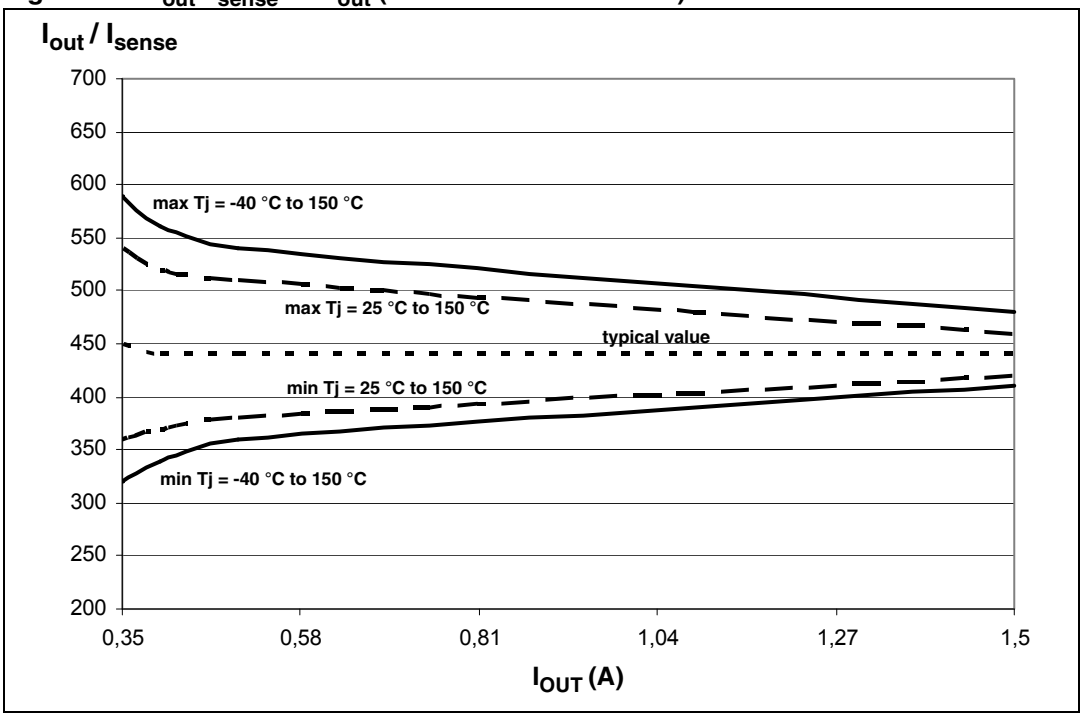
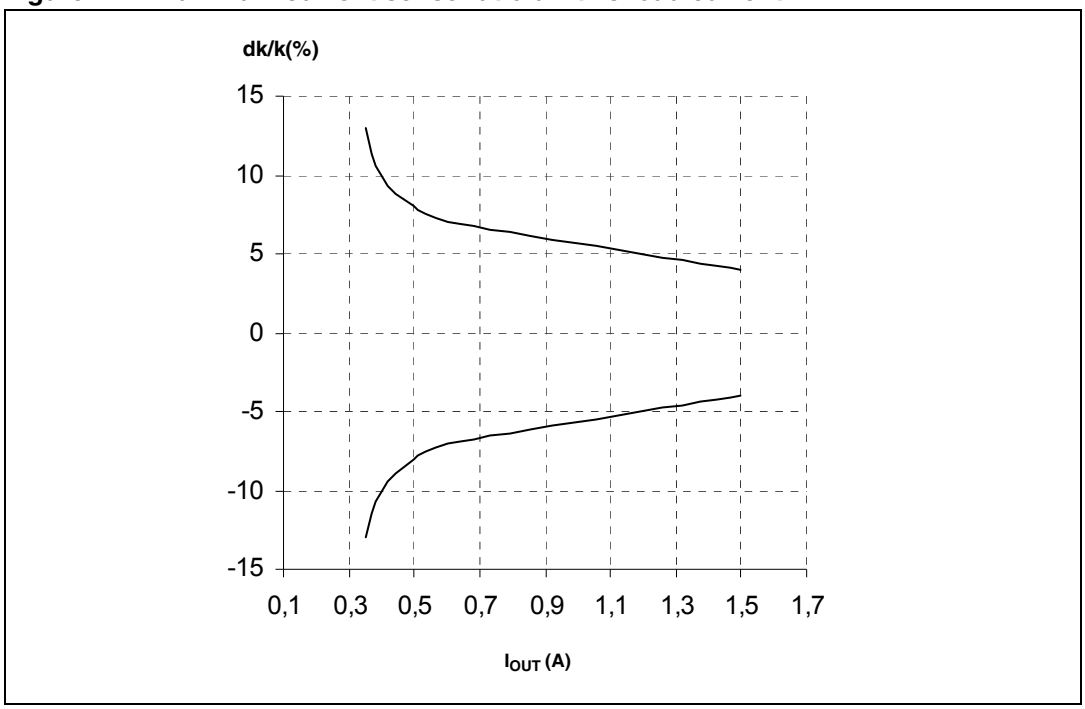


Figure 7. Maximum current sense ratio drift vs load current



Note: Parameter guaranteed by design; it is not tested.

Table 11. Truth table

Conditions	INPUT	OUTPUT	SENSE (V_{CSD}=0V)(1)
Normal operation	L H	L H	0 Nominal
Overtemperature	L H	L L	0 V_{SENSEH}
Undervoltage	L H	L L	0 0
Short circuit to GND ($R_{sc} \leq 10\ m\Omega$)	L H H	L L L	0 0 if $T_j < T_{TSD}$ V_{SENSEH} if $T_j > T_{TSD}$
Short circuit to V_{CC}	L H	H H	0 < Nominal
Negative output voltage clamp	L	L	0

1. If the V_{CSD} is high, the SENSE output is at a high impedance, its potential depends on leakage currents and external circuit.

Figure 8. Switching characteristics

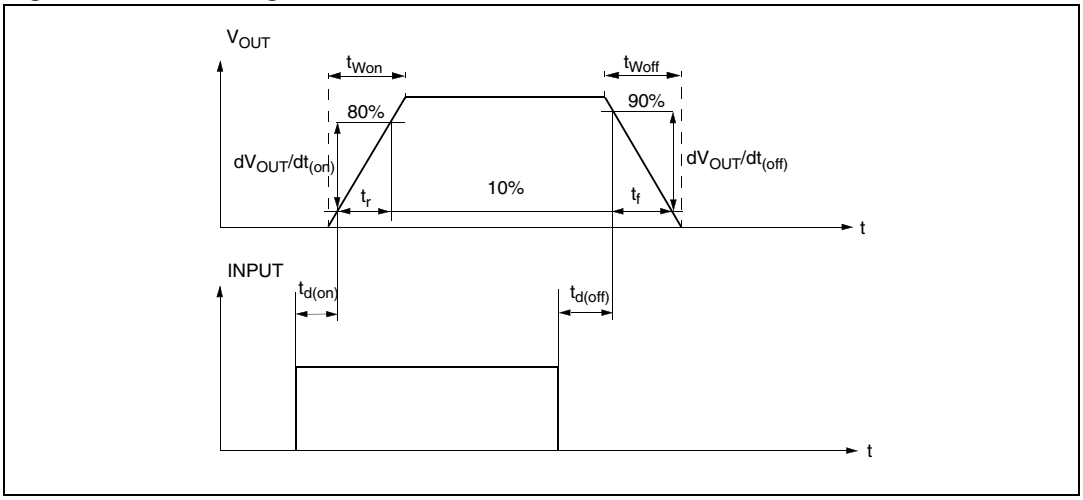


Figure 9. Output voltage drop limitation

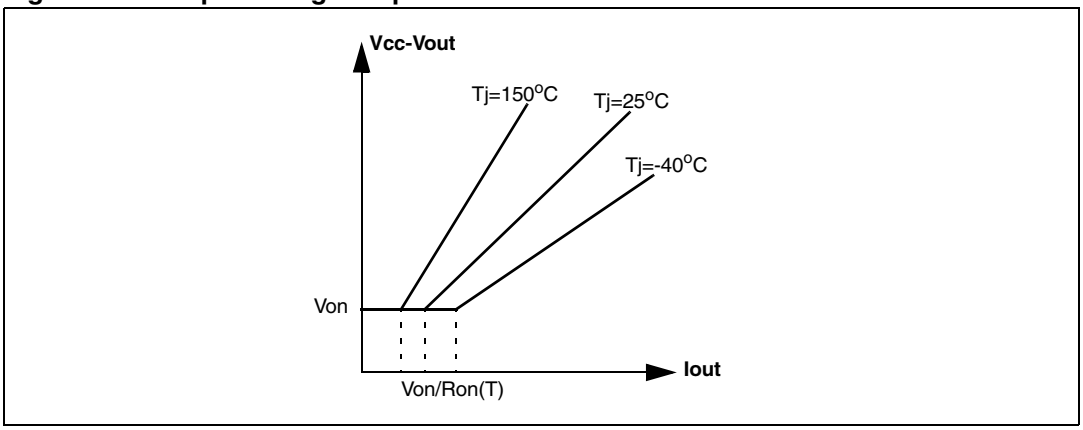


Table 12. Electrical transient requirements

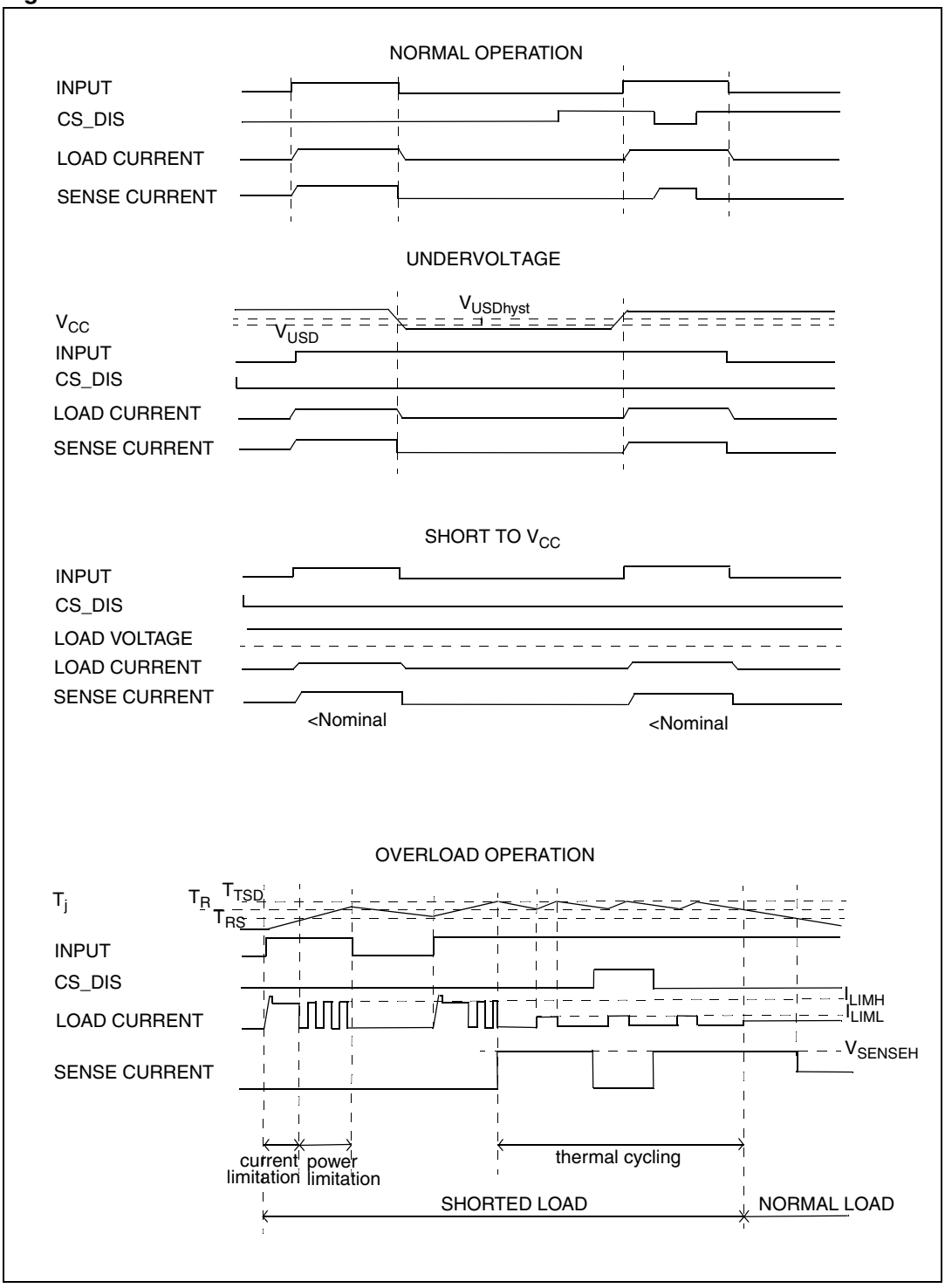
ISO 7637-2: 2004(E) Test pulse	Test levels (1)		Number of pulses or test times	Burst cycle/pulse repetition time		Delays and impedance
	III	IV				
1	-75V	-100V	5000 pulses	0.5 s	5 s	2 ms, 10 Ω
2a	+37V	+50V	5000 pulses	0.2 s	5 s	50 µs, 2 Ω
3a	-100V	-150V	1h	90 ms	100 ms	0.1 µs, 50 Ω
3b	+75V	+100V	1h	90 ms	100 ms	0.1 µs, 50 Ω
4	-6V	-7V	1 pulse			100 ms, 0.01 Ω
5b (2)	+65V	+87V	1 pulse			400 ms, 2 Ω

ISO 7637-2: 2004(E) Test pulse	Test level results(1)	
	III	IV
1	C	C
2a	C	C
3a	C	C
3b	C	C
4	C	C
5b (2)	C	C

1. The above test levels must be considered referred to V_{CC} = 13.5V except for pulse 5b.
2. Valid in case of external load dump clamp: 40V maximum referred to ground.

Class	Contents
C	All functions of the device are performed as designed after exposure to disturbance.
E	One or more functions of the device are not performed as designed after exposure to disturbance and cannot be returned to proper operation without replacing the device.

Figure 10. Waveforms



2.4 Electrical characteristics curves

Figure 11. Off state output current

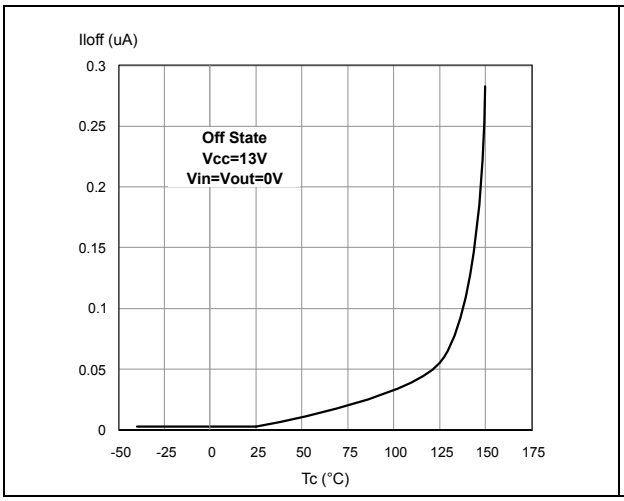


Figure 12. High level input current

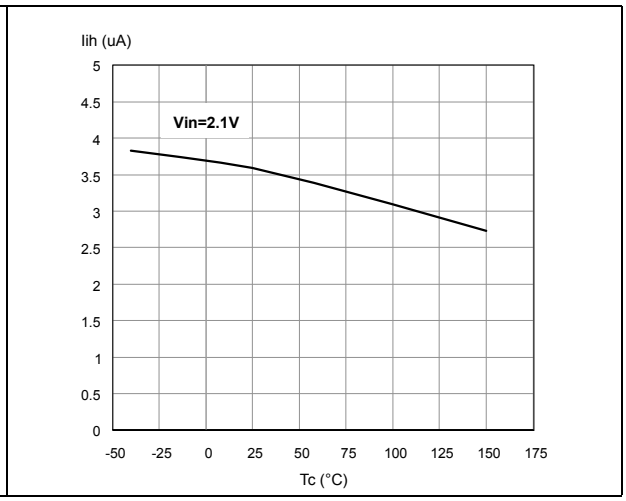


Figure 13. Input clamp voltage

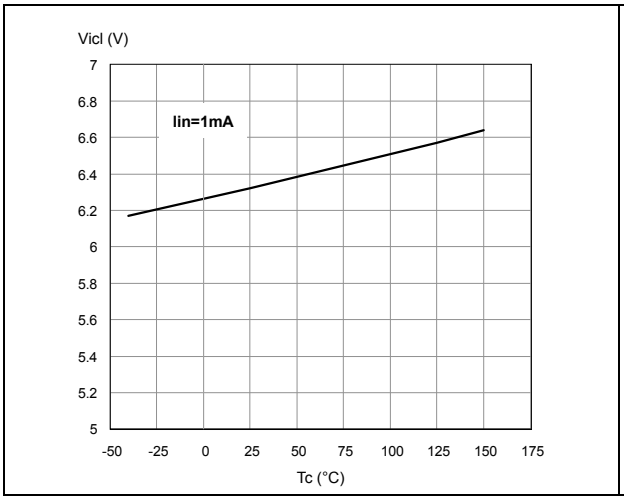


Figure 14. Input low level

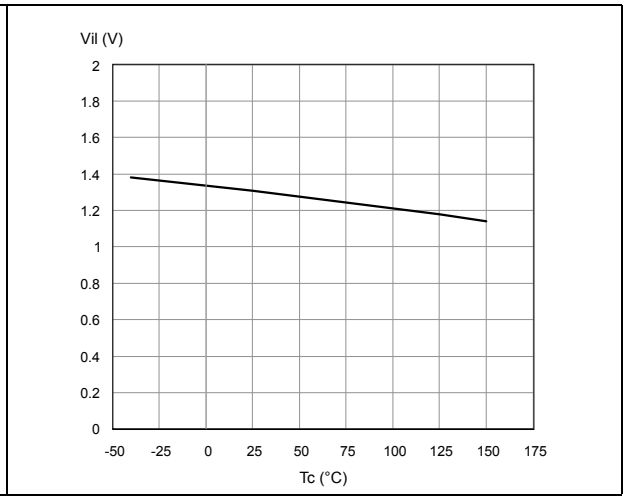


Figure 15. Input high level

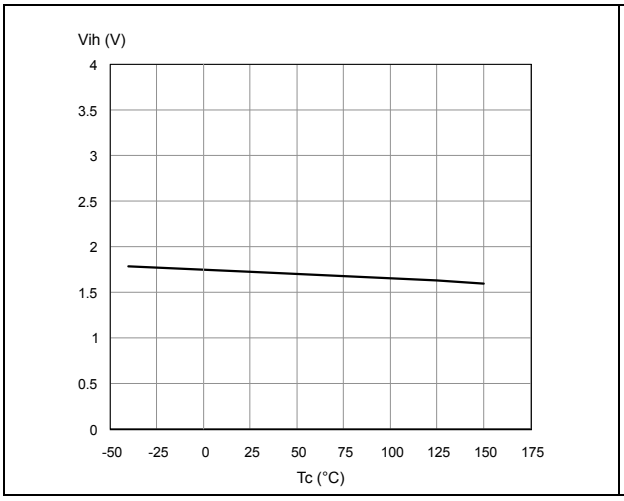


Figure 16. Input hysteresis voltage

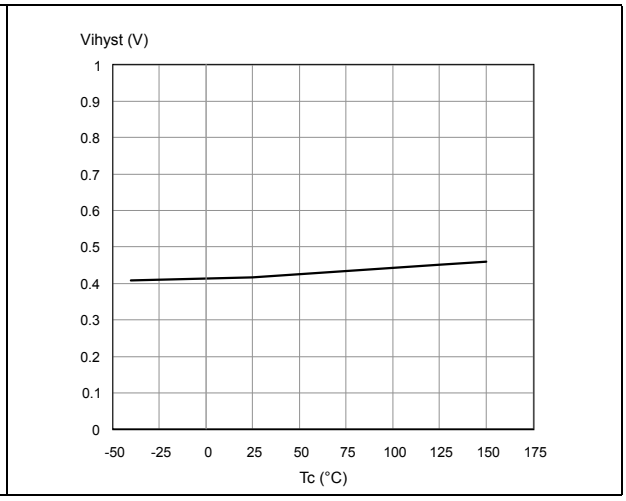


Figure 17. On state resistance vs. T_{case}

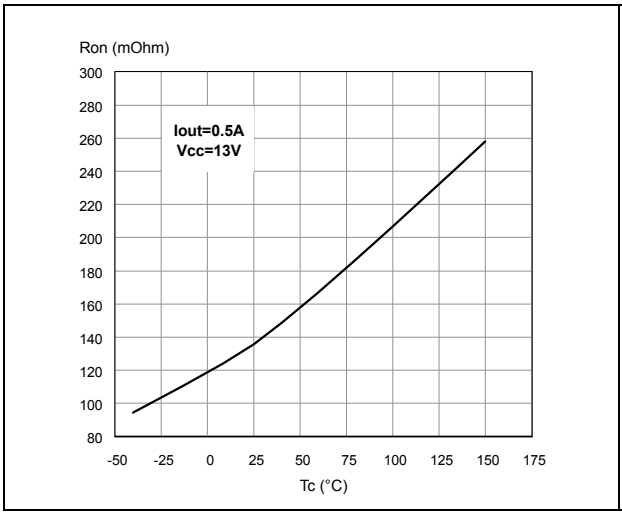


Figure 18. On state resistance vs. V_{CC}

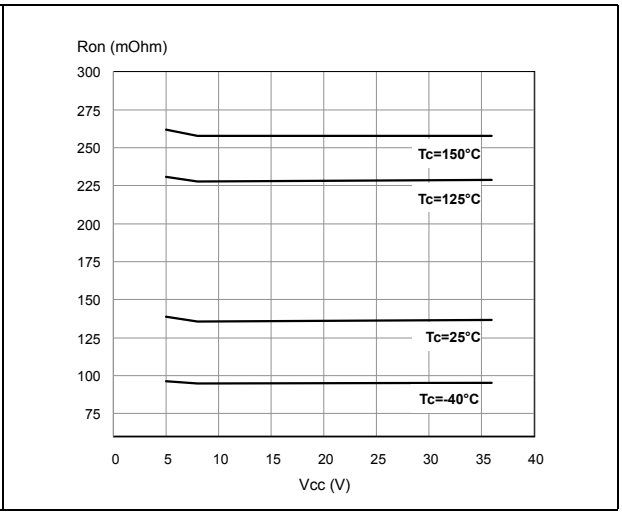


Figure 19. Undervoltage shutdown

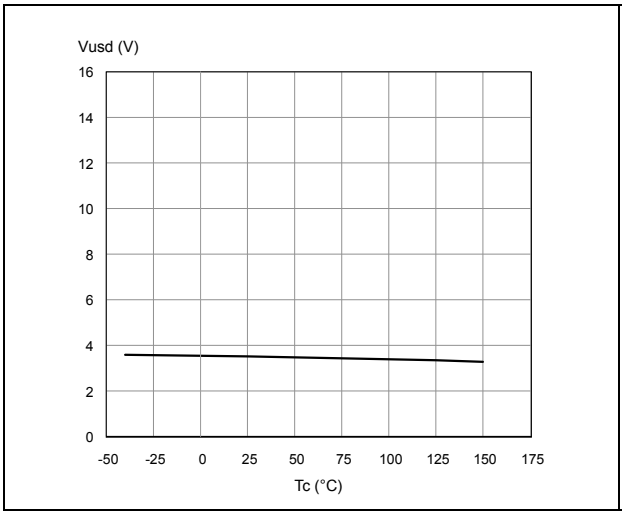


Figure 20. Turn-On voltage slope

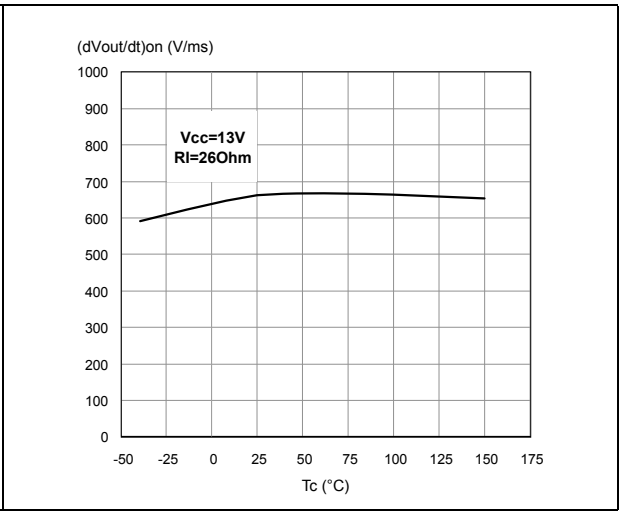


Figure 21. I_{LIMH} vs. T_{case}

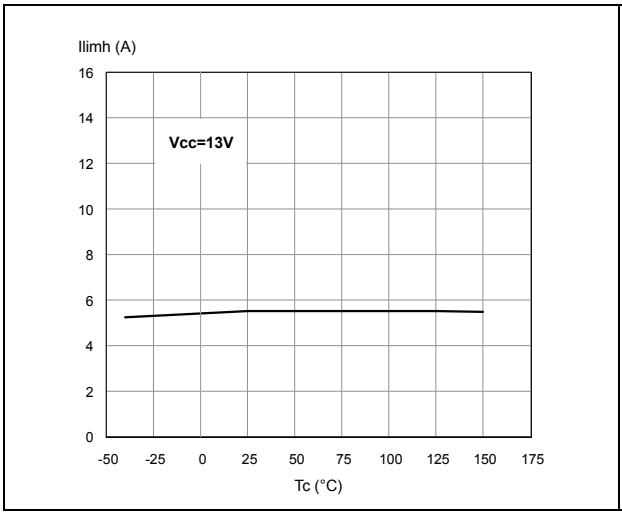


Figure 22. Turn-Off voltage slope

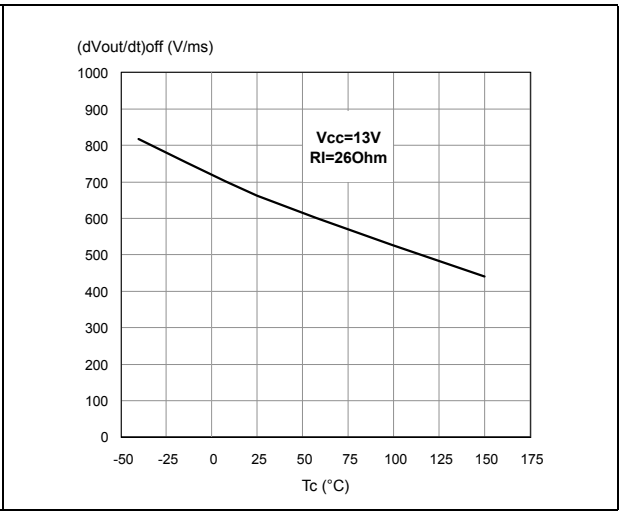


Figure 23. CS_DIS high level voltage

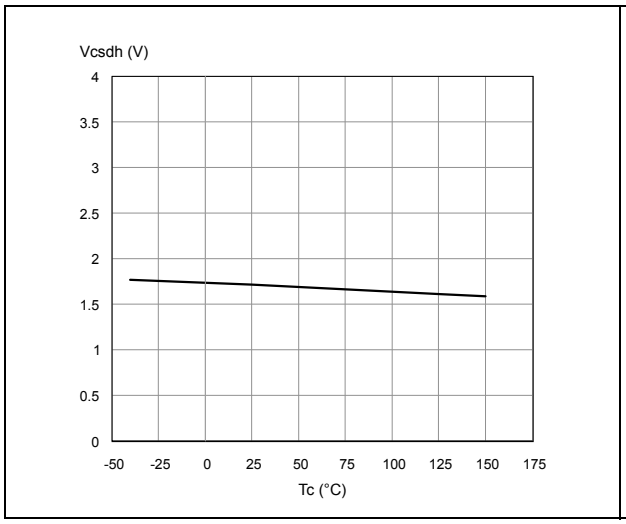


Figure 24. CS_DIS clamp voltage

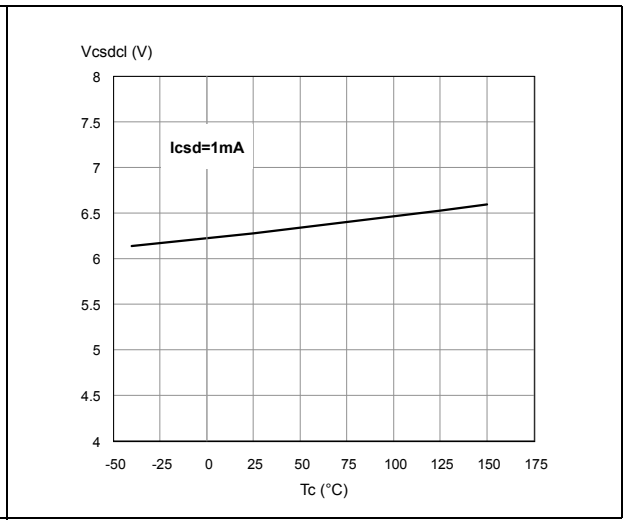
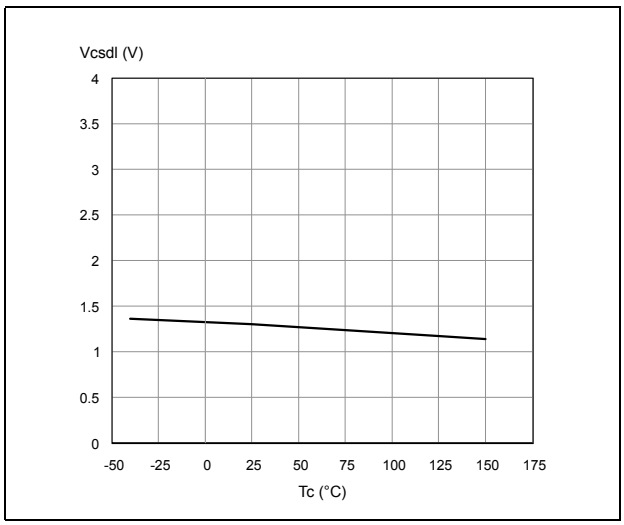
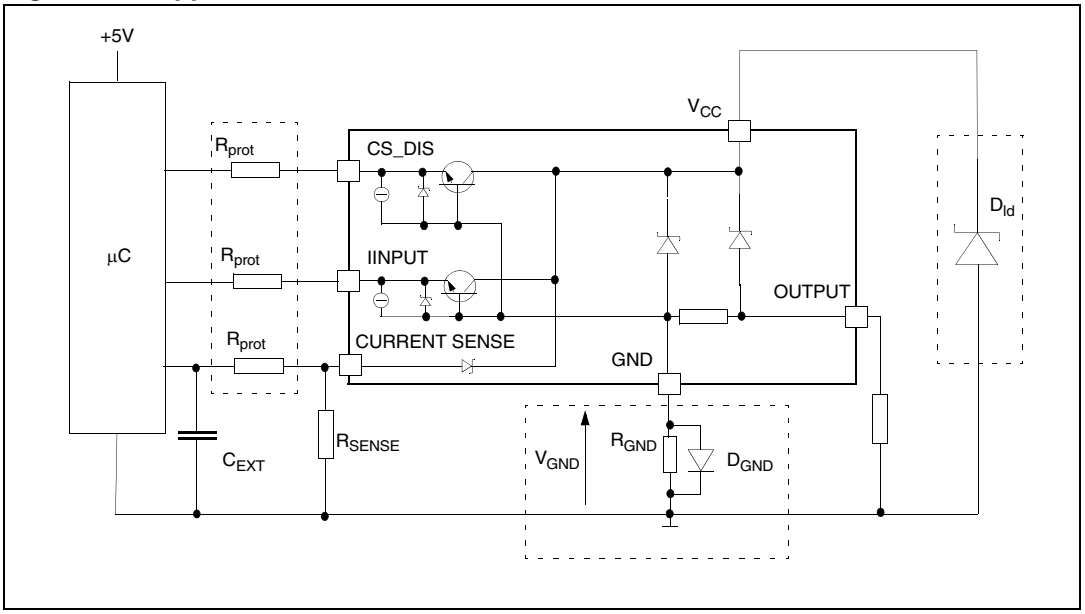


Figure 25. CS_DIS low level voltage



3 Application information

Figure 26. Application schematic



Note: Channel 2 has the same internal circuit as channel 1.

3.1 GND protection network against reverse battery

3.1.1 Solution 1 : resistor in the ground line (R_{GND} only)

This can be used with any type of load.

The following is an indication on how to dimension the R_{GND} resistor.

1. $R_{GND} \leq 600mV / (I_{S(on)max})$.
2. $R_{GND} \geq (-V_{CC}) / (-I_{GND})$

where $-I_{GND}$ is the DC reverse ground pin current and can be found in the absolute maximum rating section of the device datasheet.

Power Dissipation in R_{GND} (when $V_{CC}<0$: during reverse battery situations) is:

$P_D= (-V_{CC})^2/R_{GND}$

This resistor can be shared amongst several different HSDs. Please note that the value of this resistor should be calculated with formula (1) where $I_{S(on)max}$ becomes the sum of the maximum on-state currents of the different devices.

Please note that if the microprocessor ground is not shared by the device ground then the R_{GND} will produce a shift ($I_{S(on)max}$ * R_{GND}) in the input thresholds and the status output values. This shift will vary depending on how many devices are ON in the case of several high side drivers sharing the same R_{GND}.

If the calculated power dissipation leads to a large resistor or several devices have to share the same resistor then ST suggests to utilize Solution 2 (see below).

3.1.2 Solution 2 : diode (D_{GND}) in the ground line

A resistor (R_{GND}=1kΩ) should be inserted in parallel to D_{GND} if the device drives an inductive load.

This small signal diode can be safely shared amongst several different HSDs. Also in this case, the presence of the ground network will produce a shift (≈600mV) in the input threshold and in the status output values if the microprocessor ground is not common to the device ground. This shift will not vary if more than one HSD shares the same diode/resistor network.

3.2 Load dump protection

D_{ld} is necessary (Voltage Transient Suppressor) if the load dump peak voltage exceeds the V_{CC} max DC rating. The same applies if the device is subject to transients on the V_{CC} line that are greater than the ones shown in the ISO 7637-2: 2004(E) table.

3.3 MCU I/Os protection

If a ground protection network is used and negative transient are present on the V_{CC} line, the control pins will be pulled negative. ST suggests to insert a resistor (R_{prot}) in line to prevent the MCU I/Os pins to latch-up.

The value of these resistors is a compromise between the leakage current of MCU and the current required by the HSD I/Os (Input levels compatibility) with the latch-up limit of MCU I/Os.

$-V_{CCpeak}/I_{latchup} \leq R_{prot} \leq (V_{OH\mu C}-V_{IH}-V_{GND}) / I_{IHmax}$

Calculation example:

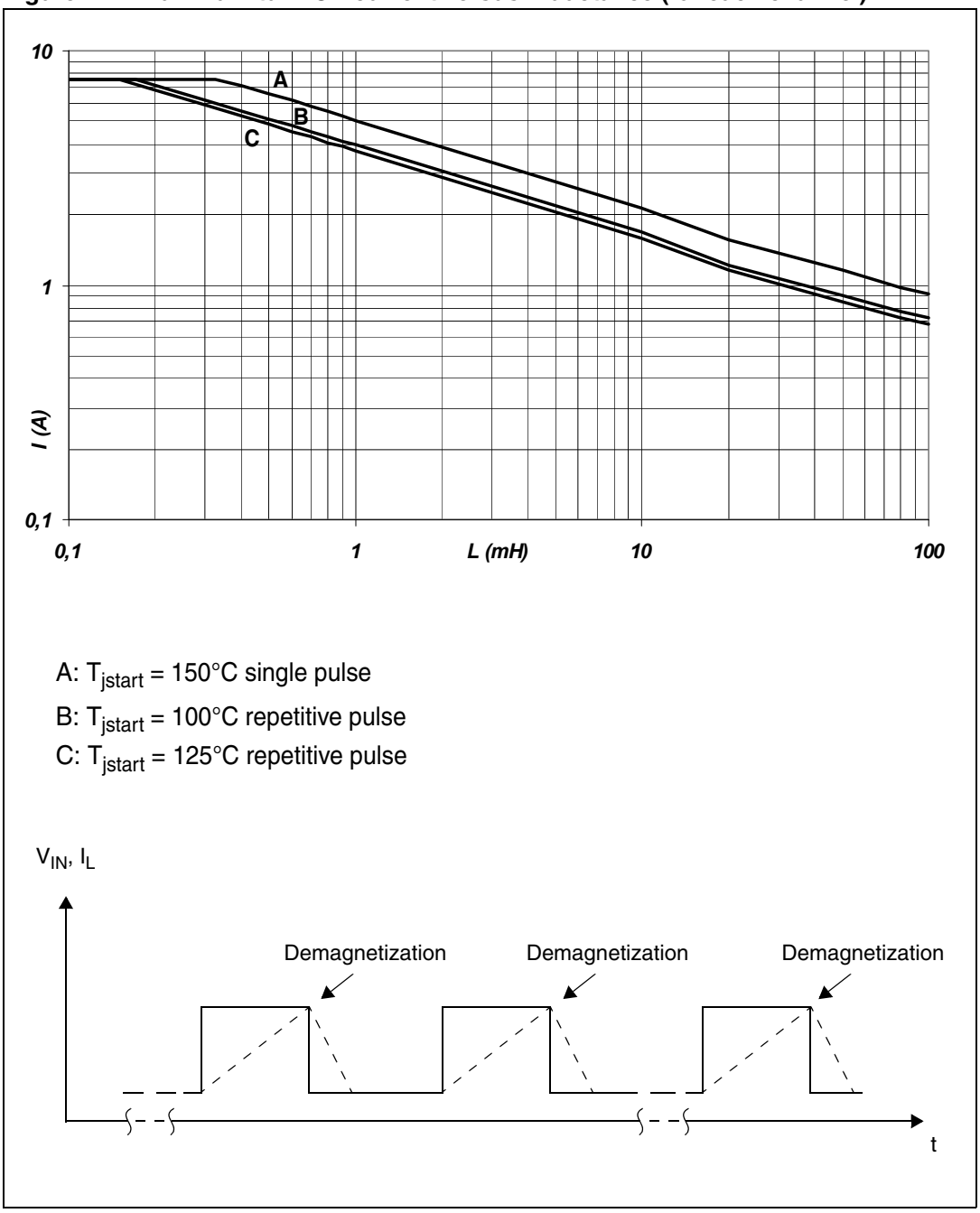
For V_{CCpeak}= - 100V and $I_{latchup} \geq$ 20mA; $V_{OH\mu C} \geq$ 4.5V

5kΩ ≤ R_{prot} ≤ 180kΩ.

Recommended values: R_{prot} =10kΩ, C_{EXT}=10nF.

3.4 Maximum demagnetization energy (V_{CC} = 13.5V)

Figure 27. Maximum turn-Off current versus inductance (for each channel)



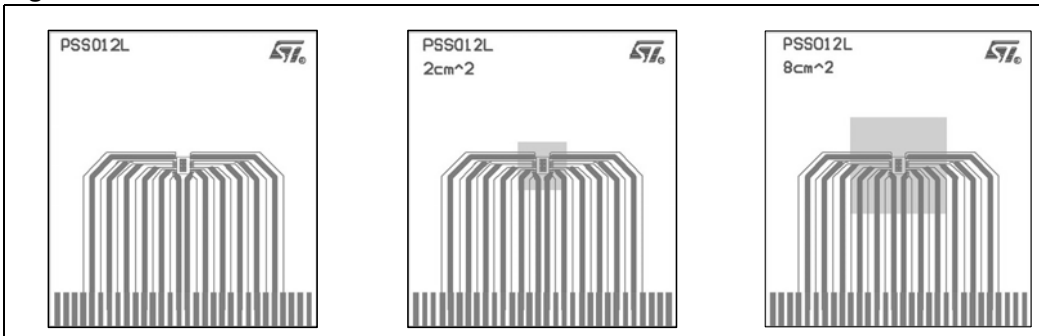
Note: Values are generated with R_L = 0 Ω.

In case of repetitive pulses, T_{jstart} (at beginning of each demagnetization) of every pulse must not exceed the temperature specified above for curves A and B.

4 Package and PC board thermal data

4.1 PowerSSO-12™ thermal data

Figure 28. PowerSSO-12™ PC board



Note: Layout condition of R_{th} and Z_{th} measurements (PCB: Double layer, Thermal Vias, FR4 area= 77mm x 86mm, PCB thickness=1.6mm, Cu thickness=70µm (front and back side), Copper areas: from minimum pad lay-out to 8cm^2).

Figure 29. $R_{thj\text{-}amb}$ vs. PCB copper area in open box free air condition (one channel ON)

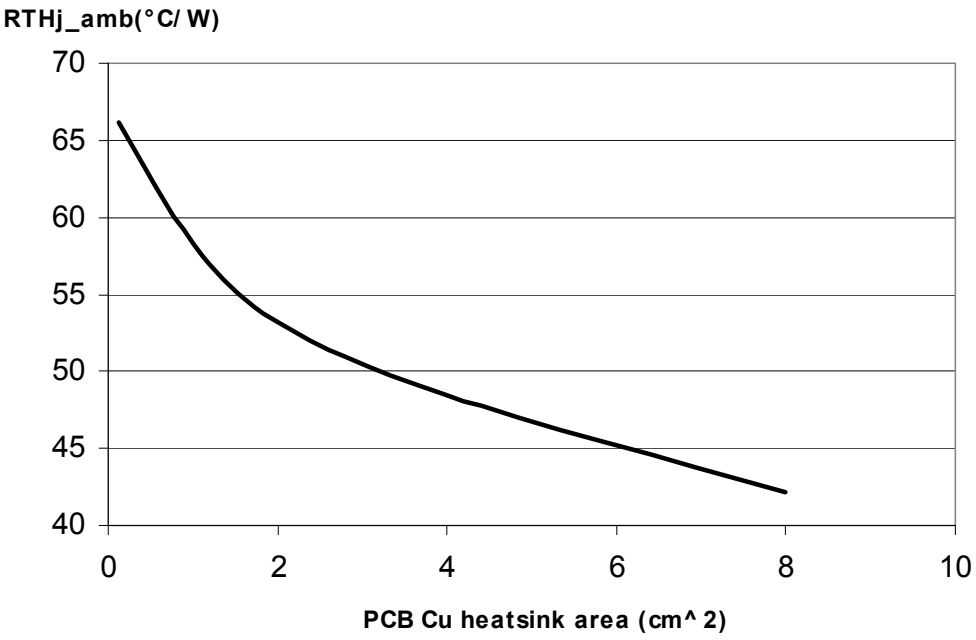
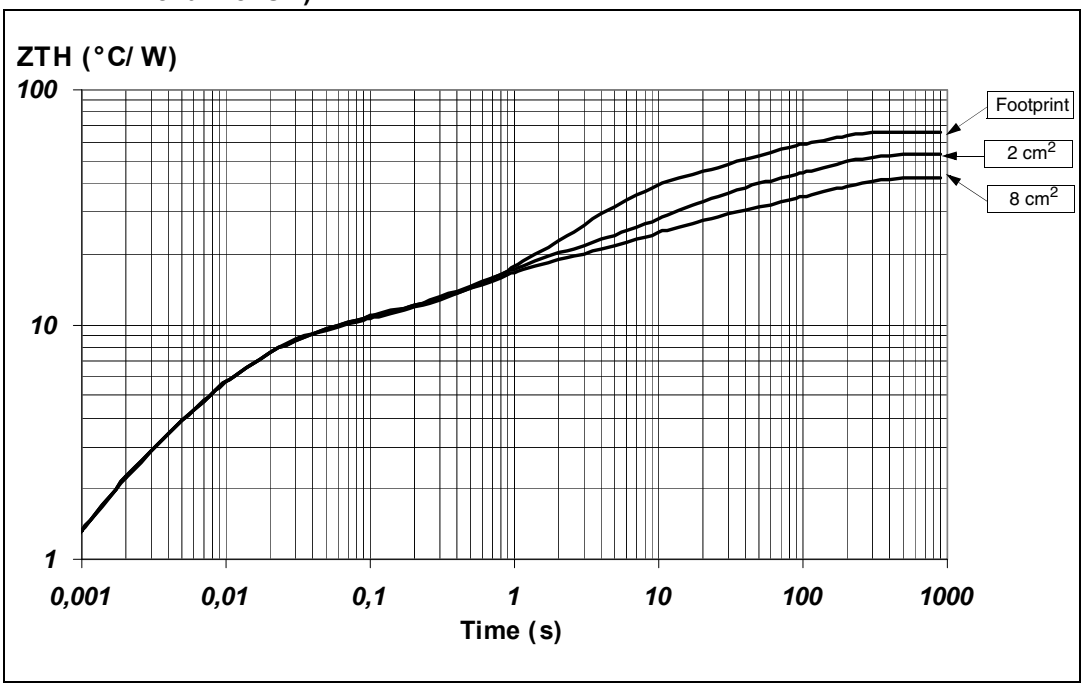


Figure 30. PowerSSO-12™ thermal impedance junction ambient single pulse (one channel ON)

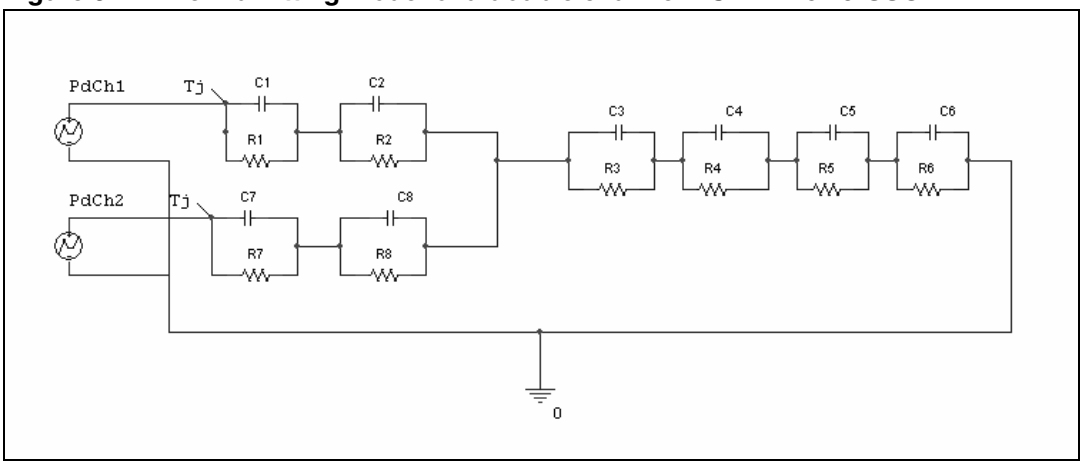


Equation 1: pulse calculation formula

$$Z_{TH\delta} = R_{TH} \cdot \delta + Z_{THtp}(1 - \delta)$$

where $\delta = t_P/T$

Figure 31. Thermal fitting model of a double channel HSD in PowerSSO-12™ (a)



a. The fitting model is a semplified thermal tool and is valid for transient evolutions where the embedded protections (power limitation or thermal cycling during thermal shutdown) are not triggered.

Table 13. Thermal parameters

Area/island (cm^2)	Footprint	2	8
R1= R7 (°C/W)	1.2		
R2= R8 (°C/W)	6		
R3 (°C/W)	3		
R4 (°C/W)	8	8	7
R5 (°C/W)	22	15	10
R6 (°C/W)	26	20	15
C1= C7 (W.s/°C)	0.0008		
C2= C8 (W.s/°C)	0.0016		
C3 (W.s/°C)	0.0166		
C4 (W.s/°C)	0.2	0.1	0.1
C5 (W.s/°C)	0.27	0.8	1
C6 (W.s/°C)	3	6	9

5 Package and packing information

5.1 ECOPACK® packages

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second-level interconnect. The category of Second-Level Interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97.
The maximum ratings related to soldering conditions are also marked on the inner box label.
ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com.

5.2 Package mechanical data

Figure 32. PowerSSO-12™ package dimensions

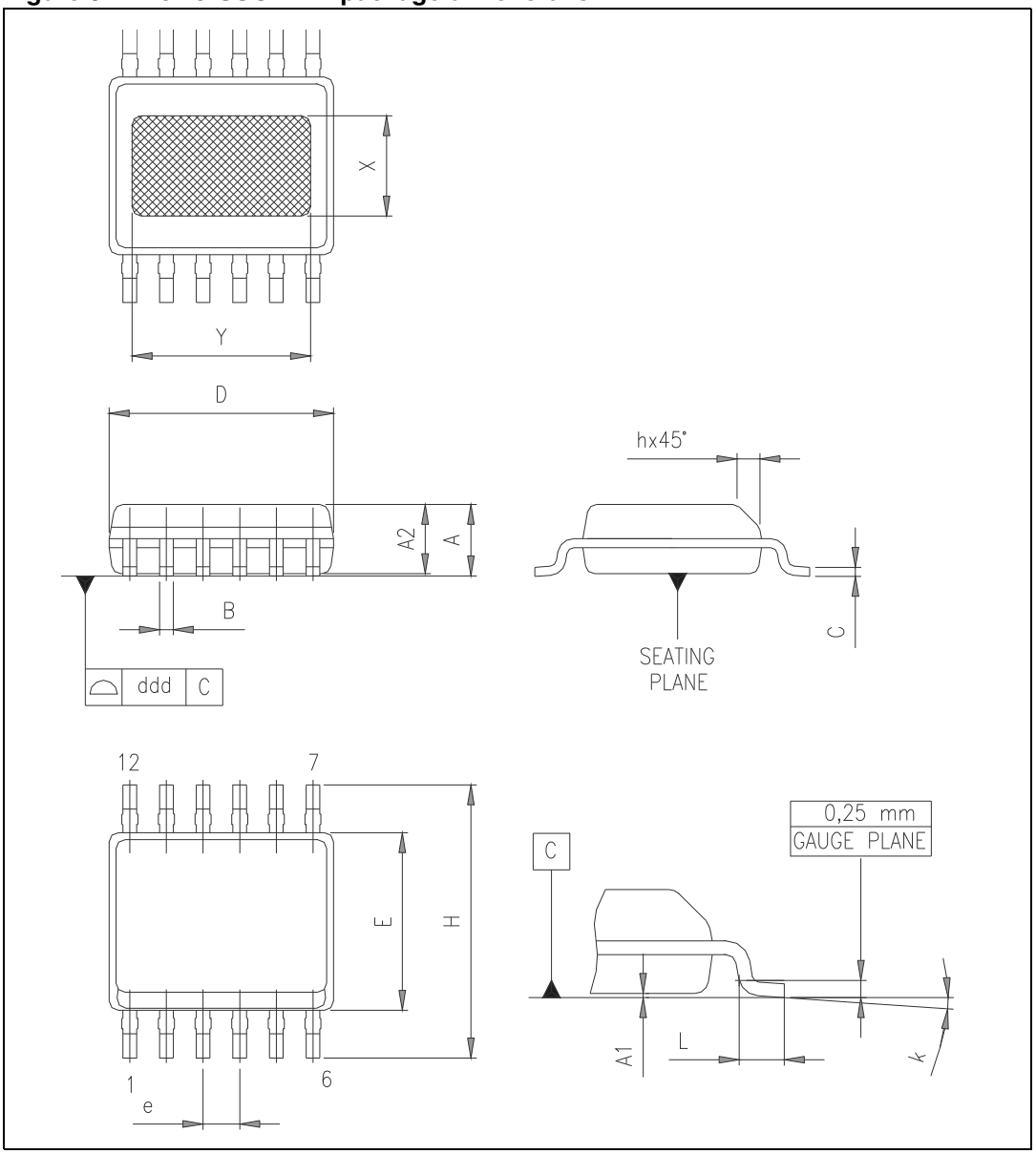
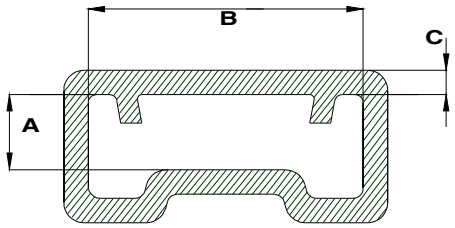


Table 14. PowerSSO-12™ mechanical data

Symbol	Millimeters		
	Min.	Typ.	Max.
A	1.250		1.620
A1	0.000		0.100
A2	1.100		1.650
B	0.230		0.410
C	0.190		0.250
D	4.800		5.000
E	3.800		4.000
e		0.800	
H	5.800		6.200
h	0.250		0.500
L	0.400		1.270
k	0°		8°
X	2.200		2.800
Y	2.900		3.500
ddd			0.100

5.3 Packing information

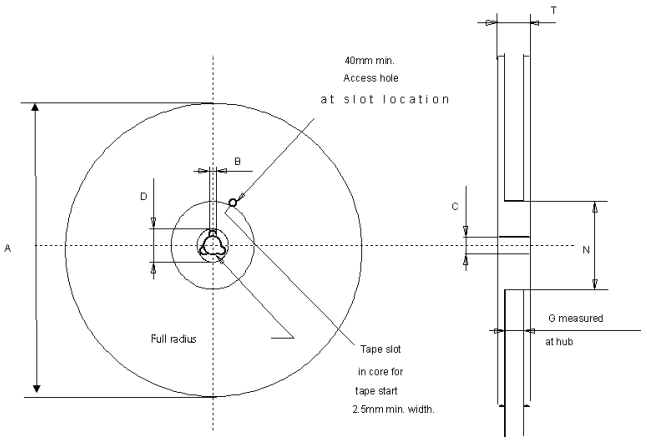
Figure 33. PowerSSO-12™ tube shipment (no suffix)



Base Q.ty	100
Bulk Q.ty	2000
Tube length (± 0.5)	532
A	1.85
B	6.75
C (± 0.1)	0.6

All dimensions are in mm.

Figure 34. PowerSSO-12™ tape and reel shipment (suffix "TR")



REEL DIMENSIONS

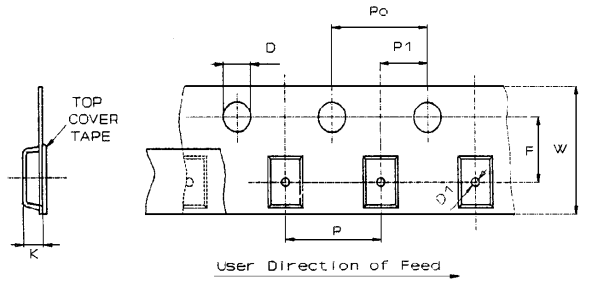
Base Q.ty	2500
Bulk Q.ty	2500
A (max)	330
B (min)	1.5
C (± 0.2)	13
F	20.2
G (+ 2 / -0)	12.4
N (min)	60
T (max)	18.4

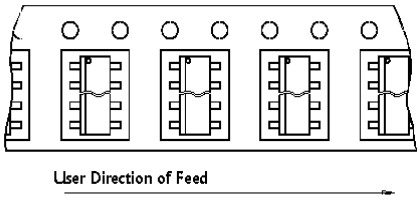
TAPE DIMENSIONS

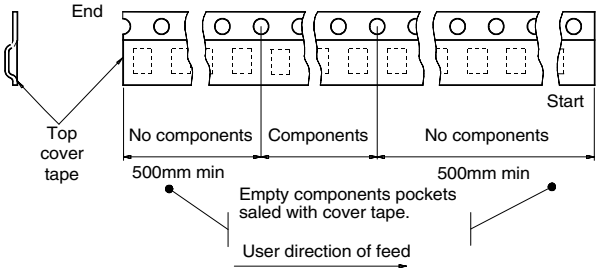
According to Electronic Industries Association (EIA) Standard 481 rev. A, Feb. 1986

Tape width	**W**	12
Tape Hole Spacing	**P0 (± 0.1)**	4
Component Spacing	**P**	8
Hole Diameter	**D (± 0.05)**	1.5
Hole Diameter	**D1 (min)**	1.5
Hole Position	**F (± 0.1)**	5.5
Compartment Depth	**K (max)**	4.5
Hole Spacing	**P1 (± 0.1)**	2

All dimensions are in mm.







6 Revision history

Table 15. Document revision history

Date	Revision	Changes
13-Sep-2004	1	Initial release.
10-Apr-2006	2	Layout changed. Major update to *Section 2: Electrical specifications*.
01-Mar-2007	3	Reformatted. Contents, List of tables and List of figures added. Added *Section 3.4: Maximum demagnetization energy (VCC = 13.5V)*. ECOPACK® package information added.
10-Dec-2007	4	Document reformatted and restructured. Updated *Figure 2: Configuration diagram (top view)* : pins 7-12 left unconnected (N.C) and added note. *Table 4: Absolute maximum ratings* : corrected E_{MAX} value from 14 to 34 mJ. Added *Figure 5: Delay response time between rising edge of ouput current and rising edge of current sense (CS enabled)*. Updated *Figure 6: Iout/ Isense vs. Iout (see Table 10 for details)*. Added *Figure 7: Maximum current sense ratio drift vs load current*. Updated *Table 10: Current sense (8V<VCC<16V)* : – changed $t_{DSENSE2H}$ max value from 300 µs to 150 µs. – added dk1/k1, dk2/k2, dk3/k3, $\Delta t_{DSENSE2H}$, I_{OL} parameters. *Table 12: Electrical transient requirements* : updated test level values III and IV for test pulse 5b and notes. Updated *Section 4.1: PowerSSO-12™ thermal data*: – changed *Figure 29: Rthj-amb vs. PCB copper area in open box free air condition (one channel ON)*. – changed *Figure 30: PowerSSO-12™ thermal impedance junction ambient single pulse (one channel ON)*. – *Figure 31: Thermal fitting model of a double channel HSD in PowerSSO-12™*: added note. – updated *Table 13: Thermal parameters*: R3 value changed from 7 to 3 °C/W. R4 values changed from 10 /10 /9 to 8 /8 /7 °C/W. C3 value changed from 0.05 to 0.0166 W.s/°C.
12-Feb-2008	5	Corrected typing error in *Table 10: Current sense (8V<VCC<16V)* : changed I_{OL} test condition from V_{IN} = 0V to V_{IN} = 5V.
24-Sep-2013	6	Updated disclaimer.

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