

- Protection input (for external OTP and external OVP)
- IC overtemperature protection

3. Applications

- All applications that require an efficient and cost-effective power supply solution up to 75 W.

4. Ordering information

Table 1. Ordering information

Type number	Package		Version
	Name	Description	
TEA1731TS	TSOP6	plastic surface-mounted package; 6 leads	SOT457

5. Block diagram

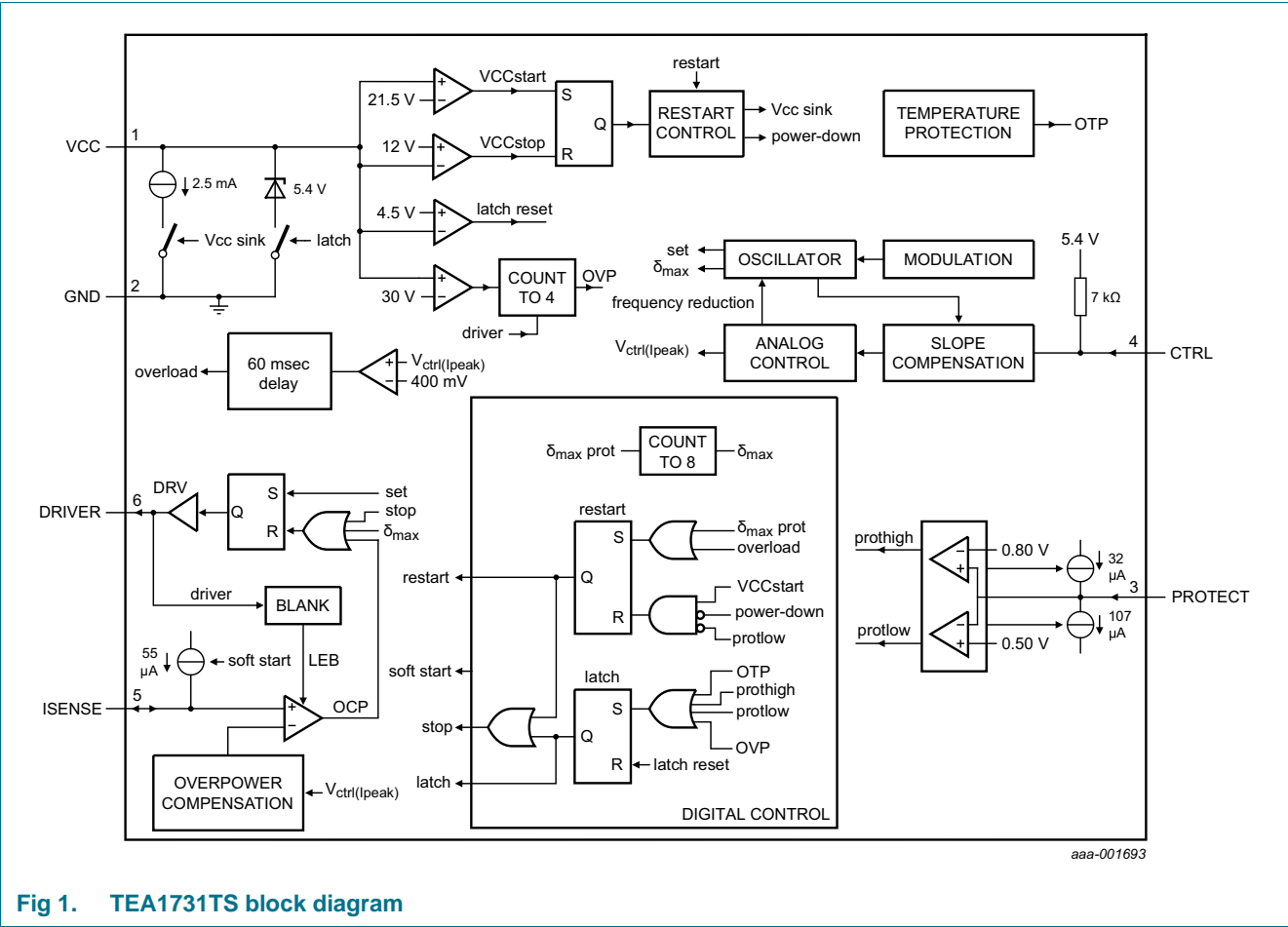
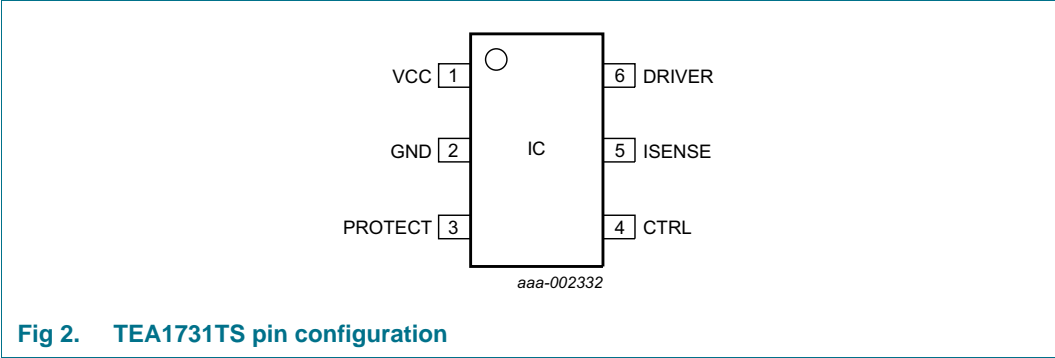


Fig 1. TEA1731TS block diagram

6. Pinning information

6.1 Pinning



6.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
VCC	1	supply voltage
GND	2	ground
PROTECT	3	general-purpose protection input
CTRL	4	control input
ISENSE	5	current sense input
DRIVER	6	gate driver output

7. Functional description

7.1 General control

The TEA1731TS contains a controller for a flyback circuit. A typical configuration is shown in [Figure 3](#).

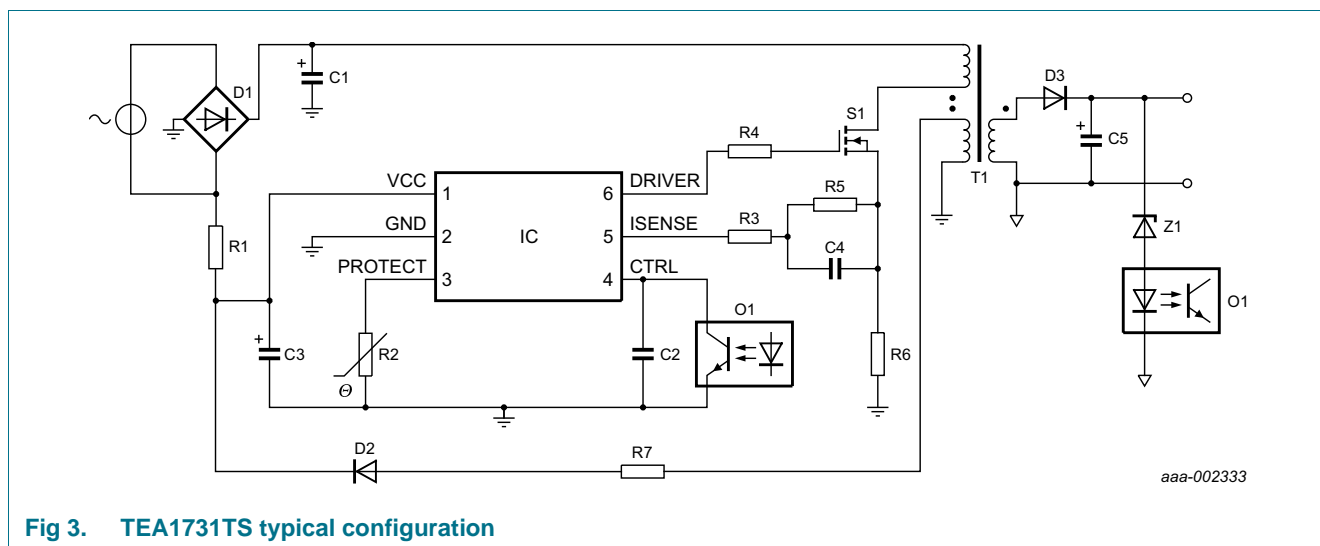


Fig 3. TEA1731TS typical configuration

7.2 Start-up and UnderVoltage LockOut (UVLO)

Initially, the capacitor on the VCC pin, C3, is charged from the high-voltage mains via resistor R1.

As long as VCC is below V_{startup} , the IC current consumption is low (10 μA typical). When VCC reaches V_{startup} , the IC first waits for the PROTECT pin to reach the $V_{\text{det(PROTECT)(L)}}$ voltage. When $V_{\text{det(PROTECT)(L)}}$ is reached, the IC charges the ISENSE pin to the $V_{\text{start(soft)}}$ level and then starts switching. In a typical application, the auxiliary winding of the transformer takes over the supply voltage.

If a protection is triggered, the controller stops switching. Depending on the protection triggered, it either causes a restart or latches the converter to an off-state.

A restart protection disables the switching of the IC. The supply voltage of the IC drops to the UVLO level. When the UVLO level is reached, the IC switches to Power-down mode, where it consumes a low supply current (10 μA typical). The VCC capacitor is recharged via R1 until the VCC start-up level is reached. A delayed restart is performed to lower the input power during a fault condition. Depending on the cause of the restart protection, the restart sequence that discharges and recharges the VCC capacitor is performed once or repeated three times, before switching recommences (See [Figure 4](#)).

When a latched protection is triggered, the TEA1731TS immediately enters Power-down mode. The VCC pin is clamped to a voltage just above the latch protection reset voltage ($V_{\text{rst(latch)}} + 0.9 \text{ V}$).

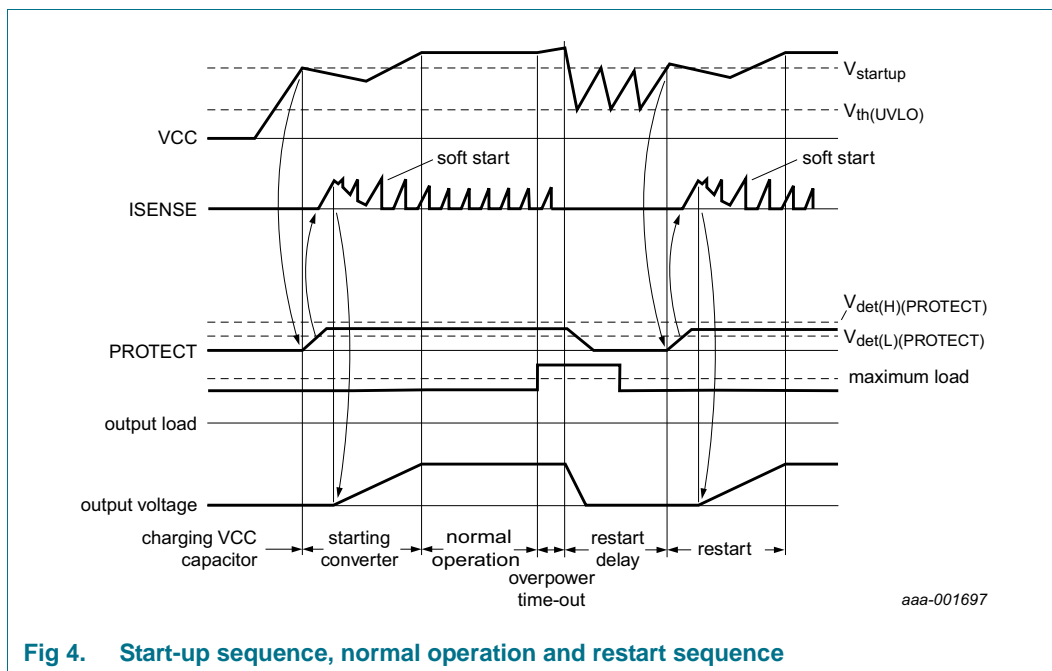


Fig 4. Start-up sequence, normal operation and restart sequence

When the voltage on pin VCC drops below the $V_{th(UVLO)}$ level during normal operation, the controller stops switching. The TEA1731TS waits for the rectified mains to charge the VCC pin using resistor R1.

7.3 Supply management

All internal reference voltages are derived from a temperature compensated on-chip band gap circuit. Internal reference currents are derived from a trimmed and temperature compensated current reference circuit.

7.4 Overvoltage protection (pin VCC)

An OverVoltage Protection (OVP) circuit is connected to the VCC pin. When the V_{CC} exceeds $V_{th(OVP)}$ (30 V typical) for four consecutive switching cycles, the IC triggers the latched protection. When V_{CC} drops below $V_{th(OVP)}$ before count = 4 is reached, the counter is reset to zero.

If a lower over voltage protection level is needed, a Zener diode can be connected between pins VCC and PROTECT.

7.5 Protection input (pin PROTECT)

Pin PROTECT is a general-purpose input pin, which can be used to switch off the converter (latched protection). The converter is stopped when the voltage on this pin is pulled above $V_{det(H)(PROTECT)}$ (0.8 V typical) or below $V_{det(L)(PROTECT)}$ (0.5 V typical) for four consecutive converter strokes. A current of 32 μA (typical) flows out of the chip when the pin voltage is $V_{det(L)(PROTECT)}$. A current of 107 μA (typical) flows into the chip when the pin voltage is $V_{det(H)(PROTECT)}$.

The PROTECT input can be used for creating an (additional) overvoltage detection and an external OverTemperature Protection (OTP) function.

A small capacitor can be connected to the pin if the protections on this pin are not used.

An internal clamp of 4.1 V (typical) protects this pin from excessive voltages.

7.6 Duty cycle control (pin CTRL)

Pin CTRL regulates the output power of the converter. This pin is connected to an internal voltage source of 5.4 V via an internal resistor (typical resistance: 7 k Ω).

The CTRL pin voltage sets the peak current which is measured using the ISENSE pin (see [Section 7.9](#)). At low and medium output power the switching frequency is reduced (see [Section 7.11](#)). The maximum duty cycle is limited to 80 % (typical).

After eight consecutive converter strokes at maximum duty cycle the restart protection is activated. In a restart, the VCC capacitor is quickly discharged to the $V_{th(UVLO)}$ level and recharged to the start-up level from the high-voltage mains, before switching recommences. This occurs when the mains input voltage is removed.

7.7 Slope compensation (pin CTRL)

A slope compensation circuit is integrated for CCM. The slope compensation guarantees stable operation for duty cycles exceeding 50 %.

7.8 Overpower timer

A temporary overload situation is allowed. If $V_{ctrl(I_{peak})}$ (see [Figure 1](#)) set by pin CTRL exceeds 400 mV, an internal timer is started. If the overload situation continues to exist for more than 60 ms (typical), an OverPower Protection (OPP) is triggered (see [Figure 5](#)).

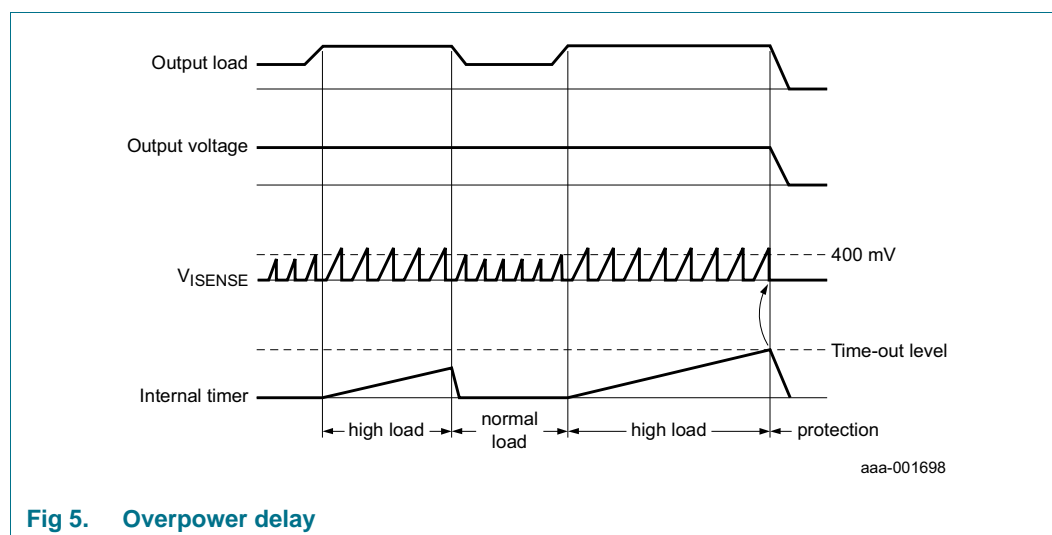


Fig 5. Overpower delay

The TEA1731TS enters the overpower restart mode when the overload time-out is reached. In overpower restart mode, the VCC capacitor is discharged to UVLO level and then charged to the start-up level three times before the converter switches again.

7.9 Current mode control (pin ISENSE)

Current mode control is used because it ensures a good line regulation.

Pin ISENSE senses the primary current across external resistor R6 and compares it with an internal control voltage. The internal control voltage is proportional to the CTRL pin voltage (see [Figure 6](#)).

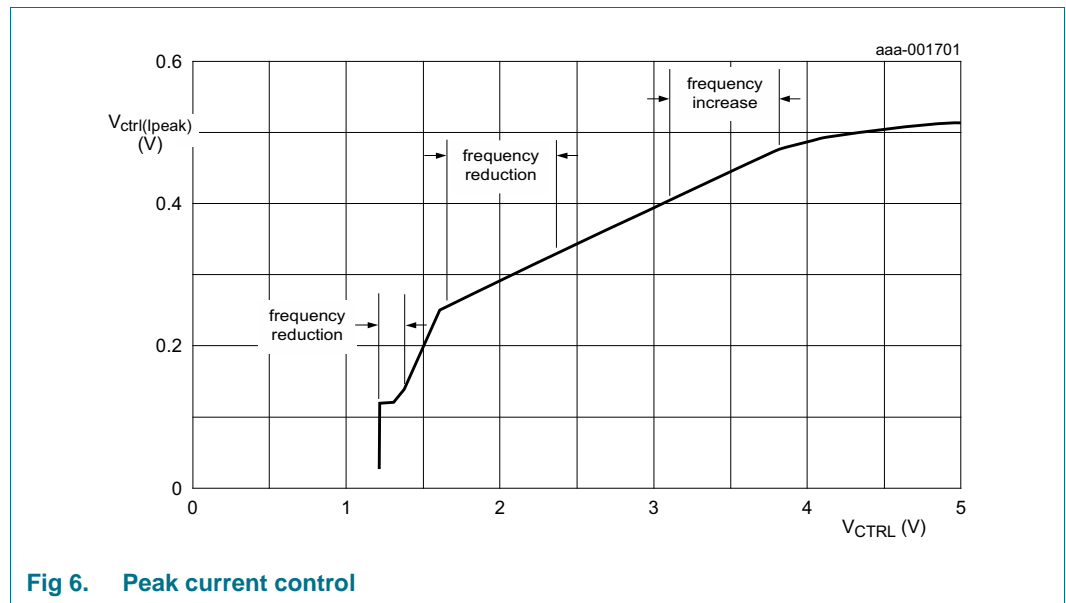


Fig 6. Peak current control

Leading edge blanking prevents false triggering due to capacitive discharge when switching on the external power switch (see [Figure 7](#)).

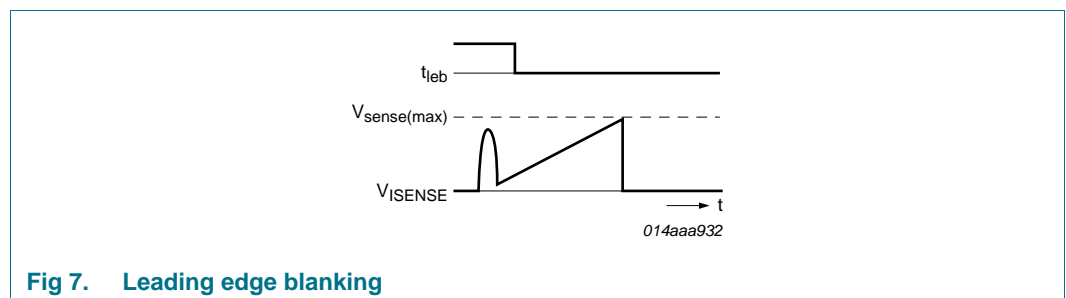


Fig 7. Leading edge blanking

7.10 Soft start-up (pin ISENSE)

A soft start is made to prevent audible noise during start-up or restart. Before the converter starts, soft start capacitor C4 on the ISENSE pin is charged. When the converter starts switching, the primary peak current slowly increases when the soft start capacitor discharges through the soft start resistor (R5, see [Figure 3](#)).

The soft start capacitor (C4) and resistor (R5) values chosen set the soft start time constant.

7.11 Peak power, high-power, medium power and low-power operation

During high-power operation, with the converter running at a 65 kHz (typical) fixed frequency, the power is controlled by varying the peak current. A peak power mode is implemented to supply a short overload situation. In peak power mode, both frequency and peak current are increased.

At reduced power levels, the converter enters the medium power mode where the peak current is reduced. The switching losses are reduced by lowering the switching frequency to 27.5 kHz (typical).

When the power is further reduced to low power, a second frequency reduction is made. In low-power operation, the switching frequency of the converter is reduced while the peak current is set to 25 % of the maximum peak current (see [Figure 6](#) and [Figure 8](#)).

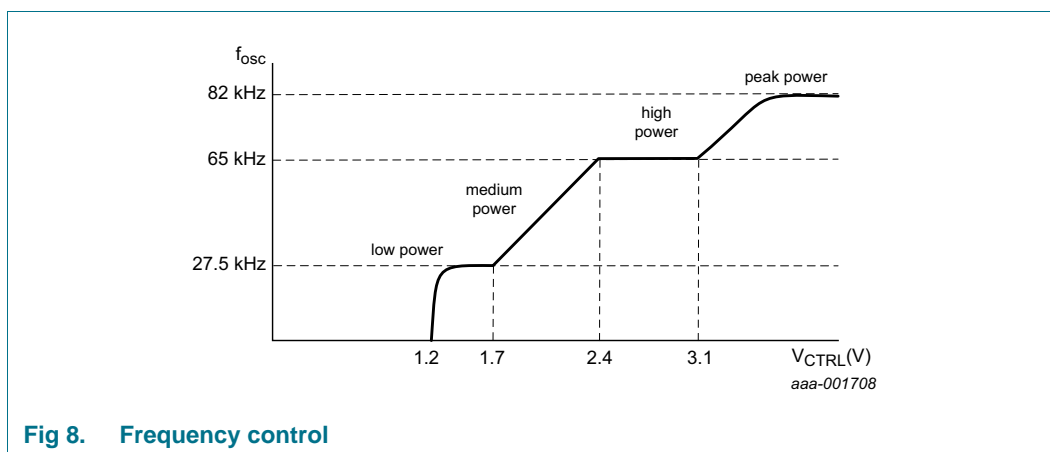


Fig 8. Frequency control

7.12 Overpower or high/low line compensation

Overpower compensation is built in to compensate for high/low line. The maximum continuous output power and the maximum peak power are about constant over the full mains input voltage range (see [Figure 9](#)). The rectified mains input voltage is measured by sensing the slope of the primary current from pin ISENSE. The slope information is then used to adjust the primary current by subtracting an offset $V_{(sense)offset}$ from the internal control voltage $V_{ctrl(lpeak)}$ cycle-by-cycle (NXP patent: 81421271EP01).

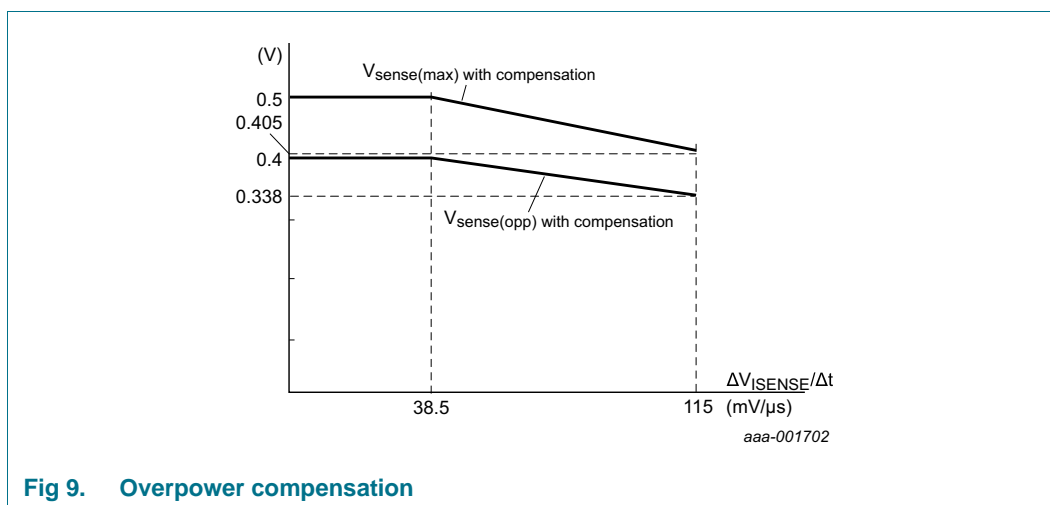


Fig 9. Overpower compensation

7.13 Driver (pin DRIVER)

The driver circuit to the gate of the power MOSFET has a current sourcing capability of typically 300 mA and a current sink capability of typically 750 mA. This enables a fast turn-on and turn-off of the power MOSFET for efficient operation.

7.14 OverTemperature Protection (OTP)

Integrated overtemperature protection ensures that the IC stops switching if the junction temperature exceeds the thermal shutdown limit.

OTP is a latched protection. It can be reset by removing the voltage on pin VCC.

8. Limiting values

Table 3. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
Voltages					
V _{CC}	supply voltage	continuous	−0.4	+30	V
		t < 100 ms	-	35	V
V _{PROTECT}	voltage on pin PROTECT	current limited	−0.4	+5	V
V _{CTRL}	voltage on pin CTRL		−0.4	+5.5	V
V _{ISENSE}	voltage on pin ISENSE	current limited	−0.4	+5	V
Currents					
I _{VCC}	current on pin VCC	δ < 10 %	-	0.4	A
I _{I(PROTECT)}	input current on pin PROTECT		−1	+1	mA
I _{CTRL}	current on pin CTRL		−3	0	mA
I _{ISENSE}	current on pin ISENSE		−10	+1	mA
I _{DRIVER}	current on pin DRIVER	δ < 10 %	−0.4	+1	A
General					
P _{tot}	total power dissipation	T _{amb} < 75 °C	-	0.29	W
T _{stg}	storage temperature		−55	+150	°C
T _j	junction temperature		−40	+150	°C
ESD					
V _{ESD}	electrostatic discharge voltage	class 1			
		human body model	[1] -	4000	V
		changed device model	-	750	V

[1] Equivalent to discharging a 100 pF capacitor through a 1.5 kΩ series resistor.

9. Thermal characteristics

Table 4. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
R _{th(j-a)}	thermal resistance from junction to ambient	in free air; single layer JEDEC test board	259	K/W
R _{th(j-c)}	thermal resistance from junction to case	in free air; JEDEC test board	152	K/W

10. Characteristics

Table 5. Characteristics

$T_{amb} = 25\text{ }^{\circ}\text{C}$; $V_{CC} = 20\text{ V}$; all voltages are measured with respect to ground (pin 2); currents are positive when flowing into the IC; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Supply voltage management (pin VCC)						
$V_{startup}$	start-up voltage		19.3	21.5	23.8	V
$V_{th(UVLO)}$	undervoltage lockout threshold voltage		11.2	12.5	13.8	V
$V_{th(ovp)}$	overvoltage protection threshold voltage		29	30	31	V
$N_{cy(ovp)}$	number of overvoltage protection cycles		-	4	-	
$V_{clamp(VCC)}$	clamp voltage on pin VCC	activated during latched protection; $I_{CC} = 100\text{ }\mu\text{A}$	-	$V_{rst(latch)} + 0.9$	-	V
		activated during latched protection, $I_{CC} = 1\text{ mA}$	-	-	$V_{rst(latch)} + 3.5$	V
$I_{CC(restart)}$	restart supply current		1	2.5	-	mA
V_{hys}	hysteresis voltage	$V_{startup} - V_{th(UVLO)}$	6.6	9.1	11.6	V
$I_{CC(startup)}$	start-up supply current	$V_{CC} < V_{startup}$	5	10	15	μA
$I_{CC(oper)}$	operating supply current	no-load on pin DRIVER; $\delta = 2\text{ }%$; excluding optocurrent	-	0.58	-	mA
		no-load on pin DRIVER; $\delta = 25\text{ }%$; excluding optocurrent	-	0.62	-	mA
$V_{rst(latch)}$	latched reset voltage		3.5	4.5	5.5	V
Protection input (pin PROTECT)						
$V_{det(L)(PROTECT)}$	LOW-level detection voltage on pin PROTECT		0.47	0.50	0.53	V
$V_{det(H)(PROTECT)}$	HIGH-level detection voltage on pin PROTECT		0.75	0.8	0.85	V
$I_{O(PROTECT)}$	output current on pin PROTECT	$V_{PROTECT} = V_{low(PROTECT)}$	-34	-32	-30	μA
		$V_{PROTECT} = V_{high(PROTECT)}$	87	107	127	μA
$V_{clamp(PROTECT)}$	clamp voltage on pin PROTECT	$I_{I(PROTECT)} = 200\text{ }\mu\text{A}$	[1] 3.5	4.1	4.7	V
Peak current control (pin CTRL)						
V_{CTRL}	voltage on pin CTRL	for minimum flyback peak current	1	1.3	1.6	V
$R_{int(CTRL)}$	internal resistance on pin CTRL		5	7	9	$\text{k}\Omega$
$I_{O(CTRL)}$	output current on pin CTRL	$V_{CTRL} = 1.4\text{ V}$	-0.7	-0.5	-0.3	mA

Table 5. Characteristics ...continued

$T_{amb} = 25\text{ }^{\circ}\text{C}$; $V_{CC} = 20\text{ V}$; all voltages are measured with respect to ground (pin 2); currents are positive when flowing into the IC; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Pulse width modulator						
f_{osc}	oscillator frequency	peak power	75	82	89	kHz
		high power	60.5	65	69.5	kHz
		medium power	24	27.5	31	kHz
f_{mod}	modulation frequency		210	280	350	Hz
Δf_{mod}	modulation frequency variation	high power	± 3	± 4	± 5	kHz
δ_{max}	maximum duty cycle		-	80	-	%
$N_{cy(dmax)}$	number of switching cycles with maximum duty cycle		-	8	-	
$V_{start(red)f}$	frequency reduction start voltage	pin CTRL dropping to low power	1.1	1.4	1.7	V
$V_{\delta(zero)}$	zero duty cycle voltage	pin CTRL	0.9	1.2	1.5	V
Overpower protection						
$t_{to(opp)}$	overpower protection time-out time		-	60	-	ms
Current sense and overpower compensation (pin ISENSE)						
$V_{sense(max)}$	maximum sense voltage	$\Delta V/\Delta t = 0\text{ V/s}$	0.47	0.50	0.53	V
$t_{PD(sense)}$	sense propagation delay		-	146	-	ns
$V_{th(sense)opp}$	overpower protection sense threshold voltage		370	400	430	mV
$V_{offset(opc)}$	overpower compensation offset voltage	$V_{sense} = 400\text{ mV}$; $\Delta V/\Delta t = 115\text{ mV}/\mu\text{s}$	38	62	86	mV
		$V_{sense} = 500\text{ mV}$; $\Delta V/\Delta t = 115\text{ mV}/\mu\text{s}$	60	95	130	mV
$\Delta V_{ISENSE}/\Delta t$	slope compensation voltage on pin ISENSE	high-power mode	-	20	-	mV/ μs
t_{leb}	leading edge blanking time		275	325	375	ns
Soft start (pin ISENSE)						
$I_{start(soft)}$	soft start current		-63	-55	-47	μA
$V_{start(soft)}$	soft start voltage	$V_{CTRL} = 4\text{ V}$; enable voltage	-	$V_{sense(max)}$	-	V
$R_{start(soft)}$	soft start resistance		12	-	-	k Ω

Table 5. Characteristics ...continued

$T_{amb} = 25\text{ }^{\circ}\text{C}$; $V_{CC} = 20\text{ V}$; all voltages are measured with respect to ground (pin 2); currents are positive when flowing into the IC; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Driver (pin DRIVER)						
$I_{source(DRIVER)}$	source current on pin DRIVER	$V_{DRIVER} = 2\text{ V}$	-	-0.3	-0.25	A
$I_{sink(DRIVER)}$	sink current on pin DRIVER	$V_{DRIVER} = 2\text{ V}$	0.25	0.3	-	A
		$V_{DRIVER} = 10\text{ V}$	0.6	0.75	-	A
$V_{O(DRIVER)max}$	maximum output voltage on pin DRIVER		9	10.5	12	V
Temperature protection						
$T_{pl(IC)}$	IC protection level temperature		130	140	150	$^{\circ}\text{C}$

[1] The clamp voltage on the PROTECT pin is lowered when the IC is in Power-down mode. (latched or restart protection)

11. Application information

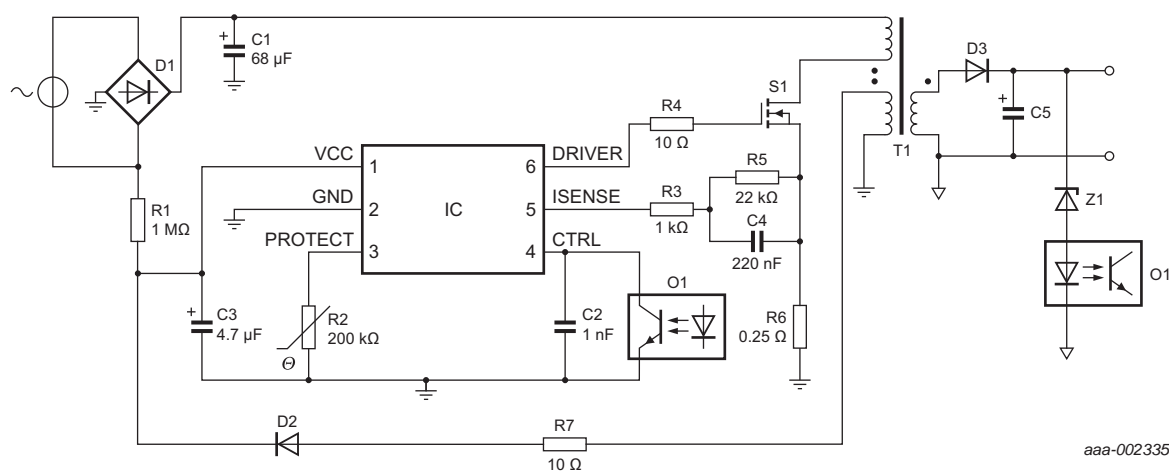
A power supply with the TEA1731TS is a flyback converter operating in continuous conduction mode. See [Figure 10](#).

Capacitor C3 buffers the IC supply voltage, which is powered via resistor R1 for start-up and via the auxiliary winding during normal operation. Sense resistor R6 converts the current through MOSFET S1 into a voltage on pin ISENSE. The value of resistor R6 defines the maximum primary peak current through MOSFET S1. Resistor R7 reduces the peak current to capacitor C3.

Resistor R5 and capacitor C4 define the soft start time. Resistor R3 is added to prevent that soft start capacitor C4 is charged during normal operation due to negative voltage spikes across current sense resistor R6.

Capacitor C2 is added to reduce noise on the CTRL pin.

Resistor R4 is required to limit the current spikes to pin DRIVER because of parasitic inductance of current sense resistor R6. Resistor R4 also dampens possible oscillations of MOSFET S1. Adding a bead on the gate pin of MOSFET S1 can be required to prevent local oscillations of the MOSFET.



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Fig 10. TEA1731TS application diagram

12. Package outline

Plastic surface-mounted package (TSOP6); 6 leads

SOT457

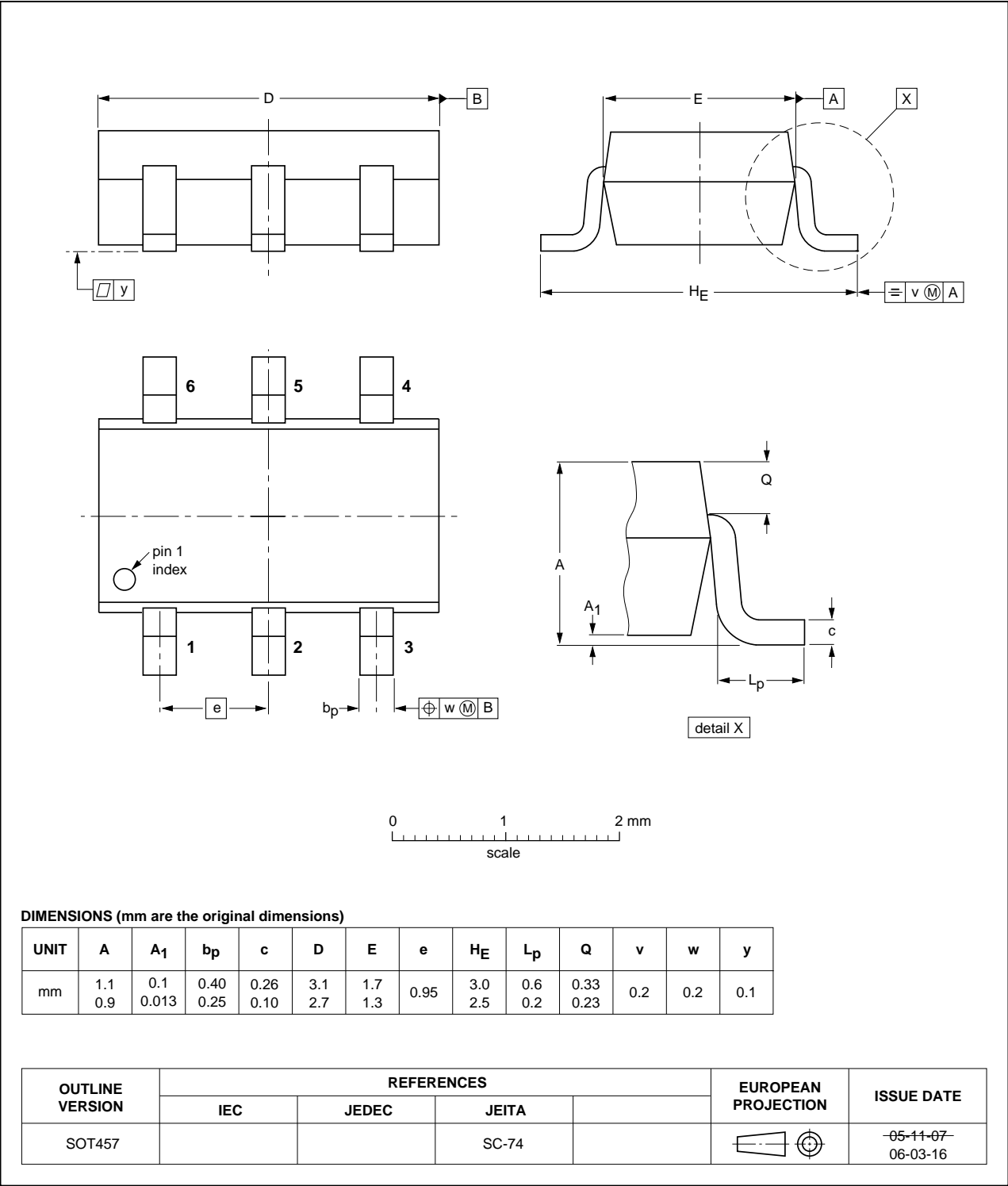


Fig 11. SOT457 (TSOP6)

13. Revision history

Table 6. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
TEA1731TS v.2.1	20120816	Product data sheet	-	TEA1731TS v.2
Modifications:	• R4 value changed in Figure 10 "TEA1731TS application diagram" has been updated.			
TEA1731TS v.2	20120731	Product data sheet	-	TEA1731TS v.1
TEA1731TS v.1	20120215	Objective data sheet	-	-

14. Legal information

14.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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16. Contents

1	General description	1
2	Features and benefits	1
3	Applications	2
4	Ordering information	2
5	Block diagram	2
6	Pinning information	3
6.1	Pinning	3
6.2	Pin description	3
7	Functional description	4
7.1	General control	4
7.2	Start-up and UnderVoltage LockOut (UVLO) ..	4
7.3	Supply management	5
7.4	Overvoltage protection (pin VCC)	5
7.5	Protection input (pin PROTECT)	5
7.6	Duty cycle control (pin CTRL)	6
7.7	Slope compensation (pin CTRL)	6
7.8	Overpower timer	6
7.9	Current mode control (pin ISENSE)	7
7.10	Soft start-up (pin ISENSE)	7
7.11	Peak power, high-power, medium power and low-power operation	8
7.12	Overpower or high/low line compensation ...	8
7.13	Driver (pin DRIVER)	9
7.14	OverTemperature Protection (OTP)	9
8	Limiting values	10
9	Thermal characteristics	10
10	Characteristics	11
11	Application information	14
12	Package outline	15
13	Revision history	16
14	Legal information	17
14.1	Data sheet status	17
14.2	Definitions	17
14.3	Disclaimers	17
14.4	Trademarks	18
15	Contact information	18
16	Contents	19

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Date of release: 16 August 2012

Document identifier: TEA1731TS