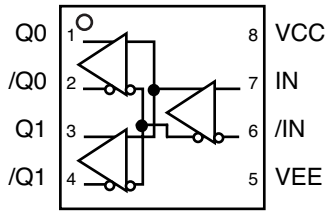
PACKAGE/ORDERING INFORMATION



8-Pin MLF®
Ultra-Small Outline (2mm × 2mm)

Ordering Information

Part Number	Package Type	Operating Range	Package Marking	Lead Finish
SY89311UMITR	MLF-8	Industrial	311	Sn-Pb
SY89311UMGTR(1)	MLF-8	Industrial	311 with Pb-Free bar-line indicator	Pb-Free NiPdAu

Note:

1. Pb-Free package is recommended for new designs.

PIN DESCRIPTION

Pin Number	Pin Name	Type	Pin Function
1, 2, 3, 4	Q0, /Q0, Q1, /Q1	100K Output	Differential PECL/ECL Outputs: Default to LOW if IN inputs are left open. See“Output Interface Applications” section for recommendations on terminations. Unused output pairs may be left floating without any inpact on skew or jitter.
5	VEE, Exposed Pad	Negative Power Supply	Negative Power Supply: V_{EE} and exposed pad must be tied to most negative supply. For PECL/LVPECL connect to ground.
6	/IN	100K Input	Differential PECL/ECL Input: Internal 75kΩ pull-up and pull-down resistors. If left floating, pin defaults to $V_{CC}/2$. When not used, this input can be left open. See “Input Interface Applications” section for single-ended inputs.
7	IN	100K Input	Differential PECL/ECL Input: Internal 75kΩ pull-down resistor. If left open, pin defaults LOW. Q output will be LOW. Accepts differential 10K and 100K ECL/PECL. See “Input Interface Applications” section for single-ended inputs.
8	VCC	Positive Power Supply	Positive Power Supply: Bypass with 0.1μF//0.01μF low ESR capacitors.

Absolute Maximum Ratings[1]

Supply Voltage (V_{CC}) ..... –0.5V to +6.0V
Input Voltage (V_{IN}) ..... –0.5V to V_{CC}
LVPECL Output Current (I_{OUT})
  Continuous 50mA
  Surge 100mA
Input Current
  Source or sink current on IN, /IN ..... ±50mA
Lead Temperature (soldering, 20 sec.) ..... +260°C
Storage Temperature (T_S) ..... –65°C to +150°C

Operating Ratings[2]

Supply Voltage $|V_{CC}–V_{EE}|$ ..... +2.375V to +2.625V
  ..... +3.0V to +3.6V
  ..... +4.5V to +5.5V
Ambient Temperature (T_A) ..... –40°C to +85°C
Package Thermal Resistance, **Note 3**
MLF™ (θ_{JA})
  Still-Air ..... 93°C/W
  500lfpm ..... 87°C/W
MLF™ (Ψ_{JB})
  Junction-to-Board ..... 60°C/W

DC ELECTRICAL CHARACTERISTICS[4]

T_A = –40°C to +85°C

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{CC}	Power Supply Voltage	LVPECL LVPECL PECL ECL LVECL LVECL	2.375 3.0 4.5 –5.5 –3.6 –2.625	2.5 3.3 5.0 –5.0 –3.3 –2.5	2.625 3.6 5.5 –4.5 –3.0 –2.375	V V V V V V
I_{EE}	Power Supply Current	Max. V_{CC}, no load		30	44	mA
I_{IH}	Input HIGH Current	$V_{IN} = V_{IH}$			150	µA
I_{IL}	Input LOW Current IN /IN	$V_{IN} = V_{IL}$ $V_{IN} = V_{IL}$	0.5 –150			µA µA
C_{IN}	Input Capacitance			1.0		pF

(100K) ECL/LVECL DC ELECTRICAL CHARACTERISTICS

V_{CC} = +2.5V ±5% or +3.3V ±10% or +5.0V ±10% and V_{EE} = 0V; V_{CC} = 0V and V_{EE} = –2.5V ±5% or –3.3V ±10% or –5.0V ±10%; R_L = 50Ω to V_{CC}–2V; T_A = –40°C to +85°C, unless otherwise noted.

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{OH}	Output HIGH Voltage		V_{CC}–1.145		V_{CC}–0.895	V
V_{OL}	Output LOW Voltage		V_{CC}–1.945		V_{CC}–1.695	V
V_{IH}	Input HIGH Voltage		V_{CC}–1.225		V_{CC}–0.88	V
V_{IL}	Input LOW Voltage		V_{CC}–1.945		V_{CC}–1.625	V
V_{IHCMR}	Input HIGH Voltage Common Mode Range	**Note 5**	V_{EE}+1.2		V_{CC}	V
I_{IH}	Input HIGH Current	$V_{IN} = V_{IH}$			150	µA
I_{IL}	Input LOW Current (IN)	$V_{IN} = V_{IL}$	0.5			µA
	Input LOW Current (/IN)	$V_{IN} = V_{IL}$	–150			µA

Notes:

1. Permanent device damage may occur if absolute maximum ratings are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data sheet. Exposure to absolute maximum ratlng conditions for extended periods may affect device reliability.
2. The data sheet limits are not guaranteed if the device is operated beyond the operating ratings.
3. Package Thermal Resistance values assume exposed pad is soldered (or equivalent) to the device's most negative potential on the PCB.
4. This circuit is designed to meet the DC specifications shown in the above table after thermal equilibrium has been established.
5. V_{IHCMR} (min) varies 1:1 with V_{EE}, (max) varies 1:1 with V_{CC}.

AC ELECTRICAL CHARACTERISTICS[6]

V_{CC} = +2.5V ±5% or +3.3V ±10% or +5.0V ±10% and V_{EE} = 0V; V_{CC} = 0V and V_{EE} = –2.5V ±5% or –3.3V ±10% or or –5.0V ±10%; R_L = 50Ω to V_{CC}–2V; T_A = –40°C to +85°C, unless otherwise noted.

Symbol	Parameter	Condition	Min	Typ	Max	Units
f_{MAX}	Maximum Toggle Frequency		3			GHz
t_{pd}	Propagation Delay (Differential) IN to Q, /Q IN to Q, /Q	 V_{CC} = 3.3V/5V V_{CC} = 2.5V	 140 170	 220 240	 300 360	 ps ps
t_{SKEW}	Within-Device Skew Q, /Q	**Note 7**		5	20	ps
	Part-to-Part Skew	V_{CC} = 3.3V/5V, **Note 7** V_{CC} = 2.5V, **Note 7**			150 120	ps ps
t_{JITTER}	Cycle-to-Cycle Jitter (rms)				1	$ps_{(rms)}$
V_{DIFF}	Input Swing	**Note 8**	150	800	1200	mV
t_r, t_f	Output Rise/Fall Time (20% to 80%)		70	120	200	ps

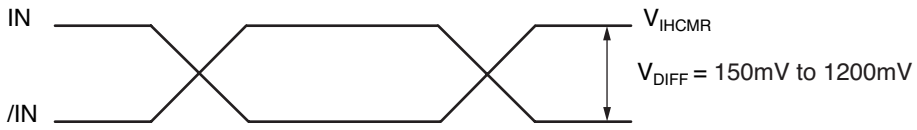
Notes:

6. Measured with 750mV input signal, 50% duty cycle. V_{DIFF_OUT} is ≥ 400mV.

7. Skew is measured between outputs under identical transitions. Duty cycle skew is defined only for differential operation when the delays are measured from the cross point of the inputs to the cross point of the outputs.

8. See “Input Waveform.”

INPUT WAVEFORM



INPUT INTERFACE APPLICATIONS

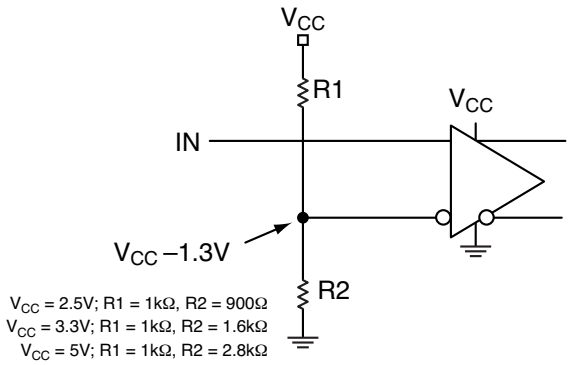


Figure 1. Single-Ended Input (Terminating unused input)

LVPECL OUTPUT INTERFACE APPLICATIONS

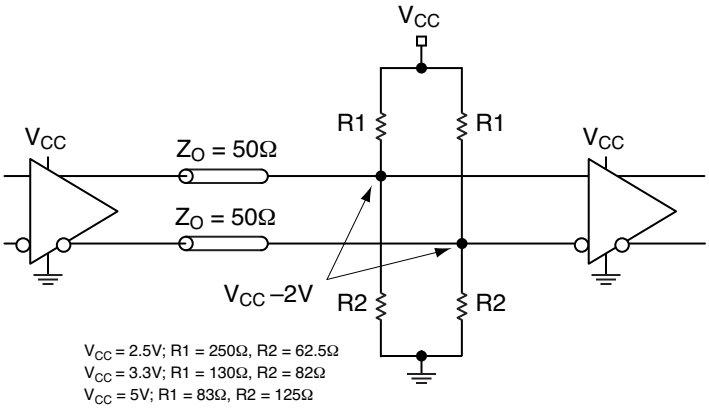


Figure 2a. Parallel Thevenin-Equivalent Termination

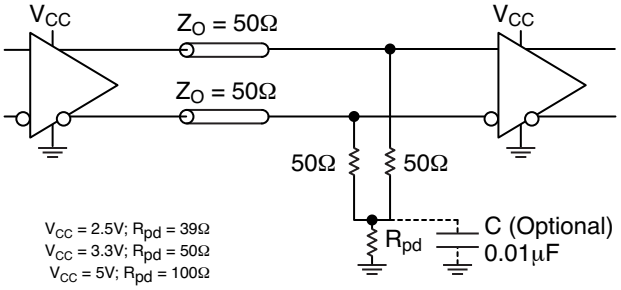


Figure 2b. Three Resistor "Y Termination"

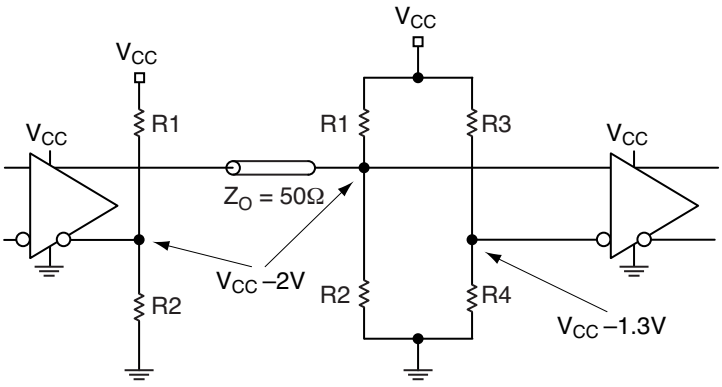
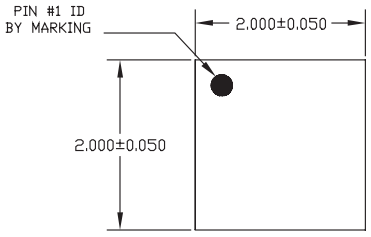
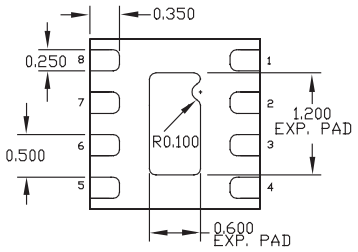


Figure 2c. Terminating Unused I/O

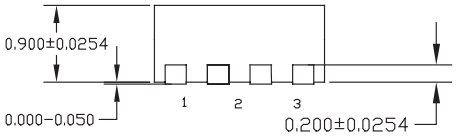
8 LEAD ULTRA-SMALL EPAD-MicroLeadFrame® (MLF-8)



TOP VIEW

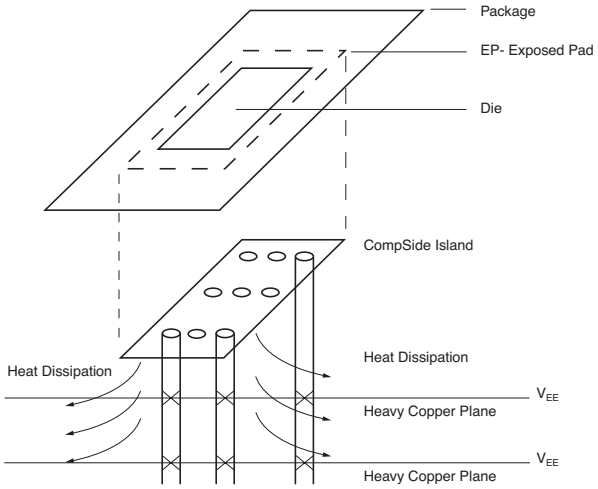


BOTTOM VIEW



SIDE VIEW

NOTE:
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. MAX. PACKAGE WARPAGE IS 0.05 mm.
3. MAXIMUM ALLOWABE BURRS IS 0.076 mm IN ALL DIRECTIONS.
4. PIN #1 ID ON TOP WILL BE LASER/INK MARKED.



PCB Thermal Consideration for 8-Pin MLF® Package

Package Notes:

1. Package meets Level 2 qualification.
2. All parts are dry-packaged before shipment.
3. Exposed pads must be soldered to a ground for proper thermal management.

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