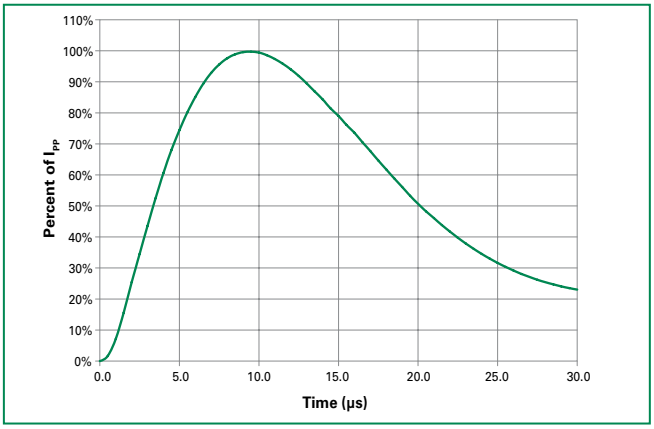
Electrical Characteristics (T_{OP} = 25°C)

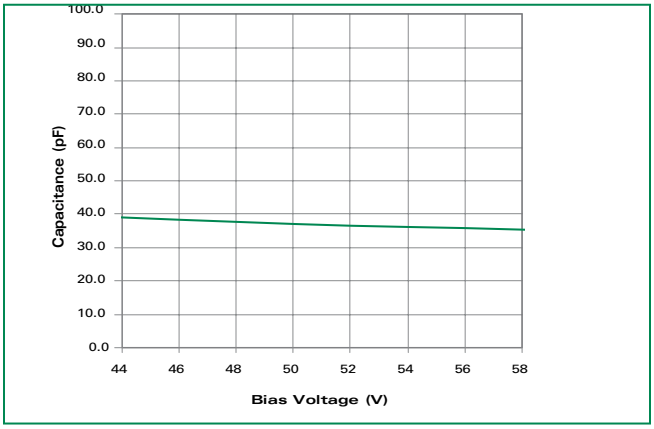
Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Leakage Current	I_{RM}	25°C, V_{PoE}= 58V	-	-	0.1	µA
		85°C, V_{PoE}= 58V [1]	-	-	1	µA
Breakdown Voltage	V_{BR}	I_R= 1mA	64	67	-	V
Clamping Voltage [2]	V_C	I_{PP}= 24A, t_p=8/20 µs	-	-	96	V
Dynamic Resistance [2]	R_{DYN}	TLP, t_p=100ns, I/O to GND [2]	-	0.35	-	Ω
Capacitance [1]	C	V_{PoE}= 58V	-	35	-	pF

Notes: 1 Parameter is guaranteed by design and/or component characterization.
2. Transmission Line Pulse (TLP) with 100ns width, 2ns rise time, and average window t1=70ns to t2= 90ns

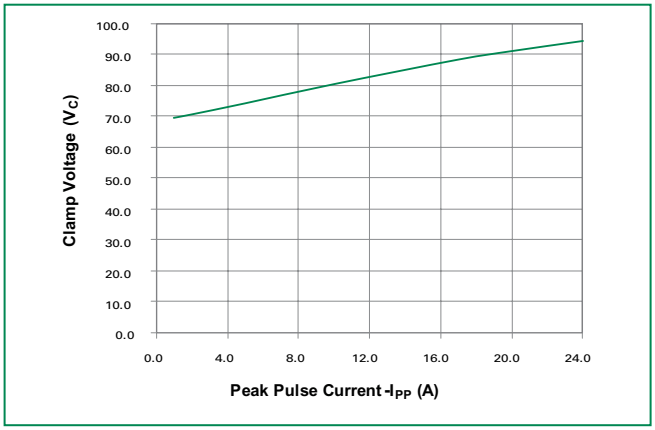
8/20µS Pulse Waveform



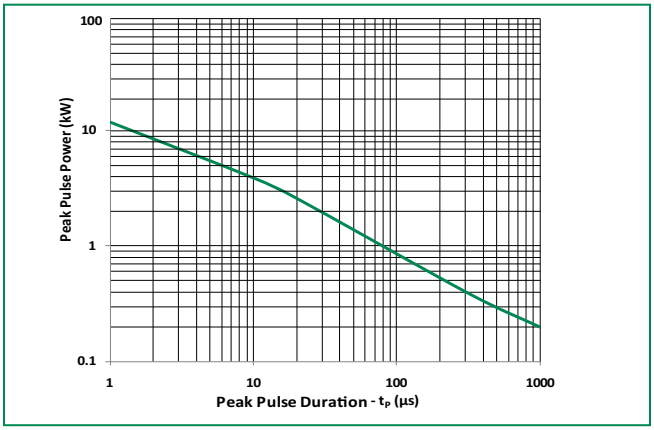
Capacitance vs. Reverse Bias



Clamping Voltage vs I_{PP}

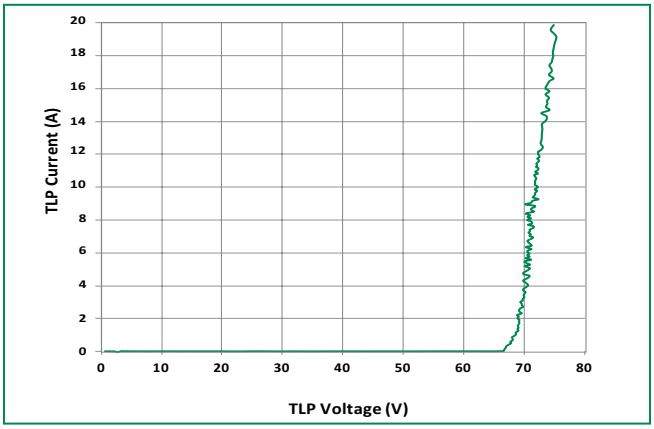


Non-Repetitive Peak Pulse Power vs. Pulse Time



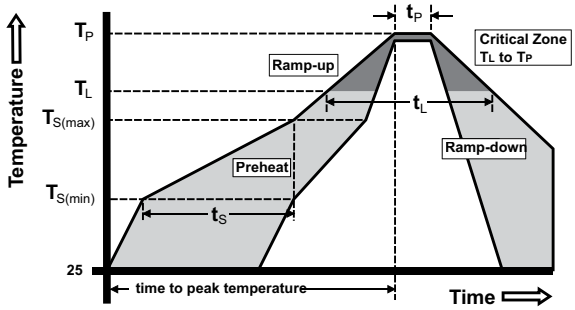
Revision: 01/08/19

Transmission Line Pulse (TLP)



Soldering Parameters

Reflow Condition		Pb – Free assembly
Pre Heat	**- Temperature Min ($T_{s(min)}$)**	150°C
	- Temperature Max ($T_{s(max)}$)	200°C
	- Time (min to max) (t_s)	60 – 180 secs
Average ramp up rate (Liquidus) Temp (T_L) to peak		3°C/second max
$T_{S(max)}$ to T_L - Ramp-up Rate		3°C/second max
Reflow	**- Temperature (T_L) (Liquidus)**	217°C
	- Temperature (t_L)	60 – 150 seconds
Peak Temperature (T_P)		$260^{+0/-5}$ °C
Time within 5°C of actual peak Temperature (t_p)		20 – 40 seconds
Ramp-down Rate		6°C/second max
Time 25°C to peak Temperature (T_P)		8 minutes Max.
Do not exceed		260°C



Product Characteristics

Lead Plating	Tin
Lead Material	Alloy 42
Lead Coplanarity	0.0004 inches (0.102mm)
Substrate Material	Silicon
Body Material	Molded Compound
Flammability	UL Recognized compound meeting flammability rating V-0

Revision: 01/08/19

Application Schematic

Figure 1: Typical application circuit with fully integrated PSE controller

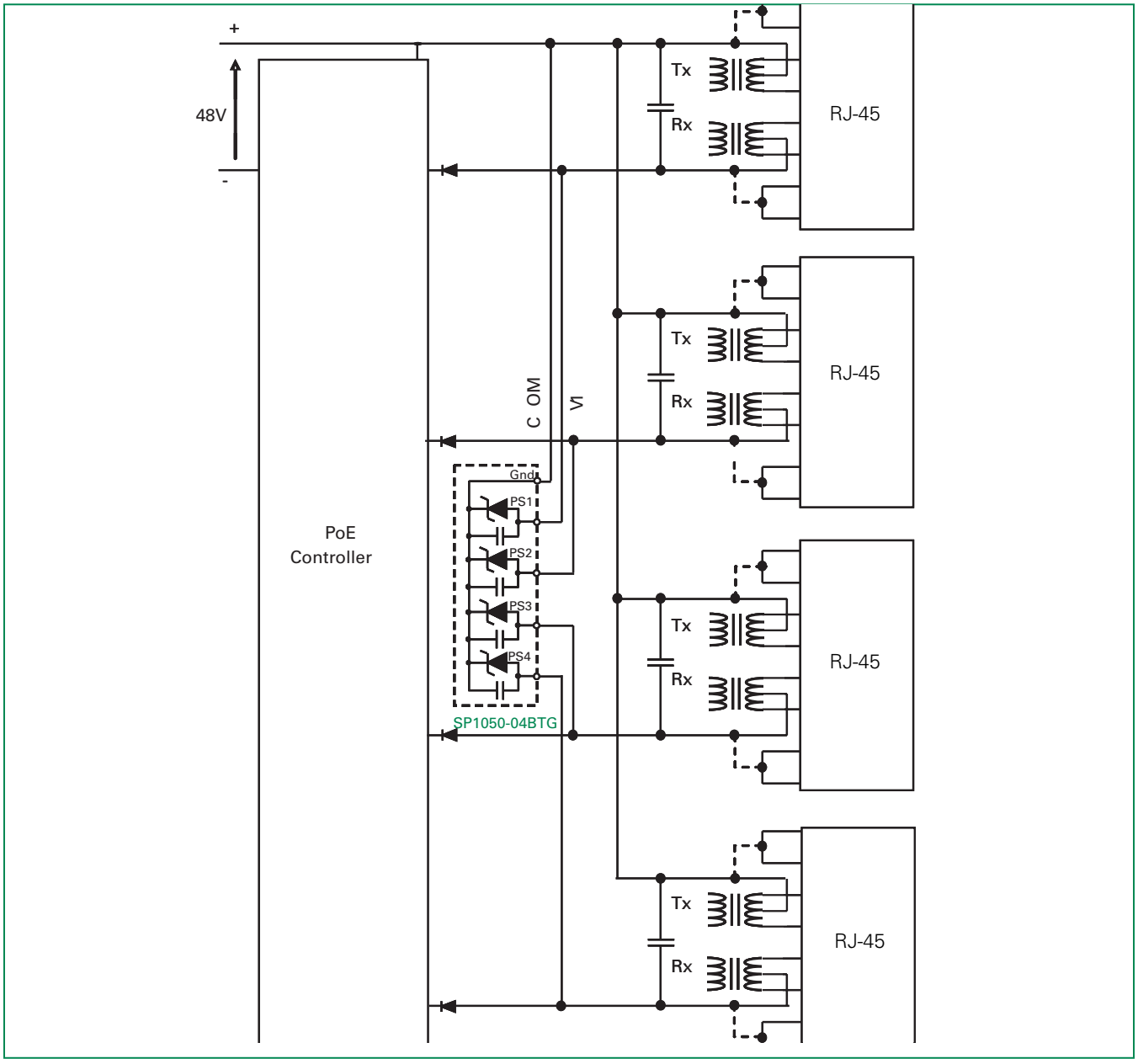
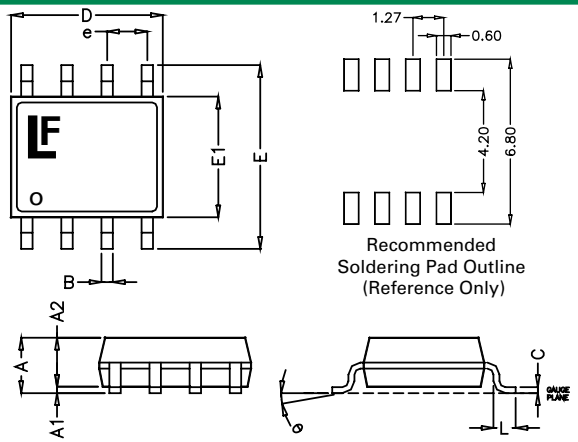


Figure 1 shows typical application of power sourcing equipment (PSE) allowing communication and power sourcing for several powered devices (PD). The SP1050-04BTG is optimized for space savings as there is generally a multiple of 4 present. This protection component complies with IEEE 802.3af and IEEE 802.3at (also known as PoE+). This component should be compatible with level 4/5 surge requirements of IEC 61000-4-5 since it is located on the secondary side of the coupling transformer, but lab testing should be conducted to confirm.

TVS Diode Array (SPA®Diodes)

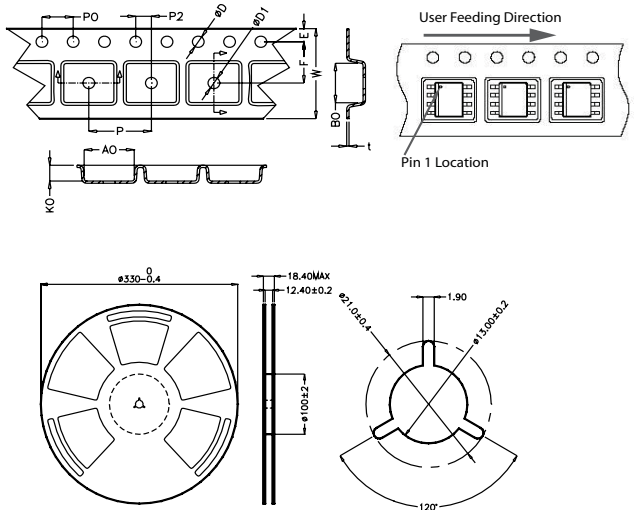
Lightning Surge Protection - SP1050 Series

Package Dimensions of SOIC-8



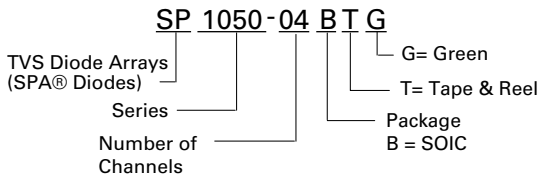
Package	SOIC			
Pins	8			
JEDEC	MS-012			
	Millimetres		Inches	
	Min	Max	Min	Max
A	1.35	1.75	0.053	0.069
A1	0.10	0.25	0.004	0.010
A2	1.25	1.65	0.050	0.065
B	0.31	0.51	0.012	0.020
c	0.17	0.25	0.007	0.010
D	4.80	5.00	0.189	0.197
E	5.80	6.20	0.228	0.244
E1	3.80	4.00	0.150	0.157
e	1.27 BSC		0.050 BSC	
L	0.40	1.27	0.016	0.050

Embossed Carrier Tape & Reel Specification — SOIC Package



	Millimetres		Inches	
	Min	Max	Min	Max
E	1.65	1.85	0.065	0.073
F	5.4	5.6	0.213	0.22
P2	1.95	2.05	0.077	0.081
D	1.5	1.6	0.059	0.063
D1	1.50 Min		0.059 Min	
P0	3.9	4.1	0.154	0.161
10P0	40.0 +/- 0.20		1.574 +/- 0.008	
W	11.9	12.1	0.468	0.476
P	7.9	8.1	0.311	0.319
A0	6.3	6.5	0.248	0.256
B0	5.1	5.3	0.2	0.209
K0	2	2.2	0.079	0.087
t	0.30 +/- 0.05		0.012 +/- 0.002	

Part Numbering System



Ordering Information

Part Number	Package	Min. Order Qty.
SP1050-04BTG	SOIC Tape & Reel	2500

Revision: 01/08/19