

Low-Power, 8-Channel, Serial 10-Bit ADC

ABSOLUTE MAXIMUM RATINGS

| | |
|-----------------------------|-----------------------------------|
| V _{DD} to AGND | -0.3V to +6V |
| AGND to DGND | -0.3V to +0.3V |
| CH0-CH7 to AGND, DGND | -0.3V to (V _{DD} + 0.3V) |
| CH0-CH7 Total Input Current | ±20mA |
| VREF to AGND | -0.3V to (V _{DD} + 0.3V) |
| REFADJ to AGND | -0.3V to (V _{DD} + 0.3V) |
| Digital Inputs to DGND | -0.3V to (V _{DD} + 0.3V) |
| Digital Outputs to DGND | -0.3V to (V _{DD} + 0.3V) |
| Digital Output Sink Current | 25mA |

| | |
|---|-----------------|
| Continuous Power Dissipation (T _A = +70°C) | |
| Plastic DIP (derate 11.11mW/°C above +70°C) | 889mW |
| SO (derate 10.00mW/°C above +70°C) | 800mW |
| SSOP (derate 8.00mW/°C above +70°C) | 640mW |
| CERDIP (derate 11.11mW/°C above +70°C) | 889mW |
| Operating Temperature Ranges | |
| MAX192_C_P | 0°C to +70°C |
| MAX192_E_P | -40°C to +85°C |
| MAX192_MJP | -55°C to +125°C |
| Storage Temperature Range | -60°C to +150°C |
| Lead Temperature (soldering, 10sec) | +300°C |

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{DD} = 5V ±5%, f_{CLK} = 2.0MHz, external clock (50% duty cycle), 15 clocks/conversion cycle (133ksp/s), 4.7µF capacitor at VREF pin, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|-------------------|---|-----|------|------|--------|
| DC ACCURACY (Note 1) | | | | | | |
| Resolution | | | 10 | | | Bits |
| Relative Accuracy (Note 2) | | MAX192A | | | ±1/2 | LSB |
| | | MAX192B | | | ±1 | |
| Differential Nonlinearity | DNL | No missing codes over temperature | | | ±1 | LSB |
| Offset Error | | | | | ±2 | LSB |
| Gain Error | | External reference, 4.096V | | | ±2 | LSB |
| Gain Temperature Coefficient | | External reference, 4.096V | | ±0.8 | | ppm/°C |
| Channel-to-Channel Offset Matching | | | | ±0.1 | | LSB |
| DYNAMIC SPECIFICATIONS (10kHz sine-wave input, 4.096Vp-p, 133ksp/s, 2.0MHz external clock) | | | | | | |
| Signal-to-Noise + Distortion Ratio | SINAD | | | 66 | | dB |
| Total Harmonic Distortion (up to the 5th harmonic) | THD | | | -70 | | dB |
| Spurious-Free Dynamic Range | SFDR | | | 70 | | dB |
| Channel-to-Channel Crosstalk | | 65kHz, V _{IN} = 4.096Vp-p (Note 3) | | -75 | | dB |
| Small-Signal Bandwidth | | -3dB rolloff | | 4.5 | | MHz |
| Full-Power Bandwidth | | | | 800 | | kHz |
| CONVERSION RATE | | | | | | |
| Conversion Time (Note 4) | t _{CONV} | Internal clock | 5.5 | | 10 | µs |
| | | External clock, 2MHz, 12 clocks/conversion | 6 | | | |
| Track/Hold Acquisition Time | t _{AZ} | | | | 1.5 | µs |
| Aperture Delay | | | | 10 | | ns |
| Aperture Jitter | | | | <50 | | ps |
| Internal Clock Frequency | | | | 1.7 | | MHz |

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ELECTRICAL CHARACTERISTICS (continued)

($V_{DD} = 5V \pm 5\%$, $f_{CLK} = 2.0MHz$, external clock (50% duty cycle), 15 clocks/conversion cycle (133kps), 4.7 μF capacitor at VREF pin, $T_A = T_{MIN}$ to T_{MAX} , unless otherwise noted. Typical values are at $T_A = +25^\circ C$.)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS | |
|---|--------|--|----------|------------------------|----------------------|------------------------|--------|
| External Clock Frequency | | External compensation, 4.7μF | 0.1 | | 2.0 | MHz | |
| | | Internal compensation (Note 5) | 0.1 | | 0.4 | | |
| | | Used for data transfer only | | 10 | | | |
| ANALOG INPUT | | | | | | | |
| Analog Input Voltage (Note 6) | | Common-mode range (any input) | | 0 | V _{DD} | V | |
| | | Single-ended range (unipolar only) | | 0 | V _{REF} | | |
| | | Differential range | Unipolar | 0 | V _{REF} | | |
| | | | Bipolar | $-\frac{V_{REF}}{2}$ | $+\frac{V_{REF}}{2}$ | | |
| Multiplexer Leakage Current | | On/off leakage current; V _{IN} = 0V, 5V | | ±0.01 | ±1 | μA | |
| Input Capacitance | | (Note 5) | | 16 | | pF | |
| INTERNAL REFERENCE (reference buffer enabled) | | | | | | | |
| VREF Output Voltage | | T _A = +25°C (Note 7) | | 4.066 | 4.096 | 4.126 | V |
| VREF Short-Circuit Current | | | | | | 30 | mA |
| VREF Tempco | | | | | ±30 | | ppm/°C |
| Load Regulation (Note 8) | | 0mA to 0.5mA output load | | | 2.5 | | mV |
| Capacitive Bypass at VREF | | Internal compensation | | 0 | | | μF |
| | | External compensation | | 4.7 | | | |
| Capacitive Bypass at REFADJ | | Internal compensation | | 0.01 | | | μF |
| | | External compensation | | 0.01 | | | |
| REFADJ Adjustment Range | | | | | ±1.5 | | % |
| EXTERNAL REFERENCE AT VREF (buffer disabled, VREF = 4.096V) | | | | | | | |
| Input Voltage Range | | | | 2.5 | | V _{DD} + 50mV | V |
| Input Current | | | | | 200 | 350 | μA |
| Input Resistance | | | | 12 | 20 | | kΩ |
| Shutdown VREF Input Current | | | | | 1.5 | 10 | μA |
| Buffer Disable Threshold REFADJ | | | | V _{DD} - 50mV | | | V |
| EXTERNAL REFERENCE AT REFADJ | | | | | | | |
| Capacitive Bypass at VREF | | Internal compensation mode | | 0 | | | μF |
| | | External compensation mode | | 4.7 | | | |
| Reference-Buffer Gain | | | | | 1.678 | | V/V |
| REFADJ Input Current | | | | | | ±50 | μA |

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ELECTRICAL CHARACTERISTICS (continued)

($V_{DD} = 5V \pm 5\%$, $f_{CLK} = 2.0MHz$, external clock (50% duty cycle), 15 clocks/conversion cycle (133ksp/s), 4.7 μF capacitor at VREF pin, $T_A = T_{MIN}$ to T_{MAX} , unless otherwise noted. Typical values are at $T_A = +25^\circ C$.)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|------------|--|----------------|----------------|-----------|---------|
| DIGITAL INPUTS (DIN, SCLK, \overline{CS}, \overline{SHDN}) | | | | | | |
| DIN, SCLK, \overline{CS} Input High Voltage | V_{INH} | | 2.4 | | | V |
| DIN, SCLK, \overline{CS} Input Low Voltage | V_{INL} | | | | 0.8 | V |
| DIN, SCLK, \overline{CS} Input Hysteresis | V_{HYST} | | | 0.15 | | V |
| DIN, SCLK, \overline{CS} Input Leakage | I_{IN} | $V_{IN} = 0V$ or V_{DD} | | | ± 1 | μA |
| DIN, SCLK, \overline{CS} Input Capacitance | C_{IN} | (Note 5) | | | 15 | pF |
| \overline{SHDN} Input High Voltage | V_{INH} | | $V_{DD} - 0.5$ | | | V |
| \overline{SHDN} Input Low Voltage | V_{INL} | | | | 0.5 | V |
| \overline{SHDN} Input Current, High | I_{INH} | $\overline{SHDN} = V_{DD}$ | | | 4.0 | μA |
| \overline{SHDN} Input Current, Low | I_{INL} | $\overline{SHDN} = 0V$ | -4.0 | | | μA |
| \overline{SHDN} Input Mid Voltage | V_{IM} | | 1.5 | $V_{DD} - 1.5$ | | V |
| \overline{SHDN} Voltage, Floating | V_{FLT} | $\overline{SHDN} = \text{open}$ | | 2.75 | | V |
| \overline{SHDN} Max Allowed Leakage, Mid Input | | $\overline{SHDN} = \text{open}$ | -100 | | 100 | nA |
| DIGITAL OUTPUTS (DOUT, SSTRB) | | | | | | |
| Output Voltage Low | V_{OL} | $I_{SINK} = 5mA$ | | | 0.4 | V |
| | | $I_{SINK} = 16mA$ | | 0.3 | | |
| Output Voltage High | V_{OH} | $I_{SOURCE} = 1mA$ | 4 | | | V |
| Three-State Leakage Current | I_L | $\overline{CS} = 5V$ | | | ± 10 | μA |
| Three-State Leakage Capacitance | C_{OUT} | $\overline{CS} = 5V$ (Note 5) | | | 15 | pF |
| POWER REQUIREMENTS | | | | | | |
| Positive Supply Voltage | V_{DD} | | | $5 \pm 5\%$ | | V |
| Positive Supply Current | I_{DD} | Operating mode | | 1.5 | 2.5 | mA |
| | | Fast power-down | | 30 | 70 | |
| | | Full power-down | | 2 | 10 | μA |
| Positive Supply Rejection (Note 9) | PSR | $V_{DD} = 5V \pm 5\%$; external reference, 4.096V; full-scale input | | ± 0.06 | ± 0.5 | mV |

Note 1: Tested at $V_{DD} = 5.0V$; single-ended, unipolar.

Note 2: Relative accuracy is the deviation of the analog value at any code from its theoretical value after the full-scale range has been calibrated.

Note 3: Grounded on-channel; sine wave applied to all off channels.

Note 4: Conversion time defined as the number of clock cycles times the clock period; clock has 50% duty cycle.

Note 5: Guaranteed by design. Not subject to production testing.

Note 6: The common-mode range for the analog inputs is from AGND to V_{DD} .

Note 7: Sample tested to 0.1% AQL.

Note 8: External load should not change during conversion for specified accuracy.

Note 9: Measured at $V_{SUPPLY} + 5\%$ and $V_{SUPPLY} - 5\%$ only.

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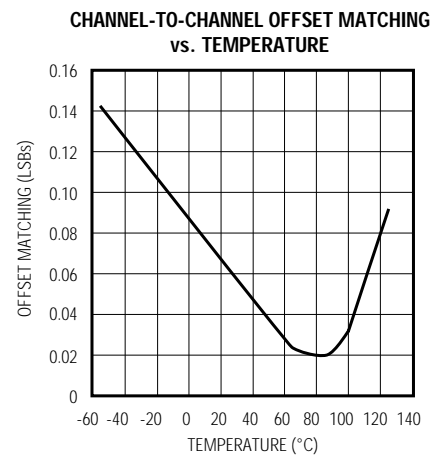
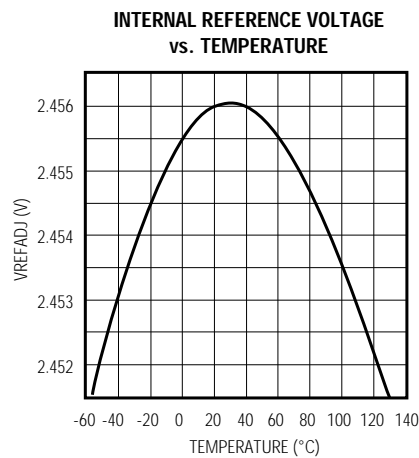
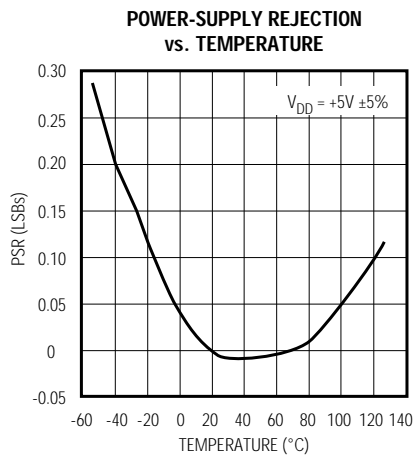
TIMING CHARACTERISTICS

($V_{DD} = 5V \pm 5\%$, $T_A = T_{MIN}$ to T_{MAX} , unless otherwise noted.)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|-------------|--|-----|-----|-----|---------|
| Acquisition Time | t_{AZ} | | 1.5 | | | μs |
| DIN to SCLK Setup | t_{DS} | | 100 | | | ns |
| DIN to SCLK Hold | t_{DH} | | | | 0 | ns |
| SCLK Fall to Output Data Valid | t_{DO} | $C_{LOAD} = 100pF$ | 20 | | 150 | ns |
| \overline{CS} Fall to Output Enable | t_{DV} | $C_{LOAD} = 100pF$ | | | 100 | ns |
| \overline{CS} Rise to Output Disable | t_{TR} | $C_{LOAD} = 100pF$ | | | 100 | ns |
| \overline{CS} to SCLK Rise Setup | t_{CSS} | | 100 | | | ns |
| \overline{CS} to SCLK Rise Hold | t_{CSH} | | 0 | | | ns |
| SCLK Pulse Width High | t_{CH} | | 200 | | | ns |
| SCLK Pulse Width Low | t_{CL} | | 200 | | | ns |
| SCLK Fall to SSTRB | t_{SSTRB} | $C_{LOAD} = 100pF$ | | | 200 | ns |
| \overline{CS} Fall to SSTRB Output Enable (Note 5) | t_{SDV} | External clock mode only, $C_{LOAD} = 100pF$ | | | 200 | ns |
| \overline{CS} Rise to SSTRB Output Disable (Note 5) | t_{STR} | External clock mode only, $C_{LOAD} = 100pF$ | | | 200 | ns |
| SSTRB Rise to SCLK Rise (Note 5) | t_{SCK} | Internal clock mode only | 0 | | | ns |

Note 5: Guaranteed by design. Not subject to production testing.

Typical Operating Characteristics



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Pin Description

| PIN | NAME | FUNCTION |
|-------|--------------------------|--|
| 1–8 | CH0–CH7 | Sampling Analog Inputs |
| 9, 13 | AGND | Analog Ground. Also IN- Input for single-enabled conversions. Connect both AGND pins to analog ground. |
| 10 | $\overline{\text{SHDN}}$ | Three-Level Shutdown Input. Pulling SHDN low shuts the MAX192 down to 10 μ A (max) supply current, otherwise the MAX192 is fully operational. Pulling SHDN high puts the reference-buffer amplifier in internal compensation mode. Letting SHDN float puts the reference-buffer amplifier in external compensation mode. |
| 11 | VREF | Reference Voltage for analog-to-digital conversion. Also, Output of the Reference Buffer Amplifier. Add a 4.7 μ F capacitor to ground when using external compensation mode. Also functions as an input when used with a precision external reference. |
| 12 | REFADJ | Reference-Buffer Amplifier Input. To disable the reference-buffer amplifier, tie REFADJ to V _{DD} . |
| 14 | DGND | Digital Ground |
| 15 | DOUT | Serial Data Output. Data is clocked out at the falling edge of SCLK. High impedance when $\overline{\text{CS}}$ is high. |
| 16 | SSTRB | Serial Strobe Output. In internal clock mode, SSTRB goes low when the MAX192 begins the A/D conversion and goes high when the conversion is done. In external clock mode, SSTRB pulses high for one clock period before the MSB decision. SSTRB is high impedance when $\overline{\text{CS}}$ is high (external mode). |
| 17 | DIN | Serial Data Input. Data is clocked in at the rising edge of SCLK. |
| 18 | $\overline{\text{CS}}$ | Active-Low Chip Select. Data will not be clocked into DIN unless $\overline{\text{CS}}$ is low. When $\overline{\text{CS}}$ is high, DOUT is high impedance. |
| 19 | SCLK | Serial Clock Input. Clocks data in and out of serial interface. In external clock mode, SCLK also sets the conversion speed. (Duty cycle must be 40% to 60% in external clock mode.) |
| 20 | VDD | Positive Supply Voltage, +5V \pm 5% |

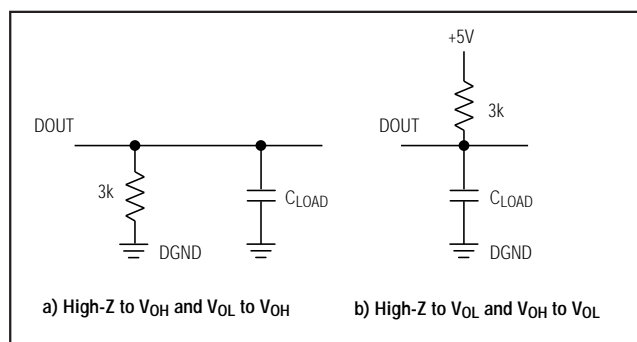


Figure 1. Load Circuits for Enable Time

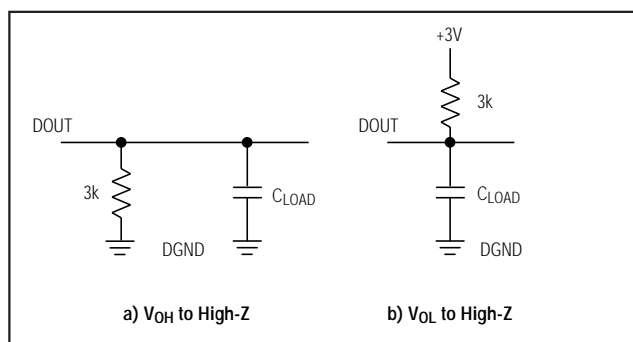


Figure 2. Load Circuits for Disabled Time

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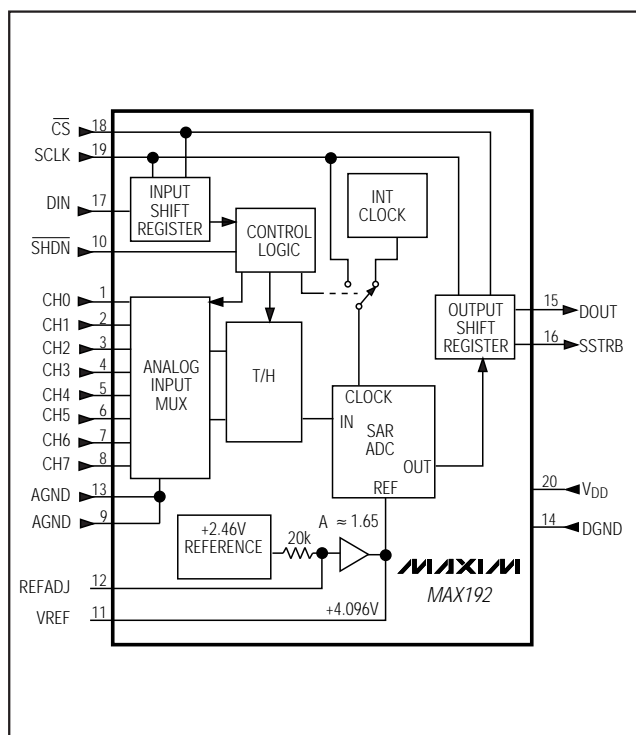


Figure 3. Block Diagram

Detailed Description

The MAX192 uses a successive-approximation conversion technique and input track/hold (T/H) circuitry to convert an analog signal to a 10-bit digital output. A flexible serial interface provides easy interface to microprocessors. No external hold capacitors are required. Figure 3 shows the block diagram for the MAX192.

Pseudo-Differential Input

The sampling architecture of the ADC's analog comparator is illustrated in the Equivalent Input Circuit (Figure 4). In single-ended mode, IN+ is internally switched to CH0–CH7 and IN- is switched to AGND. In differential mode, IN+ and IN- are selected from pairs of CH0/CH1, CH2/CH3, CH4/CH5, and CH6/CH7. Refer to Tables 1 and 2 to configure the channels.

In differential mode, IN- and IN+ are internally switched to either one of the analog inputs. This configuration is pseudo-differential to the effect that only the signal at IN+ is sampled. The return side (IN-) must remain stable within $\pm 0.5\text{LSB}$ ($\pm 0.1\text{LSB}$ for best results) with

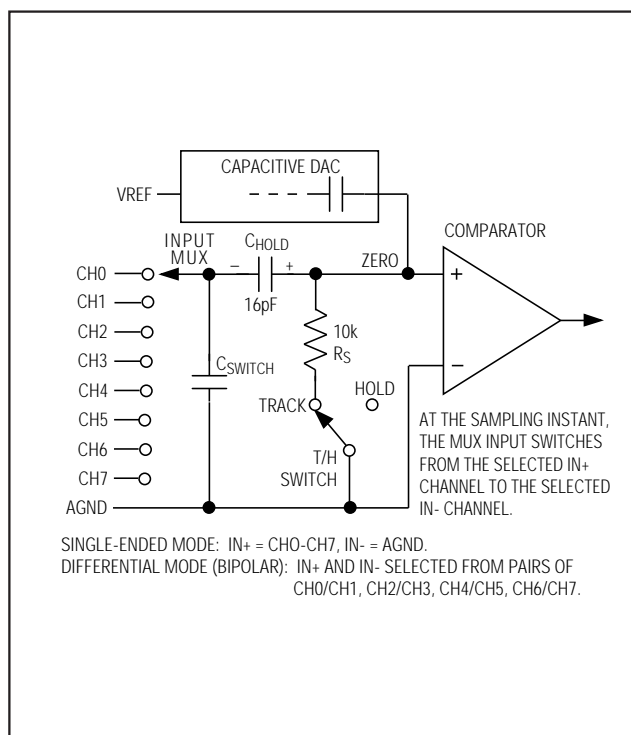


Figure 4. Equivalent Input Circuit

respect to AGND during a conversion. Accomplish this by connecting a $0.1\mu\text{F}$ capacitor from AIN- (the selected analog input, respectively) to AGND.

During the acquisition interval, the channel selected as the positive input (IN+) charges capacitor C_{HOLD} . The acquisition interval spans three SCLK cycles and ends on the falling SCLK edge after the last bit of the input control word has been entered. At the end of the acquisition interval, the T/H switch opens, retaining charge on C_{HOLD} as a sample of the signal at IN+.

The conversion interval begins with the input multiplexer switching C_{HOLD} from the positive input (IN+) to the negative input (IN-). In single-ended mode, IN- is simply AGND. This unbalances node ZERO at the input of the comparator. The capacitive DAC adjusts during the remainder of the conversion cycle to restore its node ZERO to 0V within the limits of its resolution. This action is equivalent to transferring a charge of $16\text{pF} \times (V_{\text{IN}+} - V_{\text{IN}-})$ from C_{HOLD} to the binary-weighted capacitive DAC, which in turn forms a digital representation of the analog input signal.

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Track/Hold

The T/H enters its tracking mode on the falling clock edge after the fifth bit of the 8-bit control word has been shifted in. The T/H enters its hold mode on the falling clock edge after the eighth bit of the control word has been shifted in. If the converter is set up for single-ended inputs, IN- is connected to AGND, and the converter samples the "+" input. If the converter is set up for differential inputs, IN- connects to the "-" input, and the difference of $|IN+ - IN-|$ is sampled. At the end of the conversion, the positive input connects back to IN+, and CHOLD charges to the input signal.

The time required for the T/H to acquire an input signal is a function of how quickly its input capacitance is charged. If the input signal's source impedance is high, the acquisition time lengthens and more time must be allowed between conversions. Acquisition time is calculated by:

$$t_{AZ} = 9 (R_S + R_{IN}) 16pF$$

where $R_{IN} = 5k\Omega$, R_S = the source impedance of the input signal, and t_{AZ} is never less than $1.5\mu s$. Note that source impedances below $5k\Omega$ do not significantly affect the AC performance of the ADC. Higher source impedances can be used if an input capacitor is connected to the analog inputs, as shown in Figure 5. Note that the input capacitor forms an RC filter with the input source impedance, limiting the ADC's signal bandwidth.

Input Bandwidth

The ADC's input tracking circuitry has a 4.5MHz small-signal bandwidth, so it is possible to digitize high-speed transient events and measure periodic signals with bandwidths exceeding the ADC's sampling rate by using undersampling techniques. To avoid high-frequency signals being aliased into the frequency

band of interest, anti-alias filtering is recommended. See the data sheets for the MAX291–MAX297 filters.

Analog Input Range and Input Protection

Internal protection diodes, which clamp the analog input to V_{DD} and AGND, allow the channel input pins to swing from AGND - 0.3V to $V_{DD} + 0.3V$ without damage. However, for accurate conversions near full scale, the inputs must not exceed V_{DD} by more than 50mV, or be lower than AGND by 50mV.

If the analog input exceeds 50mV beyond the supplies, do not forward bias the protection diodes of off channels over 2mA.

The MAX192 can be configured for differential (unipolar or bipolar) or single-ended (unipolar only) inputs, as selected by bits 2 and 3 of the control byte (Table 3).

In the single-ended mode, set the UNI/BIP bit to unipolar. In this mode, analog inputs are internally referenced to AGND, with a full-scale input range from 0V to V_{REF} .

In differential mode, both unipolar and bipolar settings can be used. Choosing unipolar mode sets the differential input range at 0V to V_{REF} . The output code is invalid (code zero) when a negative differential input voltage is applied. Bipolar mode sets the differential input range to $\pm V_{REF} / 2$. Note that in this differential mode, the common-mode input range includes both supply rails. Refer to Tables 4a and 4b for input voltage ranges.

Quick Look

To evaluate the analog performance of the MAX192 quickly, use Figure 5's circuit. The MAX192 requires a control byte to be written to DIN before each conversion. Tying DIN to +5V feeds in control bytes of

Table 1. Channel Selection in Single-Ended Mode ($SGL/DIF = 1$)

| SEL2 | SEL1 | SEL0 | CH0 | CH1 | CH2 | CH3 | CH4 | CH5 | CH6 | CH7 | AGND |
|------|------|------|-----|-----|-----|-----|-----|-----|-----|-----|------|
| 0 | 0 | 0 | + | | | | | | | | - |
| 1 | 0 | 0 | | + | | | | | | | - |
| 0 | 0 | 1 | | | + | | | | | | - |
| 1 | 0 | 1 | | | | + | | | | | - |
| 0 | 1 | 0 | | | | | + | | | | - |
| 1 | 1 | 0 | | | | | | + | | | - |
| 0 | 1 | 1 | | | | | | | + | | - |
| 1 | 1 | 1 | | | | | | | | + | - |

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Table 2. Channel Selection in Differential Mode ($\overline{\text{SGL/DIF}} = 0$)

| SEL2 | SEL1 | SEL0 | CH0 | CH1 | CH2 | CH3 | CH4 | CH5 | CH6 | CH7 |
|------|------|------|-----|-----|-----|-----|-----|-----|-----|-----|
| 0 | 0 | 0 | + | - | | | | | | |
| 0 | 0 | 1 | | | + | - | | | | |
| 0 | 1 | 0 | | | | | + | - | | |
| 0 | 1 | 1 | | | | | | | + | - |
| 1 | 0 | 0 | - | + | | | | | | |
| 1 | 0 | 1 | | | - | + | | | | |
| 1 | 1 | 0 | | | | | - | + | | |
| 1 | 1 | 1 | | | | | | | - | + |

Table 3. Control-Byte Format

| Bit 7 (MSB) | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 (LSB) | | | | | | | | | | | | | | | |
|-------------|------------------------------|---|-------|------------------------------|------------------------------|-------|-------------|-----|-----|------|----------|----------|--|----------|----------|---|----------|----------|---------------------|----------|----------|---------------------|
| START | SEL2 | SEL1 | SEL0 | UNI/ $\overline{\text{BIP}}$ | SGL/ $\overline{\text{DIF}}$ | PD1 | PD0 | | | | | | | | | | | | | | | |
| Bit | Name | Description | | | | | | | | | | | | | | | | | | | | |
| 7(MSB) | START | The first logic "1" bit after $\overline{\text{CS}}$ goes low defines the beginning of the control byte. | | | | | | | | | | | | | | | | | | | | |
| 6 5 4 | SEL2 SEL1 SEL0 | These three bits select which of the eight channels are used for the conversion. See Tables 1 and 2. | | | | | | | | | | | | | | | | | | | | |
| 3 | UNI/ $\overline{\text{BIP}}$ | 1 = unipolar, 0 = bipolar. Selects unipolar or bipolar conversion mode. In unipolar mode, an analog input signal from 0V to VREF can be converted; in differential bipolar mode, the differential signal can range from -VREF / 2 to +VREF / 2. Select differential operation if bipolar mode is used. | | | | | | | | | | | | | | | | | | | | |
| 2 | SGL/ $\overline{\text{DIF}}$ | 1 = single ended, 0 = differential. Selects single-ended or differential conversions. In single-ended mode, input signal voltages are referred to AGND. In differential mode, the voltage difference between two channels is measured. Select unipolar operation if single-ended mode is used. See Tables 1 and 2. | | | | | | | | | | | | | | | | | | | | |
| 1 0(LSB) | PD1 PD0 | Selects clock and power-down modes. <table><tr><th>PD1</th><th>PD0</th><th>Mode</th></tr><tr><td>0</td><td>0</td><td>Full power-down ($I_Q = 2\mu\text{A}$)</td></tr><tr><td>0</td><td>1</td><td>Fast power-down ($I_Q = 30\mu\text{A}$)</td></tr><tr><td>1</td><td>0</td><td>Internal clock mode</td></tr><tr><td>1</td><td>1</td><td>External clock mode</td></tr></table> | | | | | | PD1 | PD0 | Mode | 0 | 0 | Full power-down ($I_Q = 2\mu\text{A}$) | 0 | 1 | Fast power-down ($I_Q = 30\mu\text{A}$) | 1 | 0 | Internal clock mode | 1 | 1 | External clock mode |
| PD1 | PD0 | Mode | | | | | | | | | | | | | | | | | | | | |
| 0 | 0 | Full power-down ($I_Q = 2\mu\text{A}$) | | | | | | | | | | | | | | | | | | | | |
| 0 | 1 | Fast power-down ($I_Q = 30\mu\text{A}$) | | | | | | | | | | | | | | | | | | | | |
| 1 | 0 | Internal clock mode | | | | | | | | | | | | | | | | | | | | |
| 1 | 1 | External clock mode | | | | | | | | | | | | | | | | | | | | |

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Table 4a. Unipolar Full Scale and Zero Scale

| REFERENCE | | ZERO SCALE | FULL SCALE |
|--------------------|-----------|------------|-----------------|
| Internal Reference | | 0V | +4.096V |
| External Reference | at REFADJ | 0V | VREFADJ (1.678) |
| | at VREF | 0V | VREF |

Table 4b. Differential Bipolar Full Scale, Zero Scale, and Negative Full Scale

| REFERENCE | | NEGATIVE FULL SCALE | ZERO SCALE | FULL SCALE |
|--------------------|-----------|---------------------|------------|---------------------|
| Internal Reference | | -4.096V / 2 | 0V | +4.096V / 2 |
| External Reference | at REFADJ | -1/2VREFADJ (1.678) | 0V | +1/2VREFADJ (1.678) |
| | at VREF | -1/2VREF | 0V | +1/2VREF |

\$FF (HEX), which trigger single-ended conversions on CH7 in external clock mode without powering down between conversions. In external clock mode, the SSTRB output pulses high for one clock period before the most significant bit of the conversion result comes out of DOUT. Varying the analog input to CH7 should alter the sequence of bits from DOUT. A total of 15 clock cycles is required per conversion. All transitions of the SSTRB and DOUT outputs occur on the falling edge of SCLK.

How to Start a Conversion

A conversion is started on the MAX192 by clocking a control byte into DIN. Each rising edge on SCLK, with \overline{CS} low, clocks a bit from DIN into the MAX192's internal shift register. After \overline{CS} falls, the first arriving logic "1" bit defines the MSB of the control byte. Until this first "start" bit arrives, any number of logic "0" bits can be clocked into DIN with no effect. Table 3 shows the control-byte format.

The MAX192 is compatible with Microwire, SPI, and QSPI devices. For SPI, select the correct clock polarity and sampling edge in the SPI control registers: set CPOL = 0 and CPHA = 0. Microwire and SPI both transmit a byte and receive a byte at the same time. Using the *Typical Operating Circuit*, the simplest software interface requires only three 8-bit transfers to perform a conversion (one 8-bit transfer to configure the ADC, and two more 8-bit transfers to clock out the 12-bit conversion result).

Example: Simple Software Interface

Make sure the CPU's serial interface runs in master mode so the CPU generates the serial clock. Choose a clock frequency from 100kHz to 2MHz.

- 1) Set up the control byte for external clock mode, call it TB1. TB1 should be of the format: 1XXXXX11 binary, where the Xs denote the particular channel and conversion-mode selected.
- 2) Use a general-purpose I/O line on the CPU to pull \overline{CS} on the MAX192 low.
- 3) Transmit TB1 and simultaneously receive a byte and call it RB1. Ignore RB1.
- 4) Transmit a byte of all zeros (\$00 HEX) and simultaneously receive byte RB2.
- 5) Transmit a byte of all zeros (\$00 HEX) and simultaneously receive byte RB3.
- 6) Pull \overline{CS} on the MAX192 high.

Figure 6 shows the timing for this sequence. Bytes RB2 and RB3 will contain the result of the conversion padded with one leading zero, two sub-LSB bits, and three trailing zeros. The total conversion time is a function of the serial clock frequency and the amount of dead time between 8-bit transfers. Make sure that the total conversion time does not exceed 120μs, to avoid excessive T/H droop.

Digital Output

In unipolar input mode, the output is straight binary (Figure 15). For bipolar inputs in differential mode, the output is twos-complement (Figure 16). Data is clocked out at the falling edge of SCLK in MSB-first format.

Internal and External Clock Modes

The MAX192 may use either an external serial clock or the internal clock to perform the successive-approximation conversion. In both clock modes, the external clock shifts data in and out of the MAX192. The T/H acquires the input signal as the last three bits of the control byte are clocked into DIN. Bits PD1 and PD0 of the control byte program the clock mode. Figures 7 through 10 show the timing characteristics common to both modes.

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MAX192

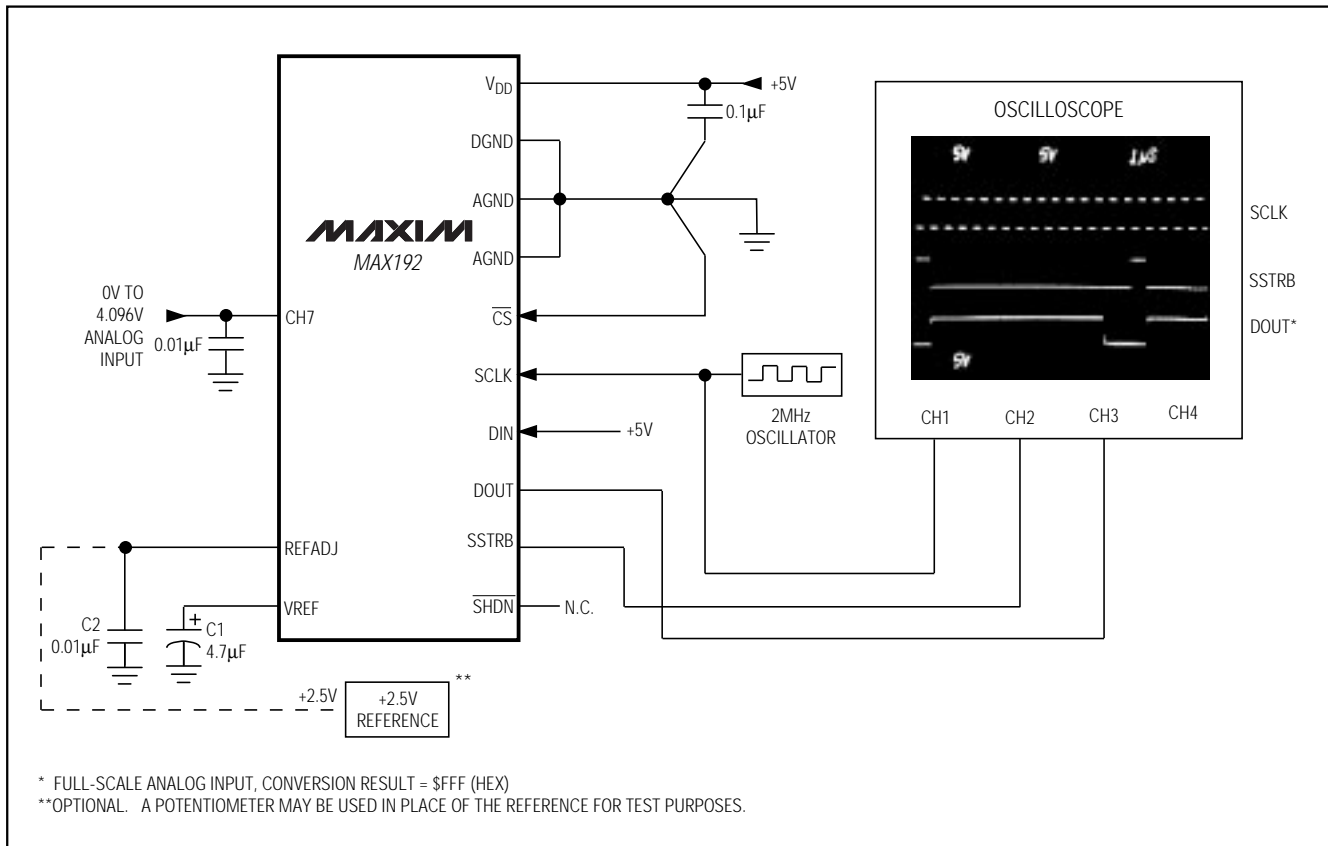


Figure 5. Quick-Look Circuit

External Clock

In external clock mode, the external clock not only shifts data in and out, it also drives the analog-to-digital conversion steps. SSTRB pulses high for one clock period after the last bit of the control byte. Successive-approximation bit decisions are made and appear at DOUT on each of the next 12 SCLK falling edges (see Figure 6). The first 10 bits are the true data bits, and the last two are sub-LSB bits.

SSTRB and DOUT go into a high-impedance state when CS goes high; after the next CS falling edge, SSTRB will output a logic low. Figure 8 shows the SSTRB timing in external clock mode.

The conversion must complete in some minimum time, or else droop on the sample-and-hold capacitors may degrade conversion results. Use internal clock mode if the clock period exceeds 10µs, or if serial-clock interruptions could cause the conversion interval to exceed 120µs.

Internal Clock

In internal clock mode, the MAX192 generates its own conversion clock internally. This frees the microprocessor from the burden of running the SAR conversion clock, and allows the conversion results to be read back at the processor's convenience, at any clock rate from zero to typically 10MHz. SSTRB goes low at the start of the conversion and then goes high when the conversion is complete. SSTRB will be low for a maximum of 10µs, during which time SCLK should remain low for best noise performance. An internal register stores data when the conversion is in progress. SCLK clocks the data out at this register at any time after the conversion is complete. After SSTRB goes high, the next falling clock edge will produce the MSB of the conversion at DOUT, followed by the remaining bits in MSB-first format (Figure 9). CS does not need to be held low once a conversion is started.

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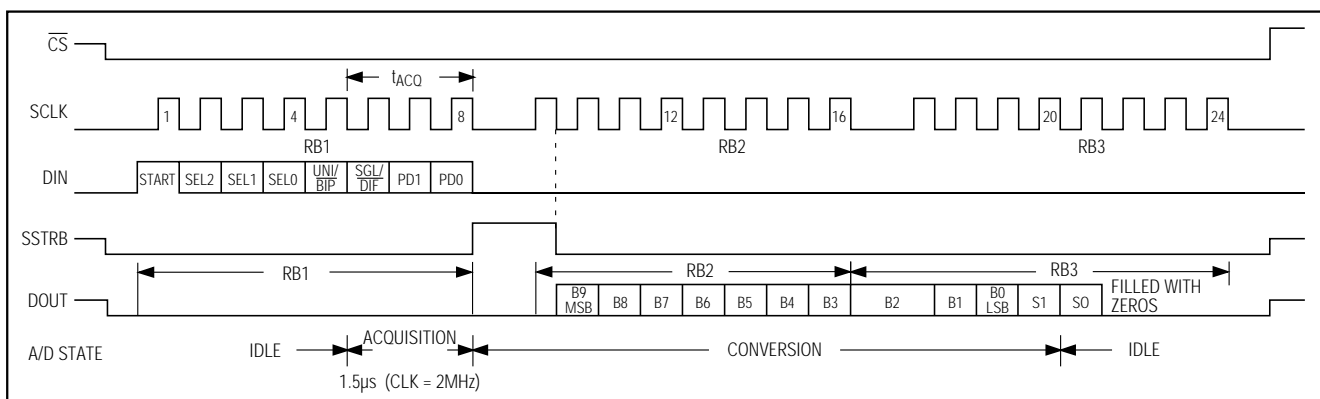


Figure 6. 24-Bit External Clock Mode Conversion Timing (SPI, QSPI and Microwire Compatible)

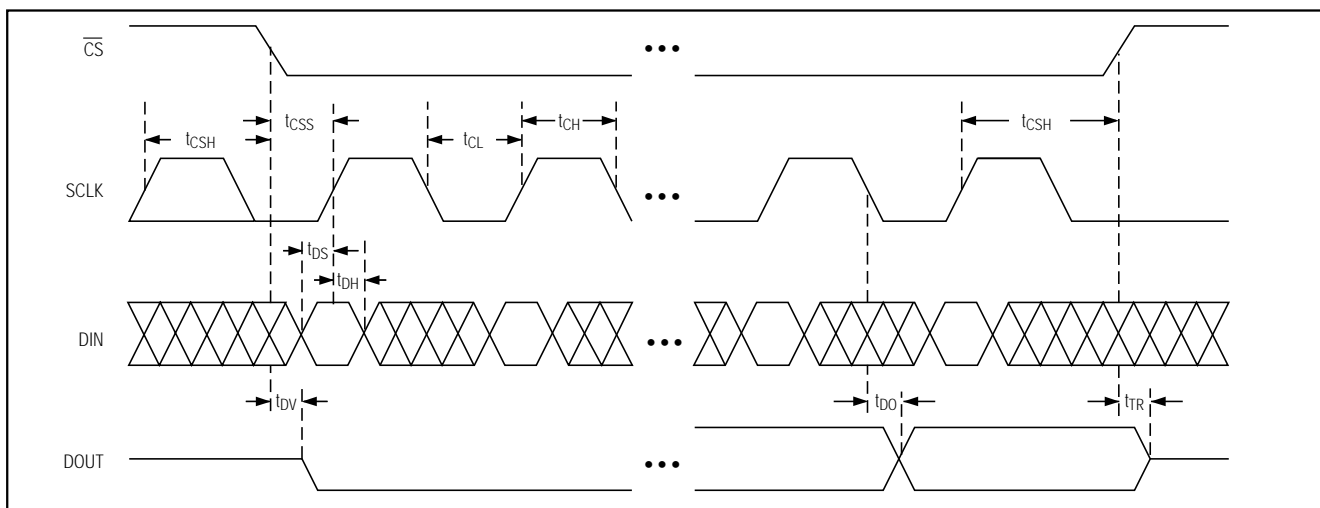


Figure 7. Detailed Serial-Interface Timing

Pulling \overline{CS} high prevents data from being clocked into the MAX192 and three-states DOUT, but it does not adversely affect an internal clock-mode conversion already in progress. When internal clock mode is selected, SSTRB does not go into a high-impedance state when \overline{CS} goes high.

Figure 10 shows the SSTRB timing in internal clock mode. In internal clock mode, data can be shifted in and out of the MAX192 at clock rates exceeding 4.0MHz, provided that the minimum acquisition time, t_{AZ} , is kept above 1.5µs.

Data Framing

The falling edge of \overline{CS} does **not** start a conversion on the MAX192. The first logic high clocked into DIN is interpreted as a start bit and defines the first bit of the control byte. A conversion starts on the falling edge of SCLK,

after the eighth bit of the control byte (the PD0 bit) is clocked into DIN. The start bit is defined as:

The first high bit clocked into DIN with \overline{CS} low any-time the converter is idle, e.g. after V_{DD} is applied.

OR

The first high bit clocked into DIN after bit 3 of a conversion in progress is clocked onto the DOUT pin.

If a falling edge on \overline{CS} forces a start bit before bit 3 (B3) becomes available, then the current conversion will be terminated and a new one started. Thus, the fastest the MAX192 can run is 15 clocks per conversion. Figure 11a shows the serial-interface timing necessary to perform a conversion every 15 SCLK cycles in external clock mode. If \overline{CS} is low and SCLK is continuous, guarantee a start bit by first clocking in 16 zeros.

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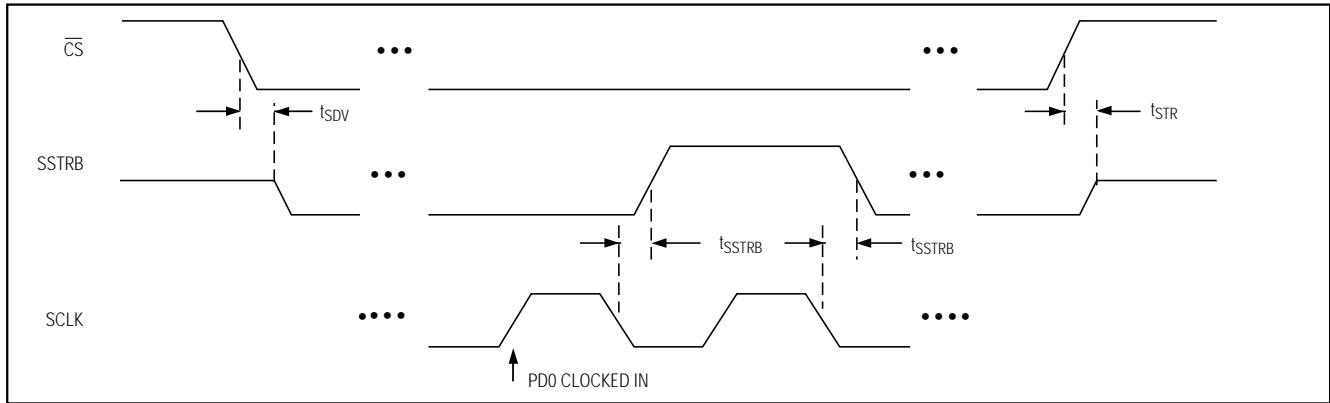


Figure 8. External Clock Mode SSTRB Detailed Timing

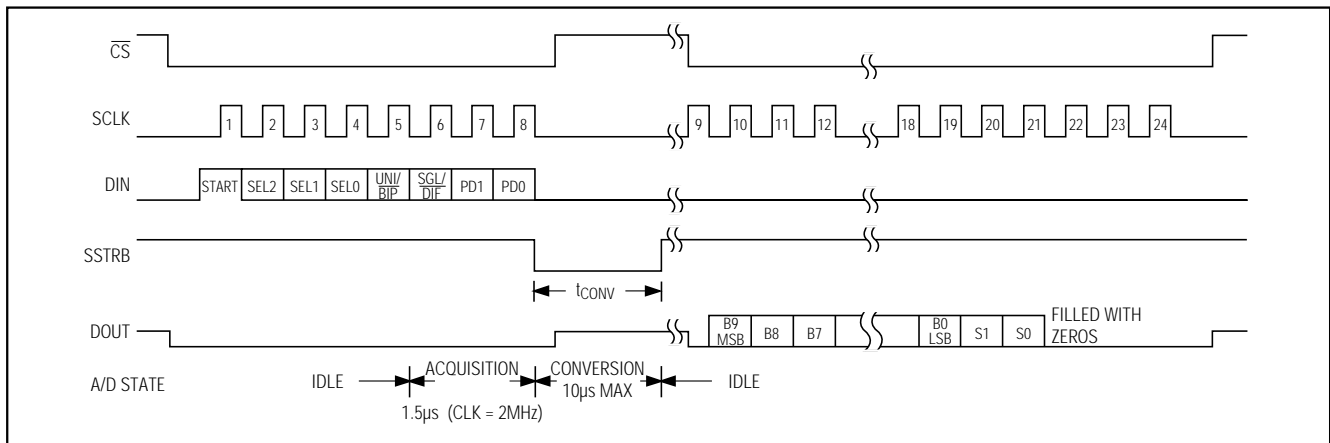


Figure 9. Internal Clock Mode Timing

Most microcontrollers require that conversions occur in multiples of 8 SCLK clocks; 16 clocks per conversion will typically be the fastest that a microcontroller can drive the MAX192. Figure 11b shows the serial-interface timing necessary to perform a conversion every 16 SCLK cycles in external clock mode.

Applications Information

Power-On Reset

When power is first applied and if SHDN is not pulled low, internal power-on reset circuitry will activate the MAX192 in internal clock mode, ready to convert with SSTRB = high. After the power supplies have been stabilized, the internal reset time is 100μs and no conversions should be performed during this phase. SSTRB is high on power-up and, if CS is low, the first logical 1 on DIN will be interpreted as a start bit. Until a conversion takes place, DOUT will shift out zeros.

Reference-Buffer Compensation

In addition to its shutdown function, the SHDN pin also selects internal or external compensation. The compensation affects both power-up time and maximum conversion speed. Compensated or not, the minimum clock rate is 100kHz due to droop on the sample-and-hold.

To select external compensation, float SHDN. See the *Typical Operating Circuit*, which uses a 4.7μF capacitor at VREF. A value of 4.7μF or greater ensures stability and allows operation of the converter at the full clock speed of 2MHz. External compensation increases power-up time (see the *Choosing Power-Down Mode* section, and Table 5).

Internal compensation requires no external capacitor at VREF, and is selected by pulling SHDN high. Internal compensation allows for shortest power-up times, but is only available using an external clock and reduces the maximum clock rate to 400kHz.

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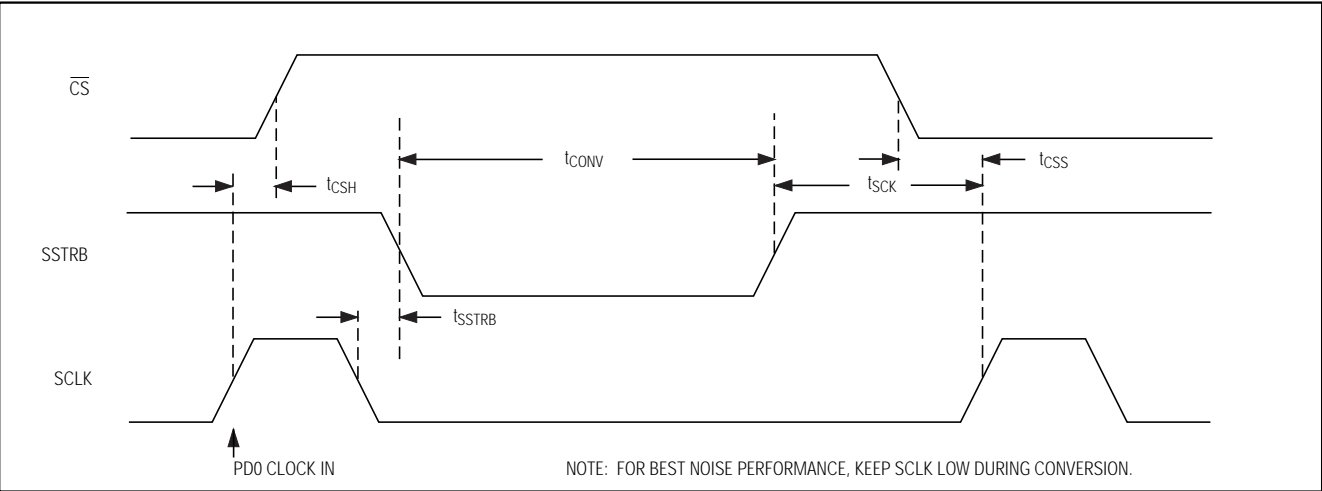


Figure 10. Internal Clock Mode SSTRB Detailed Timing

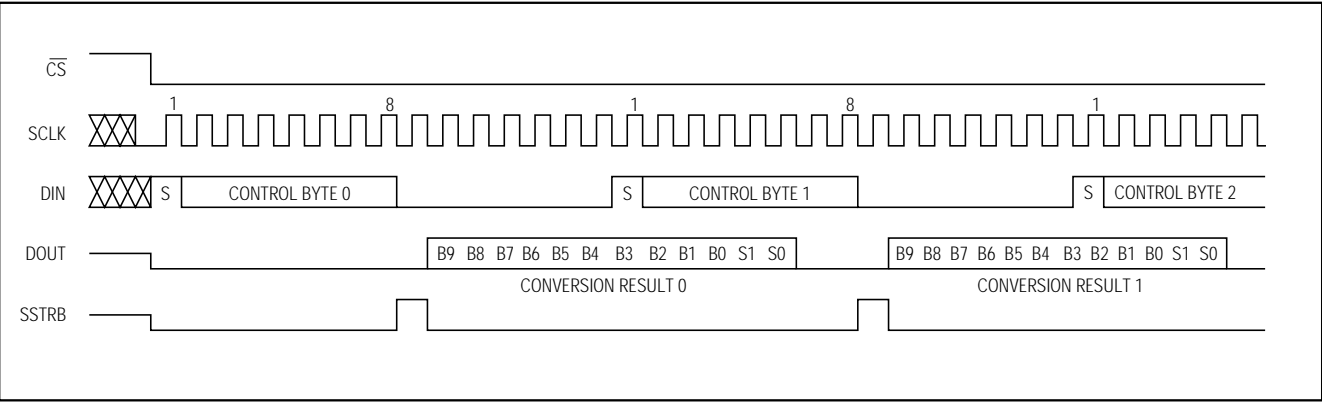


Figure 11a. External Clock Mode, 15 Clocks/Conversion Timing

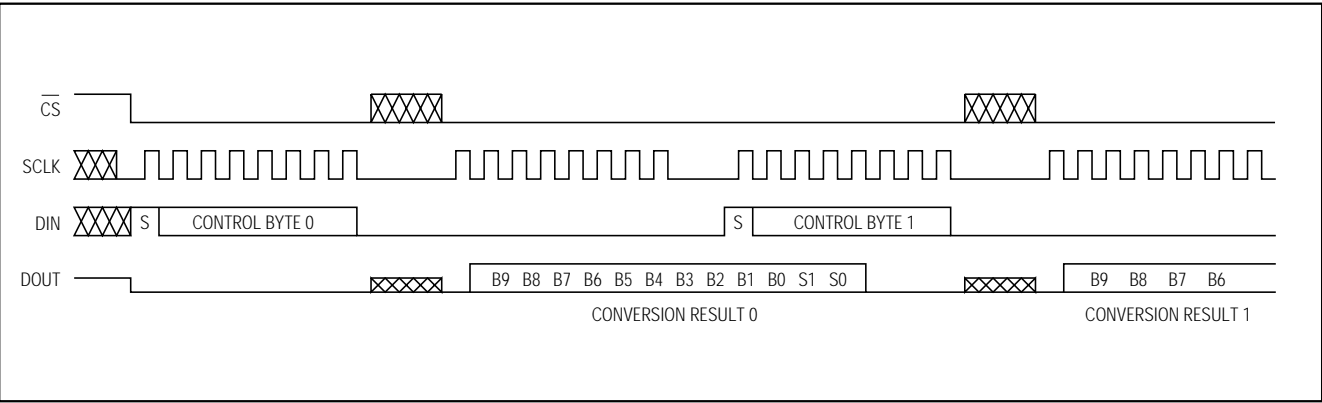


Figure 11b. External Clock Mode, 16 Clocks/Conversion Timing

Low-Power, 8-Channel, Serial 10-Bit ADC

MAX192

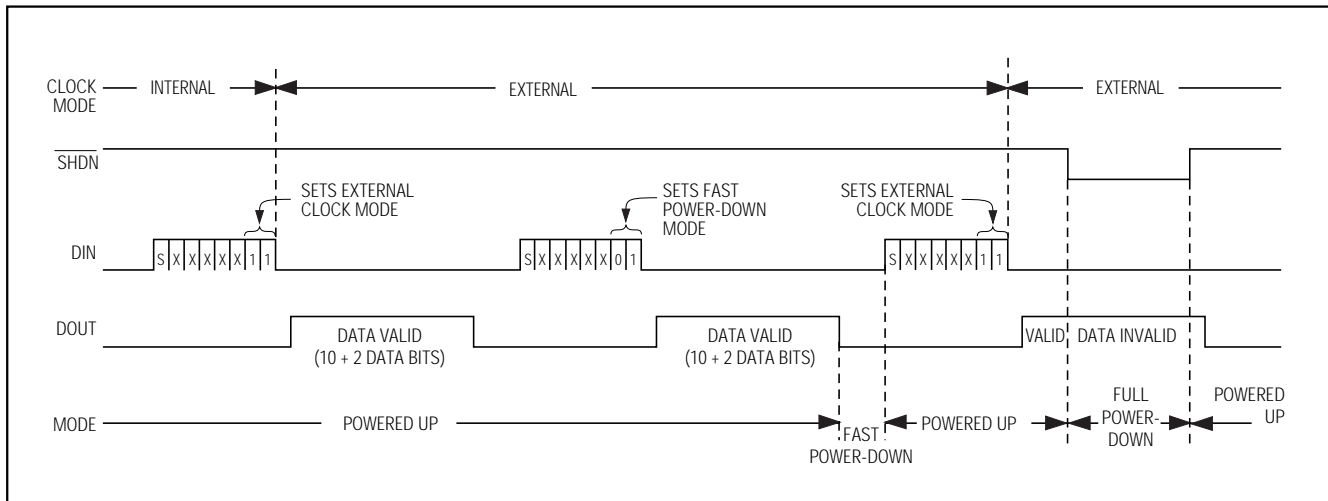


Figure 12a. Timing Diagram Power-Down Modes, External Clock

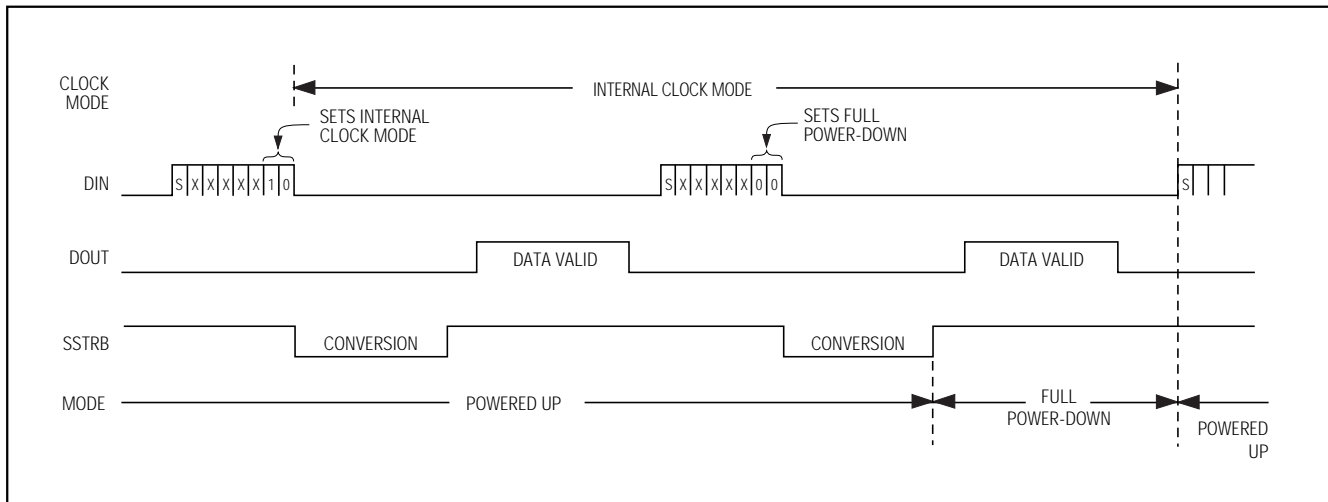


Figure 12b. Timing Diagram Power-Down Modes, Internal Clock

Power-Down Choosing Power-Down Mode

You can save power by placing the converter in a low-current shutdown state between conversions. Select full power-down or fast power-down mode via bits 1 and 0 of the DIN control byte with **SHDN** either high or floating (see Tables 3 and 6). Pull **SHDN** low at any time to shut down the converter completely. **SHDN** overrides bits 1 and 0 of DIN word (see Table 7).

Full power-down mode turns off all chip functions that draw quiescent current, typically reducing I_{DD} to 2 μ A.

Fast power-down mode turns off all circuitry except the bandgap reference. With the fast power-down mode, the supply current is 30 μ A. Power-up time can be shortened to 5 μ s in internal compensation mode.

In both software shutdown modes, the serial interface remains operational, however, the ADC will not convert. Table 5 illustrates how the choice of reference-buffer compensation and power-down mode affects both power-up delay and maximum sample rate.

In external compensation mode, the power-up time is 20ms with a 4.7 μ F compensation capacitor when the capacitor is fully discharged. In fast power-down, you can eliminate start-up time by using low-leakage capaci-

Low-Power, 8-Channel, Serial 10-Bit ADC

Table 5. Worst-Case Power-Up Delay Times

| Reference Buffer | Reference-Buffer Compensation Mode | VREF Capacitor (μF) | Power-Down Mode | Power-Up Delay (sec) | Maximum Sampling Rate (ksps) |
|------------------|------------------------------------|---------------------|-----------------|----------------------|------------------------------|
| Enabled | Internal | | Fast | 5μ | 26 |
| Enabled | Internal | | Full | 300μ | 26 |
| Enabled | External | 4.7 | Fast | See Figure 14c | 133 |
| Enabled | External | 4.7 | Full | See Figure 14c | 133 |
| Disabled | | | Fast | 2μ | 133 |
| Disabled | | | Full | 2μ | 133 |

Table 6. Software Shutdown and Clock Mode

| PD1 | PD0 | Device Mode |
|-----|-----|----------------------|
| 1 | 1 | External Clock Mode |
| 1 | 0 | Internal Clock Mode |
| 0 | 1 | Fast Power-Down Mode |
| 0 | 0 | Full Power-Down Mode |

tors that will not discharge more than 1/2LSB while shut down. In shutdown, the capacitor has to supply the current into the reference (1.5μA typ) and the transient currents at power-up.

Figures 12a and 12b illustrate the various power-down sequences in both external and internal clock modes.

Software Power-Down

Software power-down is activated using bits PD1 and PD0 of the control byte. As shown in Table 6, PD1 and PD0 also specify the clock mode. When software shutdown is asserted, the ADC will continue to operate in the last specified clock mode until the conversion is complete. Then the ADC powers down into a low quiescent-current state. In internal clock mode, the interface remains active and conversion results may be clocked out while the MAX192 has already entered a software power-down.

The first logical 1 on DIN will be interpreted as a start bit, and powers up the MAX192. Following the start bit, the data input word or control byte also determines clock and power-down modes. For example, if the DIN word contains PD1 = 1, then the chip will remain powered up. If PD1 = 0, a power-down will resume after one conversion.

Table 7. Hard-Wired Shutdown and Compensation Mode

| SHDN State | Device Mode | Reference-Buffer Compensation |
|------------|-----------------|-------------------------------|
| 1 | Enabled | Internal Compensation |
| Floating | Enabled | External Compensation |
| 0 | Full Power-Down | N/A |

Hardware Power-Down

The $\overline{\text{SHDN}}$ pin places the converter into the full power-down mode. Unlike with the software shutdown modes, conversion is not completed. It stops coincidentally with $\overline{\text{SHDN}}$ being brought low. There is no power-up delay if an external reference is used and is not shut down. The $\overline{\text{SHDN}}$ pin also selects internal or external reference compensation (see Table 7).

Power-Down Sequencing

The MAX192 auto power-down modes can save considerable power when operating at less than maximum sample rates. The following discussion illustrates the various power-down sequences.

Lowest Power at up to 500 Conversions/Channel/Second

The following examples illustrate two different power-down sequences. Other combinations of clock rates, compensation modes, and power-down modes may give lowest power consumption in other applications.

Figure 14a depicts the MAX192 power consumption for one or eight channel conversions utilizing full power-down mode and internal reference compensation. A 0.01μF bypass capacitor at REFADJ forms an

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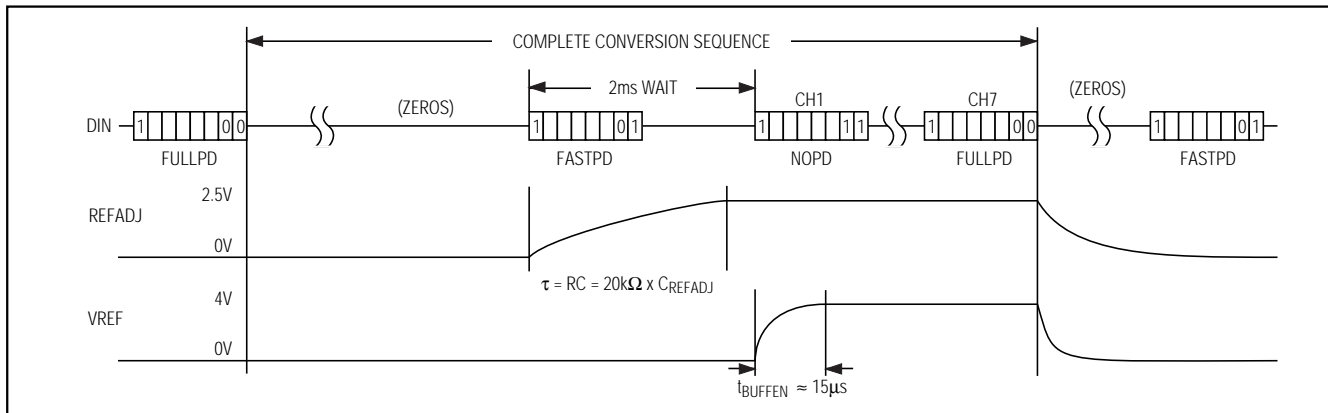


Figure 13. FULLPD/FASTPD Power-Up Sequence

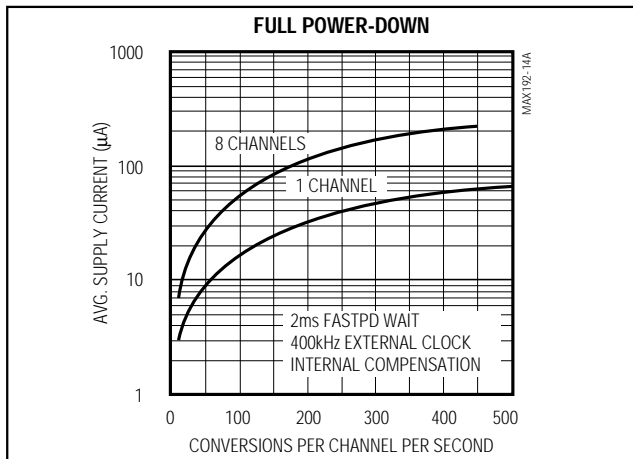


Figure 14a. Supply Current vs. Sample Rate/Second, FULLPD, 400kHz Clock

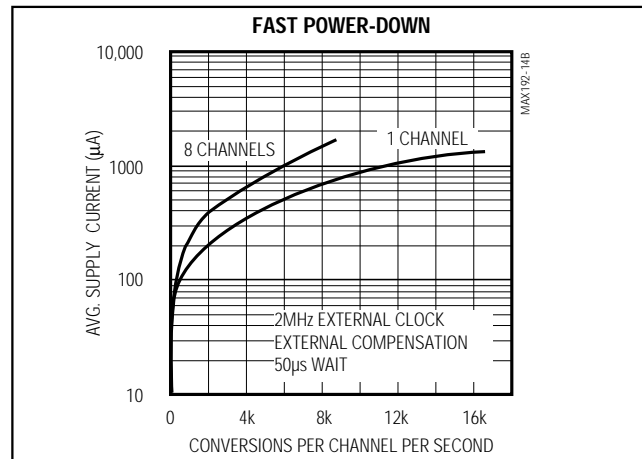


Figure 14b. Supply Current vs. Sample Rate/Second, FASTPD, 2MHz Clock

RC filter with the internal $20k\Omega$ reference resistor with a 0.2ms time constant. To achieve full 10-bit accuracy, 10 time constants or 2ms are required after power-up. Waiting 2ms in FASTPD mode instead of full power-up will reduce the power consumption by a factor of 10 or more. This is achieved by using the sequence shown in Figure 13.

Lowest Power at Higher Throughputs

Figure 14b shows the power consumption with external-reference compensation in fast power-down, with one and eight channels converted. The external $4.7\mu F$ compensation requires a $50\mu s$ wait after power-up, accomplished by 75 idle clocks after a dummy conversion. This circuit combines fast multi-channel conversion with lowest power consumption possible. Full power-down mode may provide increased power savings in applications where the

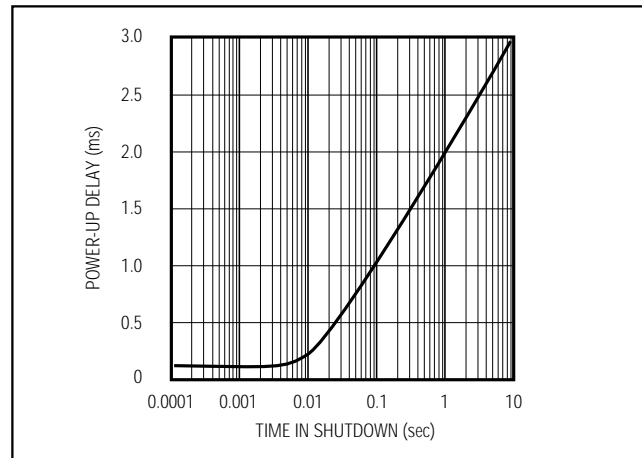


Figure 14c. Typical Power-Up Delay vs. Time in Shutdown

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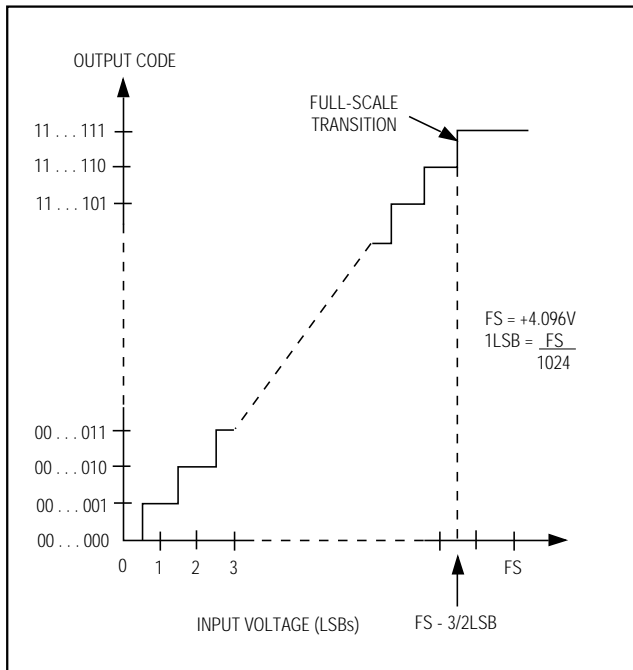


Figure 15. Unipolar Transfer Function, 4.096V = Full Scale

MAX192 is inactive for long periods of time, but where intermittent bursts of high-speed conversions are required.

External and Internal References

The MAX192 can be used with an internal or external reference. Diode D1 shown in the *Typical Operating Circuit* ensures correct start-up. Any standard signal diode can be used. An external reference can either be connected directly at the VREF terminal or at the REFADJ pin.

The MAX192's internally trimmed 2.46V reference is buffered with a gain of 1.678 to scale an external 2.5V reference at REFADJ to 4.096V at VREF.

Internal Reference

The full-scale range of the MAX192 with internal reference is 4.096V with unipolar inputs, and $\pm 2.048\text{V}$ with differential bipolar inputs. The internal reference voltage is adjustable to $\pm 1.5\%$ with the Reference-Adjust Circuit of Figure 17.

External Reference

An external reference can be placed at either the input (REFADJ) or the output (VREF) of the internal buffer amplifier. The REFADJ input impedance is

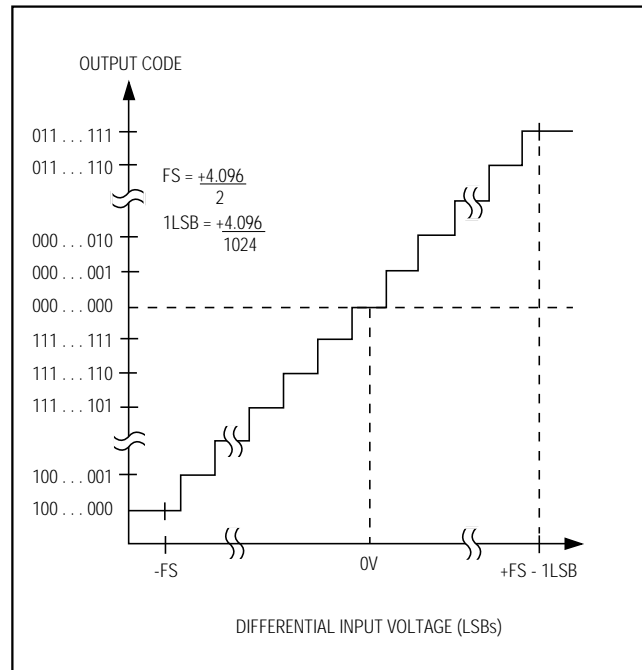


Figure 16. Differential Bipolar Transfer Function, $\pm 4.096\text{V} / 2 = \text{Full Scale}$

typically $20\text{k}\Omega$. At VREF, the input impedance is a minimum of $12\text{k}\Omega$ for DC currents. During conversion, an external reference at VREF must be able to deliver up to $350\mu\text{A}$ DC load current and have an output impedance of 10Ω or less. If the reference has higher output impedance or is noisy, bypass it close to the VREF pin with a $4.7\mu\text{F}$ capacitor.

Using the buffered REFADJ input avoids external buffering of the reference. To use the direct VREF input, disable the internal buffer by tying REFADJ to V_{DD} .

Transfer Function and Gain Adjust

Figure 15 depicts the nominal, unipolar input/output (I/O) transfer function, and Figure 16 shows the differential bipolar input/output transfer function. Code transitions occur halfway between successive integer LSB values. Output coding is binary with $1\text{LSB} = 4.00\text{mV}$ ($4.096\text{V} / 1024$) for unipolar operation and $1\text{LSB} = 4.00\text{mV}$ [$(4.096\text{V} / 2 - -4.096\text{V} / 2) / 1024$] for bipolar operation.

Figure 17, the Reference-Adjust Circuit, shows how to adjust the ADC gain in applications that use the internal reference. The circuit provides $\pm 1.5\%$ ($\pm 15\text{LSBs}$) of gain adjustment range.

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MAX192

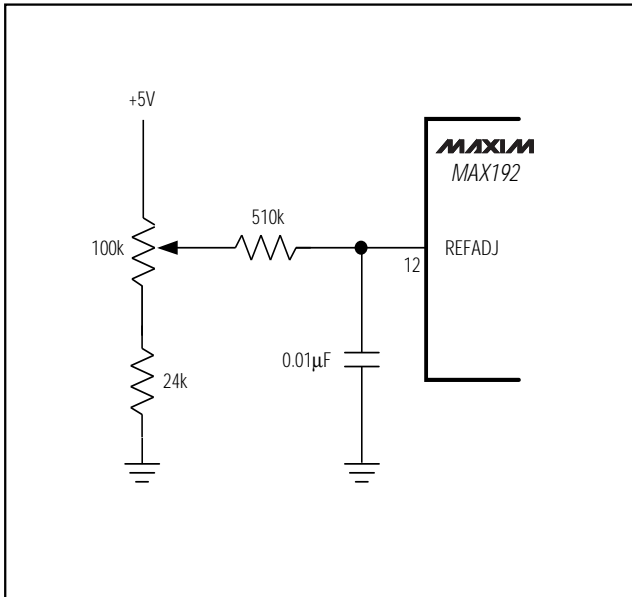


Figure 17. Reference-Adjust Circuit

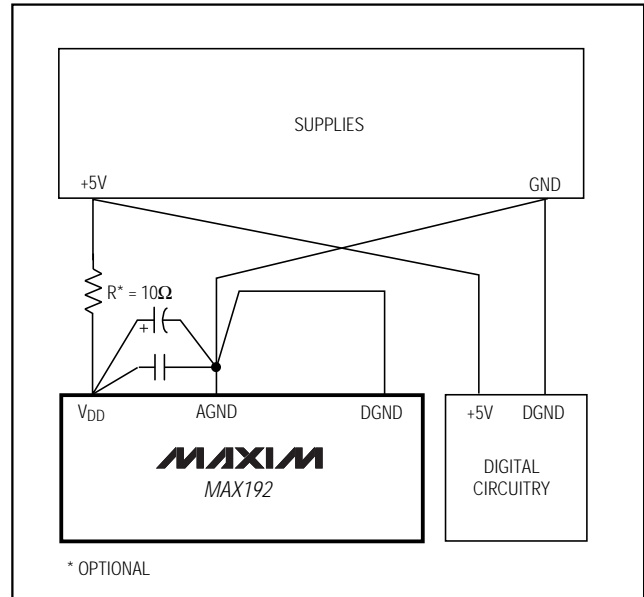


Figure 18. Power-Supply Grounding Connection

Layout, Grounding, Bypassing

For best performance, use printed circuit boards. Wire-wrap boards are not recommended. Board layout should ensure that digital and analog signal lines are separated from each other. Do not run analog and digital (especially clock) lines parallel to one another, or digital lines underneath the ADC package.

Figure 18 shows the recommended system ground connections. A single-point analog ground ("star" ground point) should be established at AGND, separate from the logic ground. All other analog grounds and DGND should be connected to this ground. No other digital system ground should be connected to this single-point analog ground. The ground return to the power supply for this ground should be low impedance and as short as possible for noise-free operation.

High-frequency noise in the V_{DD} power supply may affect the high-speed comparator in the ADC. Bypass these supplies to the single-point analog ground with 0.1µF and 4.7µF bypass capacitors close to the MAX192. Minimize capacitor lead lengths for best supply-noise rejection. If the +5V power supply is very noisy, a 10Ω resistor can be connected as a lowpass filter, as shown in Figure 18.

High-Speed Digital Interfacing

The MAX192 can interface with QSPI at high throughput rates using the circuit in Figure 19. This QSPI circuit can be programmed to do a conversion on each of the eight channels. The result is stored in memory without taxing the CPU since QSPI incorporates its own micro-sequencer.

Figure 20 details the code that sets up QSPI for autonomous operation. In external clock mode, the MAX192 performs a single-ended, unipolar conversion on each of the eight analog input channels. Figure 21 shows the timing associated with the assembly code of Figure 20. The first byte clocked into the MAX192 is the control byte, which triggers the first conversion on CH0. The last two bytes clocked into the MAX192 are all zero, and clock out the results of the CH7 conversion.

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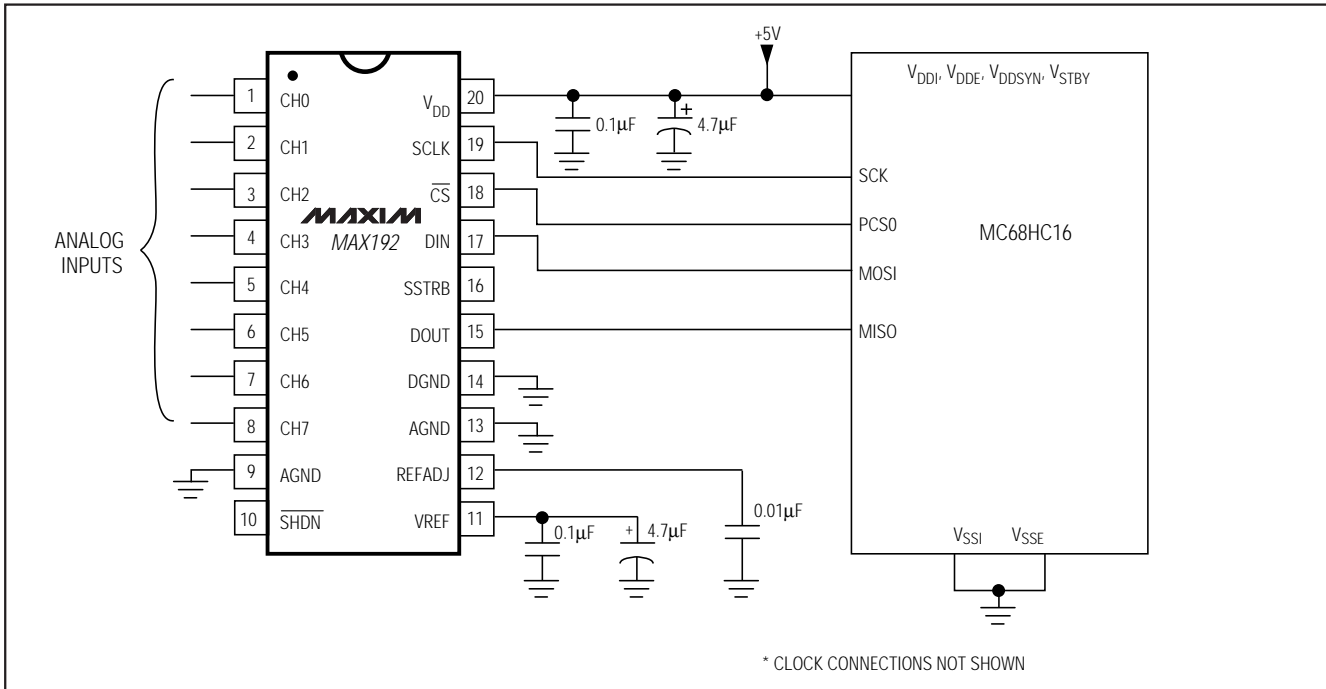


Figure 19. MAX192 QSPI Connection

TMS320 to MAX192 Interface

Figure 22 shows an application circuit to interface the MAX192 to the TMS320 in external clock mode. The timing diagram for this interface circuit is shown in Figure 23.

Use the following steps to initiate a conversion in the MAX192 and to read the results:

- 1) The TMS320 should be configured with CLKX (transmit clock) as an active-high output clock and CLKR (TMS320 receive clock) as an active-high input clock. CLKX and CLKR of the TMS320 are tied together with the SCLK input of the MAX192.
- 2) The MAX192 \overline{CS} is driven low by the XF_ I/O port of the TMS320 to enable data to be clocked into DIN of the MAX192.
- 3) An 8-bit word (1XXXXX11) should be written to the MAX192 to initiate a conversion and place the device into external clock mode. Refer to Table 3 to select the proper XXXXX bit values for your specific application.
- 4) The SSTRB output of the MAX192 is monitored via the FSR input of the TMS320. A falling edge on the SSTRB output indicates that the conversion is in progress and data is ready to be received from the MAX192.
- 5) The TMS320 reads in one data bit on each of the next 16 rising edges of SCLK. These data bits represent the 10-bit conversion result and two sub-LSBs, followed by four trailing bits, which should be ignored.
- 6) Pull \overline{CS} high to disable the MAX192 until the next conversion is initiated.

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```
* Description :
*   This is a shell program for using a stand-alone 68HC16 without any external memory. The internal 1K RAM
*   is put into bank $0F to maintain 68HC11 code compatibility. This program was written with software
*   provided in the Motorola 68HC16 Evaluation Kit.
*
* Roger J.A. Chen, Applications Engineer
* MAXIM Integrated Products
* November 20, 1992
*
*****
INCLUDE 'EQUATES.ASM' ;Equates for common reg addrs
INCLUDE 'ORG00000.ASM' ;initialize reset vector
INCLUDE 'ORG00008.ASM' ;initialize interrupt vectors
ORG $0200 ;start program after interrupt vectors
INCLUDE 'INITSYS.ASM' ;set EK=F,XK=0,YK=0,ZK=0
;set sys clock at 16.78 MHz, COP off
INCLUDE 'INITRAM.ASM' ;turn on internal SRAM at $10000
;set stack (SK=1, SP=03FE)

MAIN:
JSR INITQSPI
MAINLOOP:
JSR READ192
WAIT:
LDAA SPSR
ANDA #$80
BEQ WAIT ;wait for QSPI to finish
BRA MAINLOOP
ENDPROGRAM:

INITQSPI:

;This routine sets up the QSPI microsequencer to operate on its own.
;The sequencer will read all eight channels of a MAX192 each time
;it is triggered. The A/D converter results will be left in the
;receive data RAM. Each 16 bit receive data RAM location will
;have a leading zero, 10 + 2 bits of conversion result and three zeros.
;
;Receive RAM Bits 15 14 13 12 11 10 09 08 07 06 05 04 03 02 01 00
;A/D Result 0 MSB LSB 0 0 0
***** Initialize the QSPI Registers *****
PSHA
PSHB
LDAA #%01111000
STAA QPDR ;idle state for PCS0-3 = high
LDAA #%01111011
STAA QPAR ;assign port D to be QSPI
LDAA #%01111110
STAA QDDR ;only MISO is an input
LDD #$8008
STD SPCR0 ;master mode,16 bits/transfer,
;CPOL=CPHA=0,1MHz Ser Clock

LDD #$0000
STD SPCR1 ;set delay between PCS0 and SCK,
;set delay between transfers
```

Figure 20. MAX192 Assembly-Code Listing

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```

LDD  #$0800
STD  SPCR2          ;set ENDQP to $8 for 9 transfers
***** Initialize QSPI Command RAM *****

LDAA  #$80          ;CONT=1,BITSE=0,DT=0,DSCK=0,PCS0=ACTIVE
STAA  $FD40          ;store first byte in COMMAND RAM
LDAA  #$C0          ;CONT=1,BITSE=1,DT=0,DSCK=0,PCS0=ACTIVE
STAA  $FD41
STAA  $FD42
STAA  $FD43
STAA  $FD44
STAA  $FD45
STAA  $FD46
STAA  $FD47
LDAA  #$40          ;CONT=0,BITSE=1,DT=0,DSCK=0,PCS0=ACTIVE
STAA  $FD48
***** Initialize QSPI Transmit RAM *****

LDD  #$008F          STD  $FD20
LDD  #$00CF          STD  $FD22
LDD  #$009F          STD  $FD24
LDD  #$00DF          STD  $FD26
LDD  #$00AF          STD  $FD28
LDD  #$00EF          STD  $FD2A
LDD  #$00BF          STD  $FD2C
LDD  #$00FF          STD  $FD2E
LDD  #$0000          STD  $FD30

PULB
PULA
RTS

READ192:
;This routine triggers the QSPI microsequencer to autonomously
;trigger conversions on all 8 channels of the MAX192. Each
;conversion result is stored in the receive data RAM.
PSHA
LDAA  #$80
ORAA  SPCR1
STAA  SPCR1          ;just set SPE
PULA
RTS

***** Interrupts/Exceptions *****

BDM: BGND          ;exception vectors point here
                  ;and put the user in background debug mode

```

Figure 20. MAX192 Assembly-Code Listing (continued)

Low-Power, 8-Channel, Serial 10-Bit ADC

MAX192

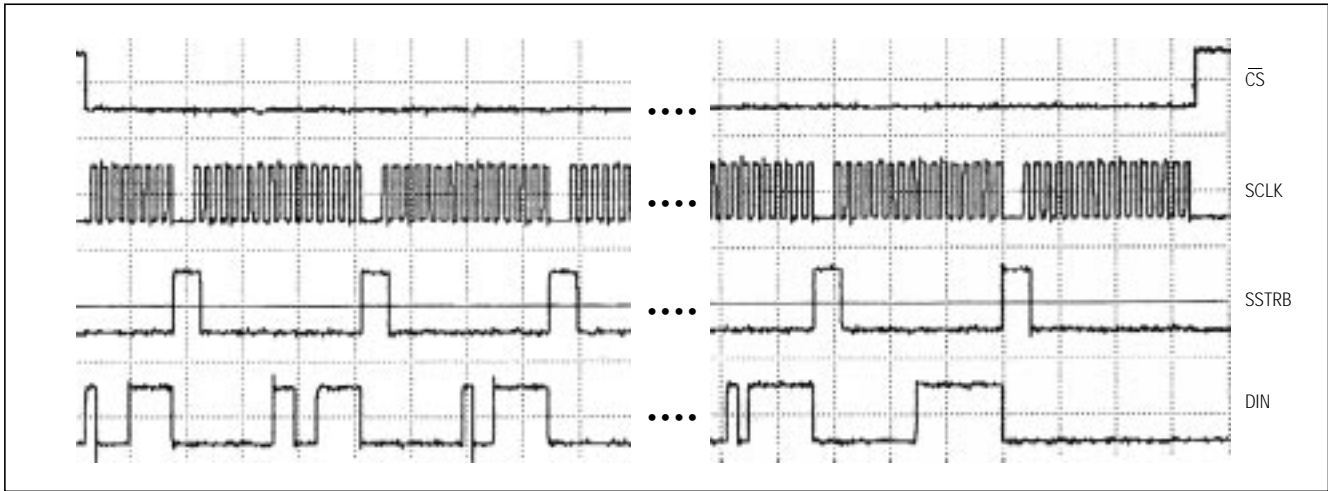


Figure 21. QSPI Assembly-Code Timing

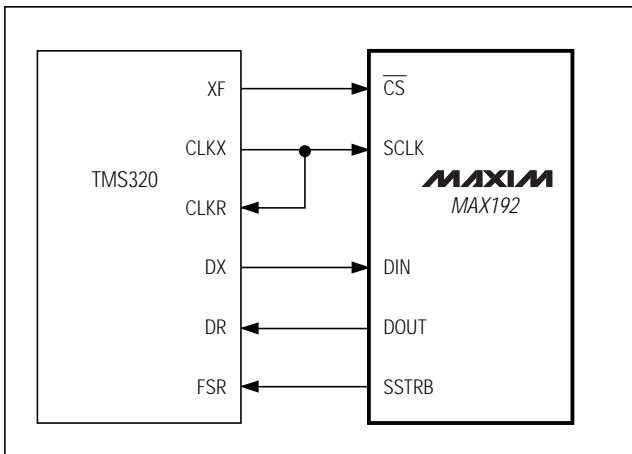


Figure 22. MAX192 to TMS320 Serial Interface

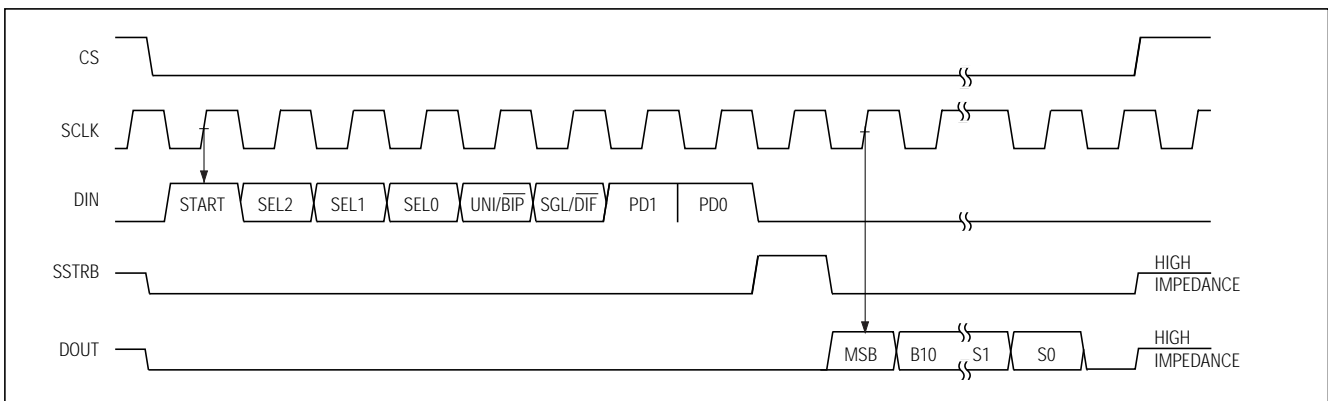
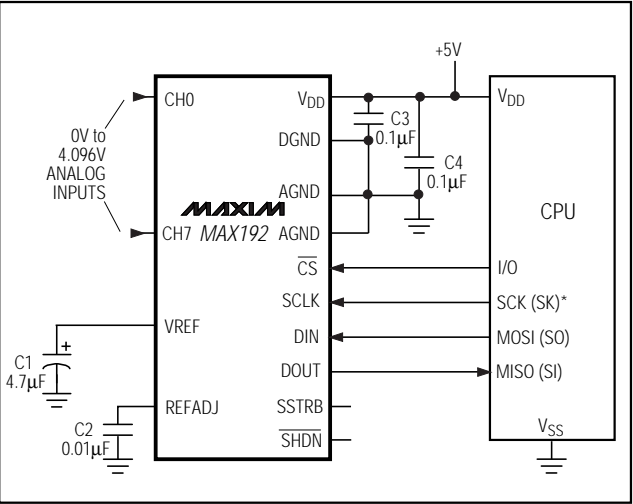


Figure 23. TMS320 Serial-Interface Timing Diagram

Low-Power, 8-Channel, Serial 10-Bit ADC

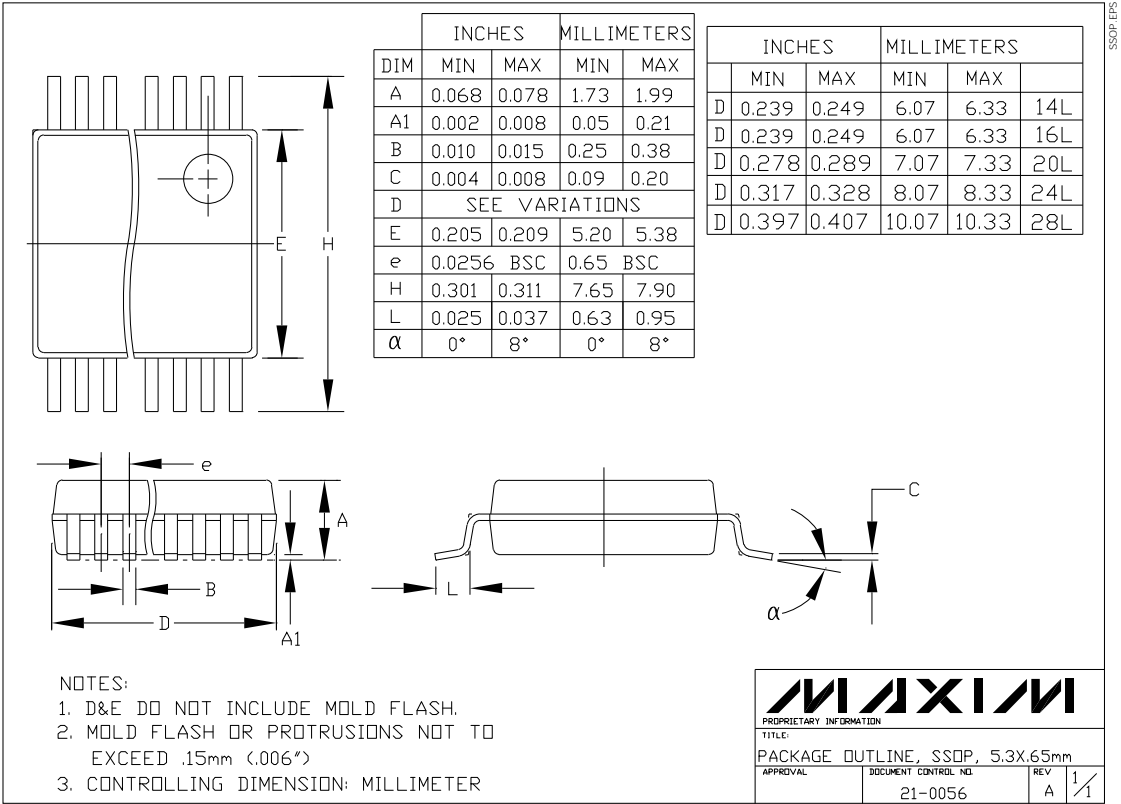
Typical Operating Circuit



Chip Information

TRANSISTOR COUNT: 2278

Package Information



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