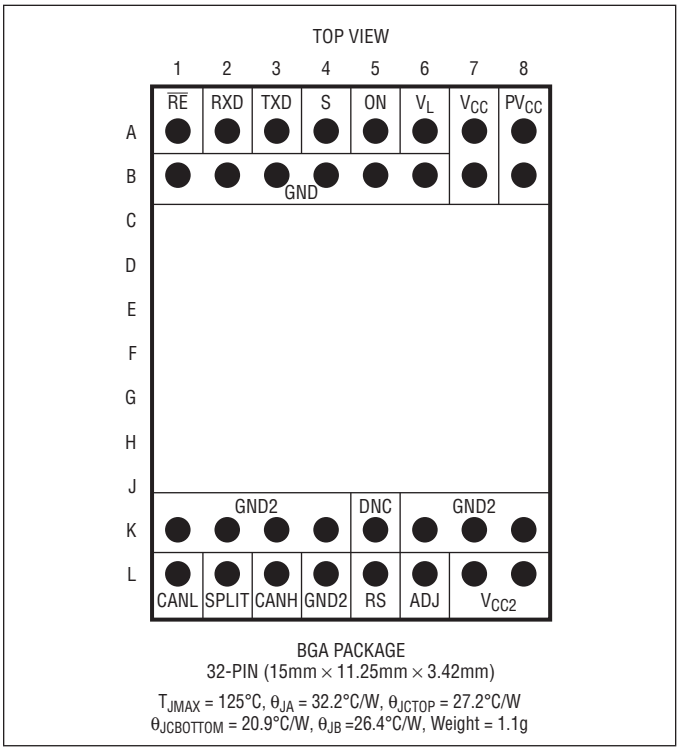
ABSOLUTE MAXIMUM RATINGS

(Note 1)

V_{CC} to GND ..... –0.3V to 6V
PV_{CC} to GND ..... –0.3V to 6V
V_L to GND ..... –0.3V to 6V
V_{CC2} to GND2..... –0.3V to 6V
Signal Voltages (ON, S, $\overline{RE}$, RXD, TXD)
to GND .....–0.3V to V_L +0.3V
Interface I/O (CANH, CANL, SPLIT) to GND2 .....±60V
Interface I/O to Interface I/O ..... ±120V
V_{CC2}, ADJ, RS to GND2..... –0.3V to 6V
Operating Temperature Range (Note 4)
LTM2889C ..... 0°C to 70°C
LTM2889I .....–40°C to 85°C
LTM2889H..... –40°C to 125°C
Maximum Internal Operating Temperature..... 125°C
Storage Temperature Range ..... –55°C to 125°C
Peak Reflow Temperature (Soldering, 10 sec)..... 245°C

PIN CONFIGURATION



BGA PACKAGE
32-PIN (15mm × 11.25mm × 3.42mm)

T_{JMAX} = 125°C, θ_{JA} = 32.2°C/W, θ_{JCTOP} = 27.2°C/W
$\theta_{JCBOTTOM}$ = 20.9°C/W, θ_{JB} =26.4°C/W, Weight = 1.1g

PRODUCT SELECTION GUIDE

LTM2889 I Y –3 #PBF

LEAD FREE DESIGNATOR
PBF = Lead Free

INPUT VOLTAGE RANGE
3 = 3V to 3.6V
5 = 4.5V to 5.5V

PACKAGE TYPE
Y = Ball Grid Array (BGA)

TEMPERATURE GRADE
C = Commercial Temperature Range (0°C to 70°C)
I = Industrial Temperature Range (–40°C to 85°C)
H = Automotive Temperature Range (–40°C to 125°C)

PRODUCT PART NUMBER

ORDER INFORMATION

http://www.linear.com/product/LTM2889#orderinfo

PART NUMBER	PAD OR BALL FINISH	PART MARKING		PACKAGE TYPE	MSL RATING	INPUT VOLTAGE RANGE	TEMPERATURE RANGE
		DEVICE	FINISH CODE				
LTM2889CY-3#PBF	SAC305 (RoHS)	LTM2889Y-3	e1	32-Lead BGA	3	3V to 3.6V	0°C to 70°C
LTM2889IY-3#PBF						3V to 3.6V	–40°C to 85°C
LTM2889HY-3#PBF						3V to 3.6V	–40°C to 125°C
LTM2889CY-5#PBF		LTM2889Y-5				4.5V to 5.5V	0°C to 70°C
LTM2889IY-5#PBF						4.5V to 5.5V	–40°C to 85°C
LTM2889HY-5#PBF						4.5V to 5.5V	–40°C to 125°C

- Device temperature grade is indicated by a label on the shipping container.
- Pad or ball finish code is per IPC/JEDEC J-STD-609.
- Terminal Finish Part Marking: www.linear.com/leadfree
- This product is not recommended for second side reflow. For more information, go to www.linear.com/BGA-assy
- Recommended BGA PCB Assembly and Manufacturing Procedures: www.linear.com/BGA-assy
- BGA Package and Tray Drawings: www.linear.com/packaging
- This product is moisture sensitive. For more information, go to: www.linear.com/BGA-assy

ELECTRICAL CHARACTERISTICS

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. Unless otherwise noted, the following conditions apply: PV_{CC} = V_{CC} = 3.3V for the LTM2889-3, PV_{CC} = V_{CC} = 5V for the LTM2889-5, V_L = 3.3V, GND = GND2 = S = $\overline{RE}$ = RS = 0V, ON = V_L. Figure 10 applies for V_{CC2} = 3.3V; otherwise ADJ is floating. Figure 1 applies with R_L = 60Ω and dominant mode measurements are taken prior to TXD dominant timeout ($t < t_{TOTXD}$). (Note 2)

SYMBOL	PARAMETER	CONDITIONS			MIN	TYP	MAX	UNITS
Power Supplies								
V_{CC}	Supply Voltage			●	3.0		5.5	V
I_{CC}	Supply Current	OFF: ON = 0V		●		0	10	µA
		ON = V_L		●		3.1	5	mA
PV_{CC}	Supply Voltage, Isolated Power Converter		LTM2889-3	●	3.0	3.3	3.6	V
			LTM2889-5	●	4.5	5.0	5.5	V
PI_{CC}	Supply Current, Isolated Power Converter, (V_{CC2} External Load Current I_{LOAD} = 0)	OFF: ON = 0V		●		0	10	µA
		Recessive: ON = V_L, TXD = V_L and/or S = V_L	LTM2889-3	●		34	60	mA
			LTM2889-5	●		32	50	mA
		Dominant: ON = V_L, TXD = S = 0	LTM2889-3	●		140	225	mA
			LTM2889-5	●		94	130	mA
V_L	Logic Supply Voltage			●	1.62	3.3	5.5	V
I_L	Logic Supply Current	OFF: ON = 0V, TXD = V_L		●		0	10	µA
		Recessive: ON = V_L, TXD = V_L		●		0	10	µA
		Dominant: ON = V_L, TXD = S = 0V		●		6	50	µA
V_{CC2}	Regulated V_{CC2} Output Voltage to GND2	No Load, TXD = V_L		●	4.75	5.0	5.25	V
		I_{LOAD} = 100mA, TXD = V_L	LTM2889-3	●	4.75	5.0	5.25	V
		I_{LOAD} = 150mA, TXD = V_L	LTM2889-5	●	4.75	5.0	5.25	V
$V_{CC2-3.3V}$	Regulated V_{CC2} Output Voltage to GND2, 3.3V Output	No Load, (Fig. 10)		●	3.1	3.3	3.5	V
		I_{LOAD} = 100mA, (Fig. 10)	LTM2889-3	●	3.0	3.3	3.5	V
		I_{LOAD} = 150mA, (Fig. 10)	LTM2889-5	●	3.0	3.3	3.5	V
	V_{CC2} Short Circuit Current	V_{CC2} = 0V, TXD = V_L				200		mA

ELECTRICAL CHARACTERISTICS

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. Unless otherwise noted, the following conditions apply: PV_{CC} = V_{CC} = 3.3V for the LTM2889-3, PV_{CC} = V_{CC} = 5V for the LTM2889-5, V_L = 3.3V, GND = GND2 = S = $\overline{RE}$ = RS = 0V, ON = V_L. Figure 10 applies for V_{CC2} = 3.3V; otherwise ADJ is floating. Figure 1 applies with R_L = 60Ω and dominant mode measurements are taken prior to TXD dominant timeout (t < t_{TOTXD}). (Note 2)

SYMBOL	PARAMETER		CONDITIONS			MIN	TYP	MAX	UNITS
Control Inputs S, ON, $\overline{RE}$:									
V_{IH}	HIGH-level Input Voltage		$V_L \geq 2.35V$		●	0.7 • V_L		V_L + 0.3	V
			1.62V ≤ V_L < 2.35V		●	0.75 • V_L		V_L + 0.3	V
V_{IL}	LOW-level Input Voltage		$V_L \geq 2.35V$		●	–0.3		0.3 • V_L	V
			1.62V ≤ V_L < 2.35V		●	–0.3		0.25 • V_L	V
I_{IH}	HIGH-level Input Current		ON = S = $\overline{RE}$ = V_L		●		11	25	µA
I_{IL}	LOW-level Input Current		ON = S = $\overline{RE}$ = 0V		●			±1	µA
CAN Transmit Data Input Pin TXD									
V_{IH}	HIGH-level Input Voltage		$V_L \geq 2.35V$		●	0.7 • V_L		V_L + 0.3	V
			1.62V ≤ V_L < 2.35V		●	0.75 • V_L		V_L + 0.3	V
V_{IL}	LOW-level Input Voltage		$V_L \geq 2.35V$		●	–0.3		0.3 • V_L	V
			1.62V ≤ V_L < 2.35V		●	–0.3		0.25 • V_L	V
I_{IH}	HIGH-level Input Current		TXD = V_L		●			±5	µA
I_{IL}	LOW-level Input Current		TXD = 0V		●	–50		–2	µA
C_{IN}	Input Capacitance		(Note 6)				5		pF
CAN Receive Data Output Pin RXD									
I_{OH}	HIGH-level Output Current		RXD = V_L – 0.4V	3V ≤ V_L ≤ 5.5V	●			–4	mA
				1.62V ≤ V_L < 3V	●			–1	mA
I_{OL}	LOW-level Output Current		RXD = 0.4V, Bus Dominant	3V ≤ V_L ≤ 5.5V	●	4			mA
				1.62V ≤ V_L < 3V	●	1			mA
Bus Driver Pins CANH, CANL									
$V_{O(D)}$	Bus Output Voltage (Dominant) to GND2	CANH	TXD = 0V, t< t_{TOTXD}	V_{CC2} = 5V	●	2.75	3.6	4.5	V
				V_{CC2} = 3.3V	●	2.15	2.9	3.3	V
		CANL	TXD = 0V, t< t_{TOTXD}	V_{CC2} = 5V	●	0.5	1.4	2.25	V
				V_{CC2} = 3.3V	●	0.5	0.9	1.65	V
$V_{O(R)}$	Bus Output Voltage (Recessive) to GND2		V_{CC2} = 5V, No Load (Figure 1)		●	2	2.5	3	V
			V_{CC2} = 3.3V, No Load (Figure 1)		●	1.45	1.95	2.45	V
$V_{OD(D)}$	Differential Output Voltage (Dominant)		R_L = 50Ω to 65Ω (Figure 1)		●	1.5	2.2	3	V
$V_{OD(R)}$	Differential Output Voltage (Recessive)		No Load (Figure 1)		●	–500	0	50	mV
$V_{OC(D)}$	Common Mode Output Voltage (Dominant) to GND2		V_{CC2} = 5V, (Figure 1)		●	2	2.5	3	V
			V_{CC2} = 3.3V, (Figure 1)		●	1.45	1.95	2.45	V
$I_{OS(D)}$	Bus Output Short-Circuit Current (Dominant)	CANH	CANH = 0V to GND2		●	–100	–75		mA
		CANH	CANH = ±60V to GND2		●	–100		3	mA
		CANL	CANL = 5V to GND2		●		75	110	mA
		CANL	CANL = ±60V to GND2		●	–3		100	mA

ELECTRICAL CHARACTERISTICS

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. Unless otherwise noted, the following conditions apply: PV_{CC} = V_{CC} = 3.3V for the LTM2889-3, PV_{CC} = V_{CC} = 5V for the LTM2889-5, V_L = 3.3V, GND = GND2 = S = $\overline{RE}$ = RS = 0V, ON = V_L. Figure 10 applies for V_{CC2} = 3.3V; otherwise ADJ is floating. Figure 1 applies with R_L = 60Ω and dominant mode measurements are taken prior to TXD dominant timeout ($t < t_{TOTXD}$). (Note 2)

SYMBOL	PARAMETER	CONDITIONS			MIN	TYP	MAX	UNITS
Bus Receiver Pins CANH, CANL								
V_{CM}	Bus Common Mode Voltage to GND2 = (CANH + CANL)/2 for Data Reception	V_{CC2} = 5V		●			±36	V
		V_{CC2} = 3.3V		●			±25	V
V_{TH}^+	Bus Input Differential Threshold Voltage (Positive-Going)	V_{CC2} = 5V, –36V ≤ V_{CM} ≤ 36V		●		775	900	mV
		V_{CC2} = 3.3V, –25V ≤ V_{CM} ≤ 25V		●		775	900	mV
V_{TH}^-	Bus Input Differential Threshold Voltage (Negative-Going)	V_{CC2} = 5V, –36V ≤ V_{CM} ≤ 36V		●	500	625		mV
		V_{CC2} = 3.3V, –25V ≤ V_{CM} ≤ 25V		●	500	625		mV
ΔV_{TH}	Bus Input Differential Hysteresis Voltage	V_{CC2} = 5V, –36V ≤ V_{CM} ≤ 36V				150		mV
		V_{CC2} = 3.3V, –25V ≤ V_{CM} ≤ 25V				150		mV
R_{IN}	Input Resistance (CANH and CANL) to GND2	R_{IN} = ΔV/ΔI; ΔI = ±20µA		●	25	40	50	kΩ
R_{ID}	Differential Input Resistance	R_{IN} = ΔV/ΔI; ΔI = ±20µA		●	50	80	100	kΩ
ΔR_{IN}	Input Resistance Matching	R_{IN} (CANH) to R_{IN} (CANL)					±1	%
C_{IH}	Input Capacitance to GND2 (CANH)	(Note 6)				32		pF
C_{IL}	Input Capacitance to GND2 (CANL)	(Note 6)				8		pF
C_{ID}	Differential Input Capacitance	(Note 6)				8.4		pF
I_{BL}	Bus Leakage Current (V_{CC2} = 0V) (I-Grade)	CANH = CANL = 5V, T ≤ 85°C		●			±10	µA
	Bus Leakage Current (V_{CC2} = 0V) (H-Grade)	CANH = CANL = 5V, T ≤ 125°C		●			±40	µA
Bus Common Mode Stabilization Pin SPLIT								
V_{O_SPLIT}	SPLIT Output Voltage to GND2	–500µA ≤ I(SPLIT) ≤ 500µA	V_{CC2} = 5V	●	1.5	2.5	3.5	V
			V_{CC2} = 3.3V	●	0.9	1.9	2.9	V
I_{OS_SPLIT}	SPLIT Short-Circuit Current	–60V ≤ SPLIT ≤ 60V to GND2		●			±3	mA
Logic/Slew Control Input RS								
V_{IH_RS}	High Level Input Voltage to GND2			●	0.9 • V_{CC2}			V
V_{IL_RS}	Low Level Input Voltage to GND2			●		0.5 • V_{CC2}		V
I_{IN_RS}	Logic Input Current	0 ≤ RS ≤ V_{CC2}		●	–170	0	10	µA
ESD (HBM) (Note 3)								
	Isolation Boundary	GND2 to GND				±10		kV
	CANH, CANL, SPLIT	Referenced to GND2 or V_{CC2}				±25		kV
	All Other Pins	Referenced to GND, GND2, or V_{CC2}				±4		kV

SWITCHING CHARACTERISTICS

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. Unless otherwise noted, the following conditions apply: PV_{CC} = V_{CC} = 3.3V for the LTM2883-3, PV_{CC} = V_{CC} = 5V for the LTM2883-5, V_L = 3.3V, GND = GND2 = S = $\overline{RE}$ = RS = 0V, ON = V_L. Figure 2 applies with R_L = 60Ω, C_L = 100pF, RSL = 0Ω. Figure 10 applies for V_{CC2} = 3.3V; otherwise ADJ is floating.

SYMBOL	PARAMETER	CONDITIONS			MIN	TYP	MAX	UNITS
Transceiver Timing								
f_{MAX}	Maximum Data Rate			●	4			Mbps
t_{PTXBD}	TXD to Bus Dominant Propagation Delay	(Figure 3)	V_{CC2} = 3.3V	●	55	105	165	ns
			V_{CC2} = 5V	●	50	100	150	ns
t_{PTXBR}	TXD to Bus Recessive Propagation Delay	(Figure 3)	V_{CC2} = 3.3V	●	100	145	205	ns
			V_{CC2} = 5V	●	80	115	155	ns
t_{PTXBDS}	TXD to Bus Dominant Propagation Delay, Slow Slew	RSL = 200k (Figure 3)	V_{CC2} = 3.3V	●	200	565	1255	ns
			V_{CC2} = 5V	●	220	585	1225	ns
t_{PTXBRS}	TXD to Bus Recessive Propagation Delay, Slow Slew	RSL = 200k (Figure 3)	V_{CC2} = 3.3V	●	420	985	2035	ns
			V_{CC2} = 5V	●	490	1065	2245	ns
t_{PBDRX}	Bus Dominant to RXD Propagation Delay	(Figure 3)		●	40	65	100	ns
t_{PBRRX}	Bus Recessive to RXD Propagation Delay	(Figure 3)		●	45	70	115	ns
t_{PTXRXD}	TXD to RXD Dominant Propagation Delay	(Figure 3)	V_{CC2} = 3.3V	●	120	170	240	ns
			V_{CC2} = 5V	●	110	165	225	ns
t_{PTXRXR}	TXD to RXD Recessive Propagation Delay	(Figure 3)	V_{CC2} = 3.3V	●	160	215	275	ns
			V_{CC2} = 5V	●	140	185	245	ns
$t_{PTXRXDS}$	TXD to RXD Dominant Propagation Delay, Slow Slew	RSL = 200k (Figure 3)	V_{CC2} = 3.3V	●	210	550	1170	ns
			V_{CC2} = 5V	●	240	580	1150	ns
$t_{PTXRXRS}$	TXD to RXD Recessive Propagation Delay, Slow Slew	RSL = 200k (Figure 3)	V_{CC2} = 3.3V	●	450	990	1960	ns
			V_{CC2} = 5V	●	500	1070	2150	ns
t_{TOTXD}	TXD Timeout Time	(Figure 4)		●	0.5	2	4	ms
$t_{BIT(RXD),2M}$	Receiver Output Recessive Bit Time, 2Mbps, Loop Delay Symmetry	(Figure 8)	V_{CC2} = 3.3V	●	400	455	550	ns
			V_{CC2} = 5V	●	400	475	550	ns
$t_{BIT(RXD),4M}$	Receiver Output Recessive Bit Time, 4Mbps	(Figure 8)	V_{CC2} = 5V	●	200	225	275	ns
t_{ZLR}	Receiver Output Enable Time	(Figure 5)		●			20	ns
t_{LZR}	Receiver Output Disable Time	(Figure 5)		●			30	ns
t_{ENRSRX}	RXD Enable from Shutdown Time	(Figure 6)		●			40	µs
t_{ENRSTX}	TXD Enable from Shutdown TIme	(Figure 7) (Note 5)		●			40	µs
t_{SHDNRX}	Time to Shutdown, Receiver	(Figure 6)		●			3	µs
t_{SHDNTX}	Time to Shutdown, Transmitter	(Figure 7)		●			250	ns
Power Supply Generator								
t_{ENPS}	V_{CC2} Supply Start-Up Time	No load, ON ↑, V_{CC2} to 4.5V		●		2.3	5	ms
Transmitter Drive Symmetry (Common Mode Voltage Fluctuation)								
V_{SYM}	Driver Symmetry (CANH + CANL – $2V_{O(R)}$) (Dynamic Peak Measurement)	R_L = 60Ω/Tol. < 1%, C_{SPLIT} = 4.7nF/5%, f_{TXD} = 250kHz, Input Impedance of Oscilloscope: ≤ 20pF/≥1MΩ (Figure 2)		●			±500	mV

ISOLATION CHARACTERISTICS T_A = 25°C

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{ISO}	Rated Dielectric Insulation Voltage	1 Second (Notes 7, 8, 9)	3000			V_{RMS}
		1 Minute, Derived from 1 Second Test (Note 9)	2500			V_{RMS}
	Common Mode Transient Immunity	LTM2889-3 V_{CC} = 3.3V, LTM2889-5 V_{CC} = 5.0V, V_L = ON = 3.3V, ΔV(GND2-GND) = 1kV, Δt = 33ns (Note 3)	30	50		kV/µs
V_{IORM}	Maximum Working Insulation Voltage	(Notes 3,10)	560 400			V_{PEAK}, V_{DC} V_{RMS}
	Partial Discharge	V_{PD} = 1060 V_{PEAK} (Note 7)			5	pC
CTI	Comparative Tracking Index	IEC 60112 (Note 3)	600			V_{RMS}
	Depth of Erosion	IEC 60112 (Note 3)		0.017		mm
DTI	Distance Through Insulation	(Note 3)		0.06		mm
	Input to Output Resistance	(Notes 3, 7)	10^9			Ω
	Input to Output Capacitance	(Notes 3, 7)		6		pF
	Creepage Distance	(Notes 3, 7)		9.5		mm

Note 1. Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2. All currents into device pins are positive; all currents out of device pins are negative. All voltages are referenced to device ground unless otherwise specified.

Note 3. Not tested in production.

Note 4. This module includes overtemperature protection that is intended to protect the device during momentary overload conditions. Junction temperature exceeds 150°C when overtemperature protection is active. Continuous operation above the specified maximum operating temperature may result in device degradation or failure.

Note 5. TXD must make a high to low transition after this time to assert a bus dominant state.

Note 6. Pin capacitance given for reference only and is not tested in production.

Note 7. Device considered a 2-terminal device. Pin group A1 through B8 shorted together and pin group K1 through L8 shorted together.

Note 8. The Rated Dielectric Insulation Voltage should not be interpreted as a continuous voltage rating.

Note 9. In accordance with UL1577, each device is proof tested for the 2500V_{RMS} rating by applying an insulation test voltage of 3000V_{RMS} for 1 second.

Note 10. Maximum Working Insulation Voltage is for continuous or repeated voltage applied across the isolation boundary. Refer also to relevant equipment level safety specifications which may reduce V_{IORM} depending on application conditions.

TEST CIRCUITS

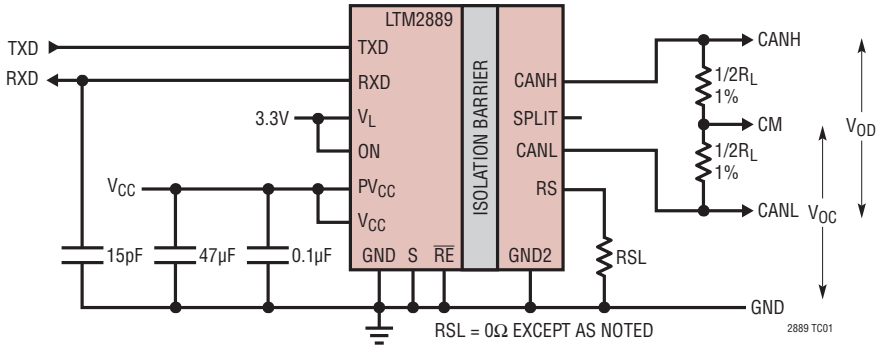


Figure 1. Electrical Characteristic Measurements of Bus Pins CANH, CANL

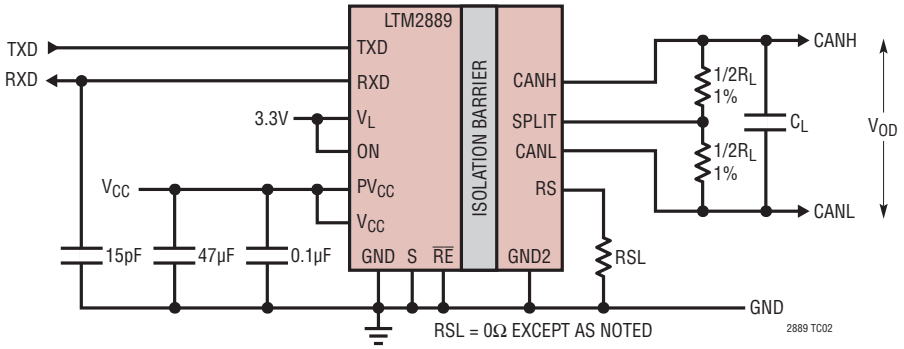


Figure 2. All Bus Pin Switching Characteristic Measurements Except Receiver Enable/Disable Times

TEST CIRCUITS

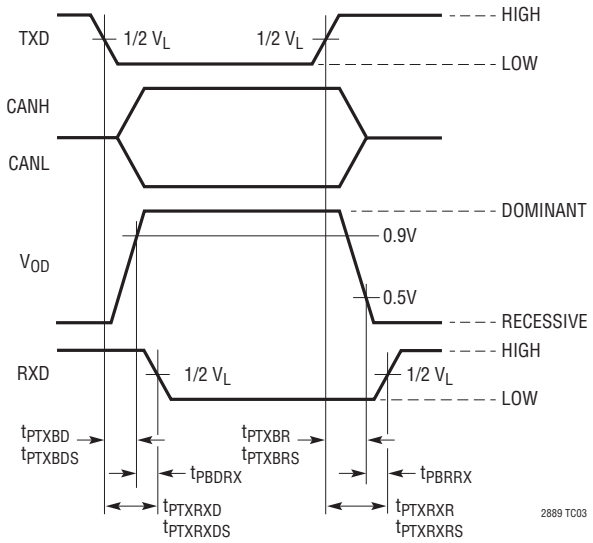


Figure 3. CAN Transceiver Data Propagation Timing Diagram

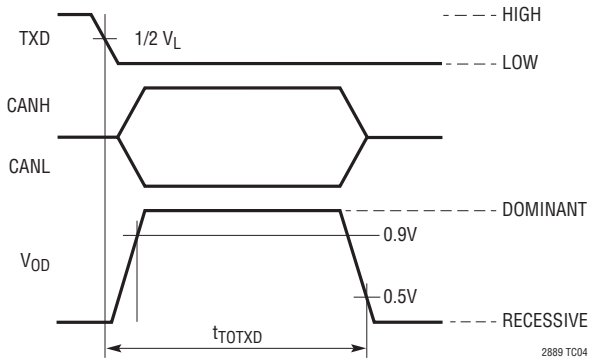


Figure 4. TXD Dominant Timeout Time

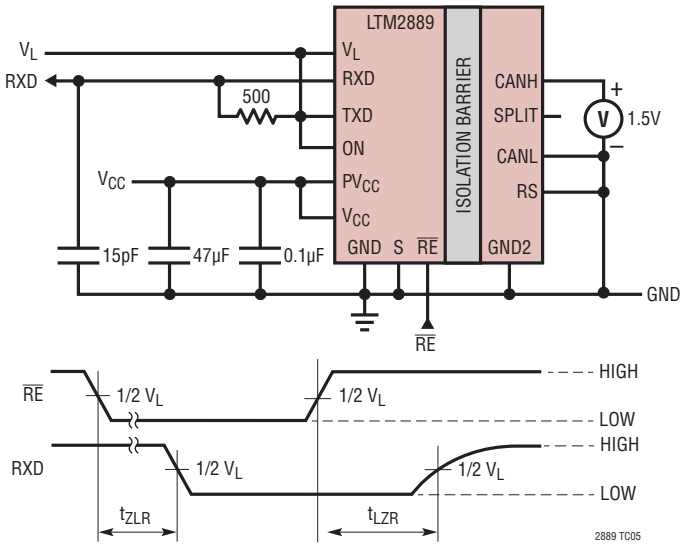


Figure 5. Receiver Output Enable and Disable Timing

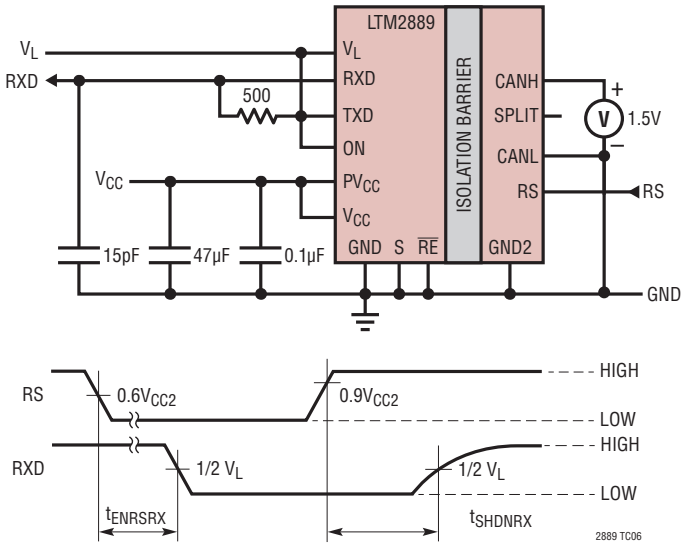


Figure 6. RXD Enable and Disable Timing from Shutdown

TEST CIRCUITS

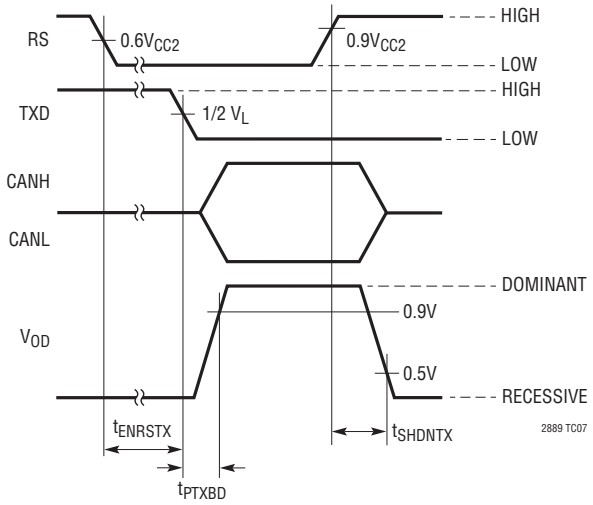


Figure 7. TXD Enable and Disable Timing from Shutdown

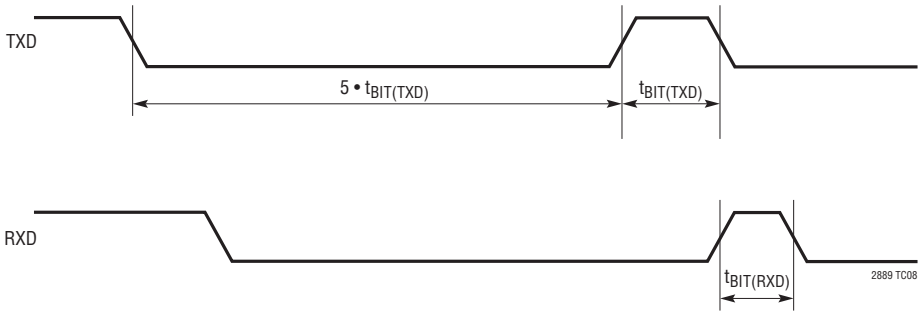
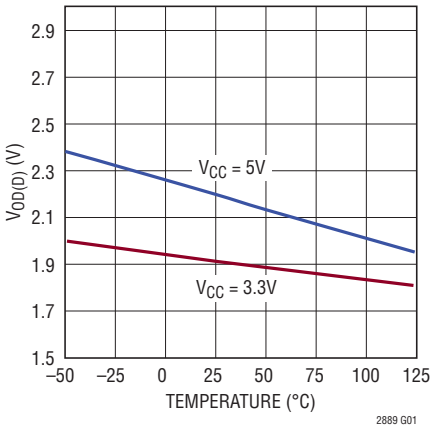


Figure 8. Loop Delay Symmetry

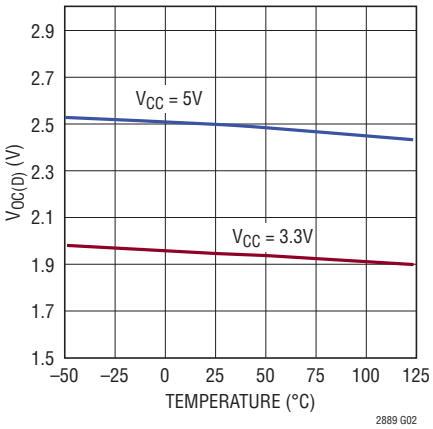
TYPICAL PERFORMANCE CHARACTERISTICS

Unless otherwise noted, the following conditions apply: T_A = 25°C, PV_{CC} = V_{CC} = 3.3V for the LTM2889-3, PV_{CC} = V_{CC} = 5.0V for the LTM2889-5, V_L = 3.3V, GND = GND2 = S = $\overline{RE}$ = 0V, ON = V_L.

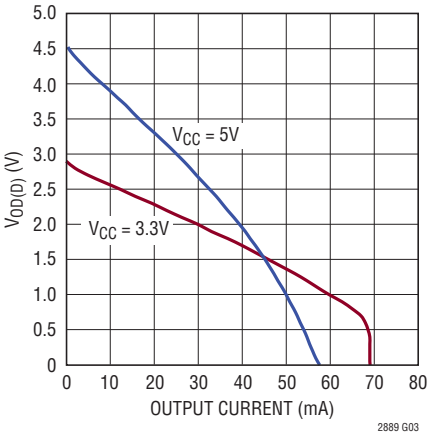
Driver Differential Output Voltage (Dominant) vs Temperature



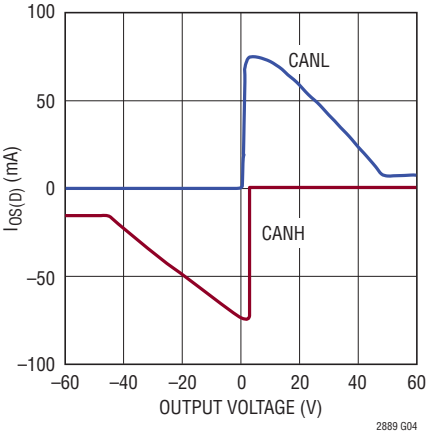
Common Mode Output Voltage (Dominant) vs Temperature



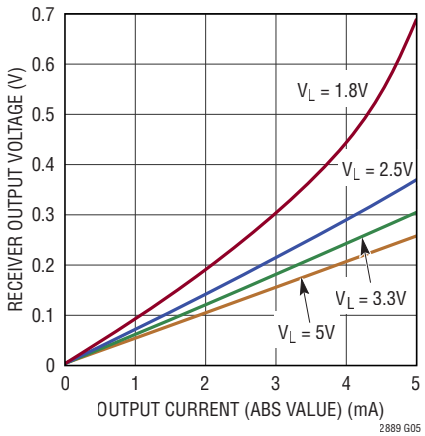
Driver Differential Output Voltage (Dominant) vs Output Current



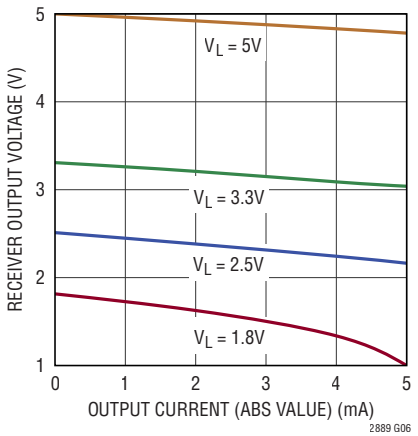
Driver Output Current vs Differential Output Voltage (Dominant)



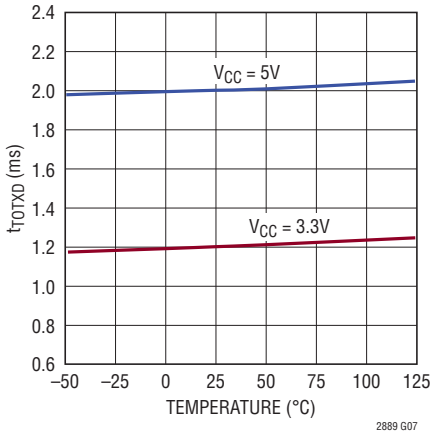
Receiver Dominant Output Voltage vs Output Current



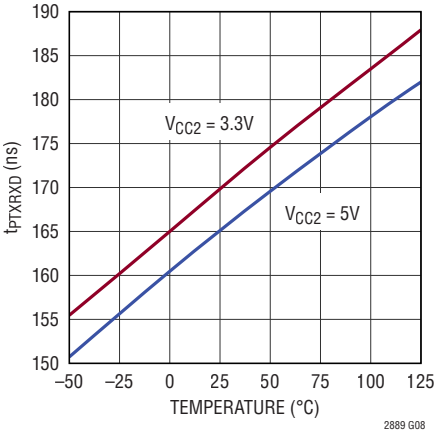
Receiver Recessive Output Voltage vs Output Current



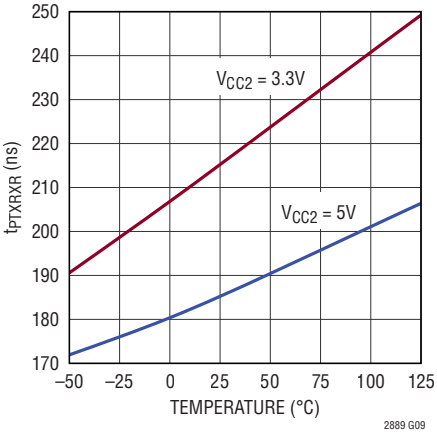
TXD Timeout Time vs Temperature



TXD to RXD Dominant Propagation Delay vs Temperature



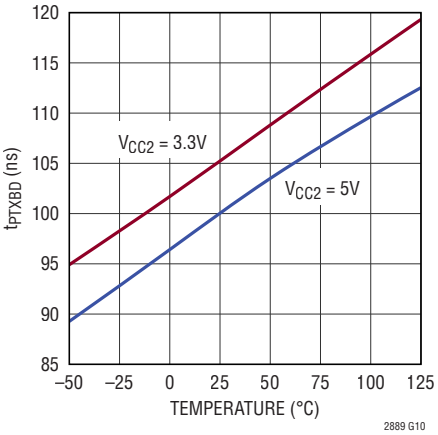
TXD to RXD Recessive Propagation Delay vs Temperature



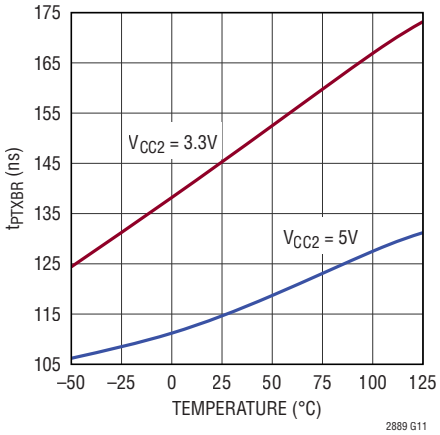
TYPICAL PERFORMANCE CHARACTERISTICS

Unless otherwise noted, the following conditions apply: T_A = 25°C, PV_{CC} = V_{CC} = 3.3V for the LTM2889-3, PV_{CC} = V_{CC} = 5.0V for the LTM2889-5, V_L = 3.3V, GND = GND2 = S = $\overline{RE}$ = 0V, ON = V_L.

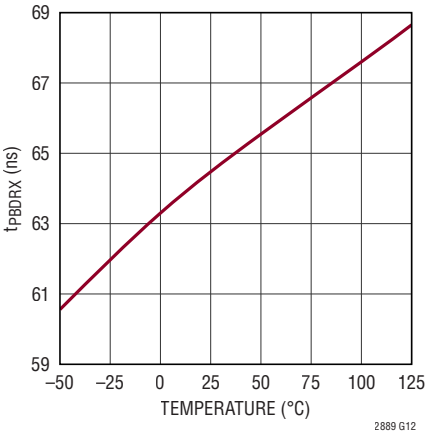
TXD to Bus Dominant Propagation Delay vs Temperature



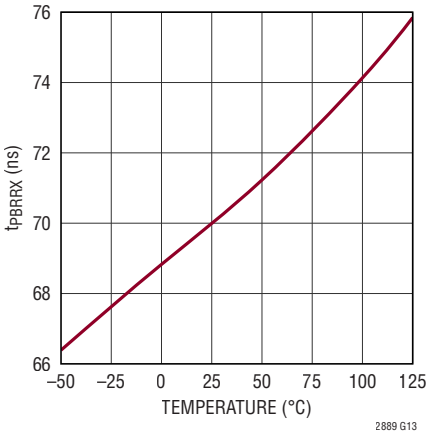
TXD to Bus Recessive Propagation Delay vs Temperature



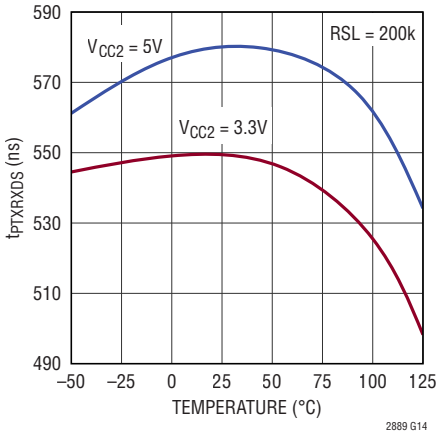
Bus Dominant to RXD Propagation Delay vs Temperature



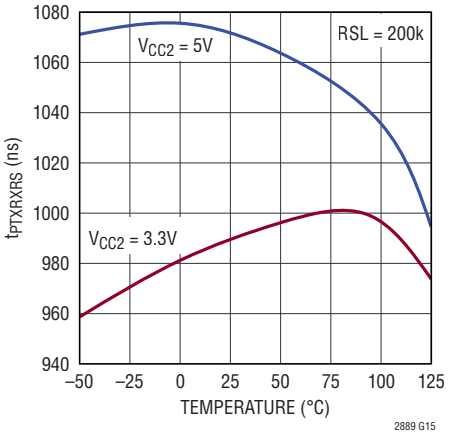
Bus Recessive to RXD Propagation Delay vs Temperature



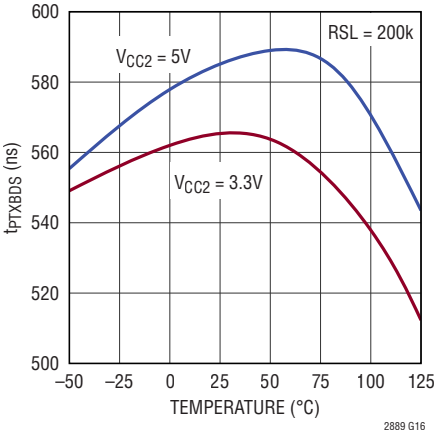
TXD to RXD Dominant Propagation Delay vs Temperature, Slow Slew



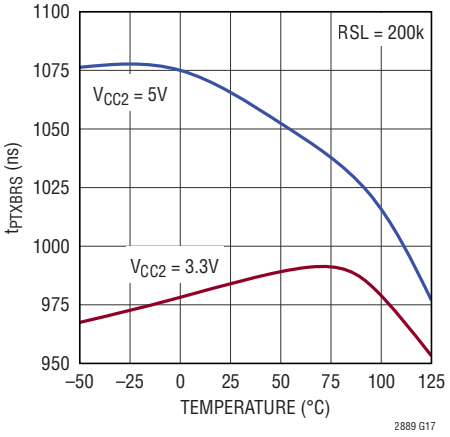
TXD to RXD Recessive Propagation Delay vs Temperature, Slow Slew



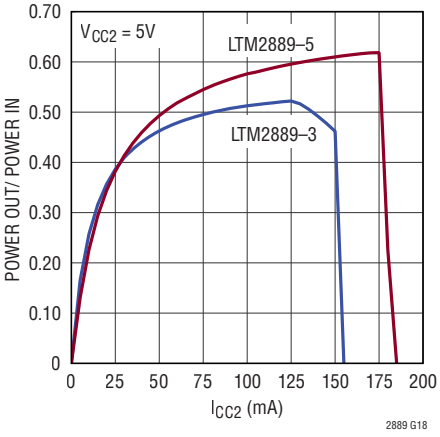
TXD to Bus Dominant Propagation Delay vs Temperature, Slow Slew



TXD to Bus Recessive Propagation Delay vs Temperature, Slow Slew



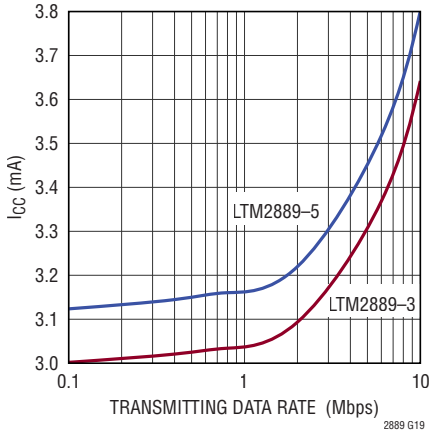
V_{CC2} Power Efficiency



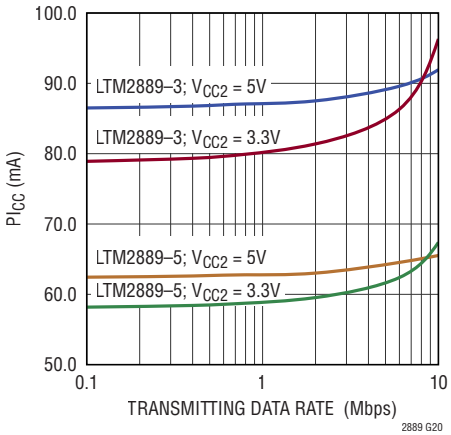
TYPICAL PERFORMANCE CHARACTERISTICS

Unless otherwise noted, the following conditions apply:
T_A = 25°C, PV_{CC} = V_{CC} = 3.3V for the LTM2889-3, PV_{CC} = V_{CC} = 5.0V for the LTM2889-5, V_L = 3.3V, GND = GND2 = S = $\overline{RE}$ = 0V, ON = V_L.

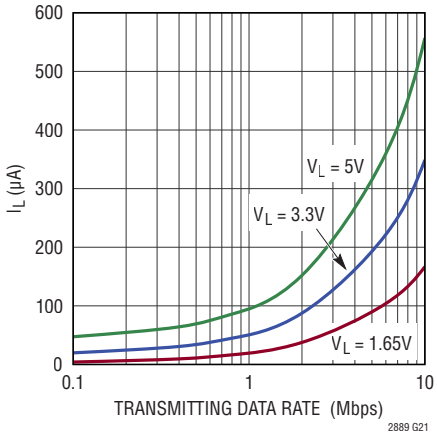
V_{CC} Supply Current vs Transmitting Data Rate



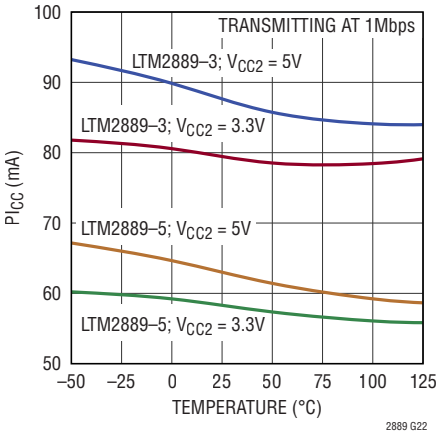
PV_{CC} Supply Current vs Transmitting Data Rate



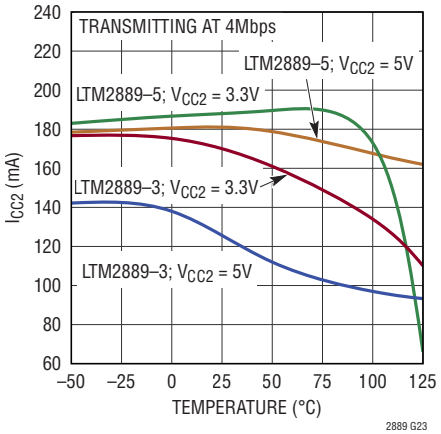
V_L Supply Current vs Transmitting Data Rate



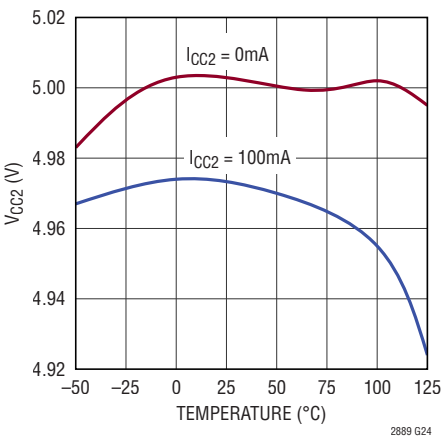
PV_{CC} Supply Current vs Temperature



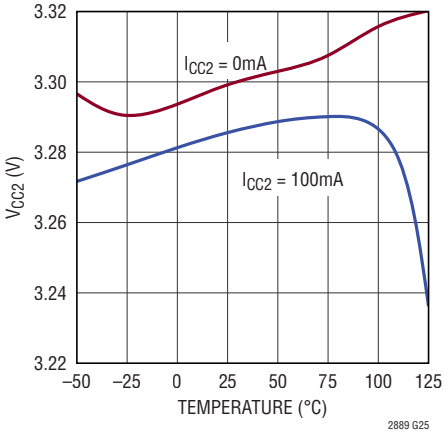
V_{CC2} Surplus Current vs Temperature



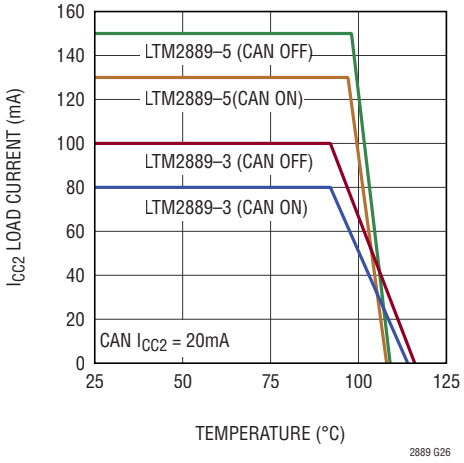
V_{CC2} vs Temperature (5V)



V_{CC2} vs Temperature (3.3V)



Derating for 125°C Maximum Internal Operating Temperature



PIN FUNCTIONS

LOGIC SIDE:

(I/O pins referenced to V_L and GND)

$\overline{RE}$ (Pin A1): Receiver Output Enable. A logic low enables the receiver output, RXD. A logic high disables the receiver output. $\overline{RE}$ has a weak pull-down to GND. In typical usage, $\overline{RE}$ is tied to ground.

RXD (Pin A2): Receiver Output. When the CAN bus is in the dominant state, RXD is low. When the CAN bus is in the recessive state, RXD is high. When the receiver output is disabled, RXD is high-Z and has a weak pull-up to V_L. Under the condition of an isolation communication failure, the receiver output is disabled.

TXD (Pin A3): Transmit Driver Input. When S is low, a low on TXD puts the driver into the dominant state, driving CANH high and CANL low. A high on TXD forces the driver into the recessive state, with both CANH and CANL in a high impedance state. If TXD and S are both held low for longer than t_{TOTXD}, the driver reverts to the recessive state. TXD has a weak pull-up to V_L.

S (Pin A4): Transmit Driver Silent. A high on S forces the driver into the recessive state, with both CANH and CANL in a high impedance state. S has a weak pull-down to GND.

ON (Pin A5): Enable. Enables the power and data communications through the isolation barrier. If ON is high the LTM2889 is enabled and power and communications are functional to the isolated side. If ON is low, the logic side is held in reset and the isolated side is unpowered. ON has a weak pull-down to GND.

V_L (Pin A6): Logic Supply. Interface supply voltage for pins $\overline{RE}$, RXD, TXD, S, and ON. Operating voltage is 1.62V to 5.5V. Internally bypassed to GND with 1µF.

V_{CC} (Pins A7, B7): Supply Voltage. Operating voltage is 3V to 5.5V for both LTM2889-3 and LTM2889-5. Internally bypassed to GND with 1µF.

PV_{CC} (Pins A8, B8): Isolated Power Supply Input. Operating voltage is 3V to 3.6V for LTM2889-3 and 4.5V to 5.5V for LTM2889-5. Internally bypassed to GND with 2.2µF. In typical usage, PV_{CC} is tied to V_{CC}.

GND (Pins B1-B8): Logic Side Circuit Ground

ISOLATED SIDE:

(I/O pins referenced to V_{CC2} and GND2)

CANL (Pin L1): Low Level CAN Bus Line. ±60V tolerant, 25kV ESD.

SPLIT (Pin L2): Common Mode Stabilization Output for Optional Split Termination. ±60V tolerant, 25kV ESD. If unused, leave open. Internally bypassed to GND2 with 4.7nF.

CANH (Pin L3): High Level CAN Bus Line. ±60V tolerant, 25kV ESD.

GND2 (Pins L4, K1-K4, K6-K8): Isolated Side Circuit Ground.

RS (Pin L5): Shutdown Mode/Slew Control Input. A voltage on RS higher than V_{IH_RS} puts the CAN transceiver in a low power shutdown state. The CAN bus and RXD will be in the recessive state, the CAN receiver will be disconnected from the bus, and the power converter will continue to operate. A voltage on RS lower than V_{IL_RS} enables the CAN transceiver. A resistor between RS and GND2 can be used to control the slew rate. See Applications Information section for details.

ADJ (Pin L6): Adjust pin to override the default 5V regulation voltage of the isolated power supply. May be used to set V_{CC2} to 3.3V in either the LTM2889-3 or LTM2889-5 versions. Leave floating for 5V output. See Applications Information section for details.

V_{CC2} (Pin L7-L8): Isolated Power Supply Output. Internally generated from PV_{CC} by an isolated DC/DC converter and regulated to 5V. Internally bypassed to GND2 with 10µF.

DNC (Pin K5): Do not make electrical connection to this pin. Do not connect to GND2.

BLOCK DIAGRAM

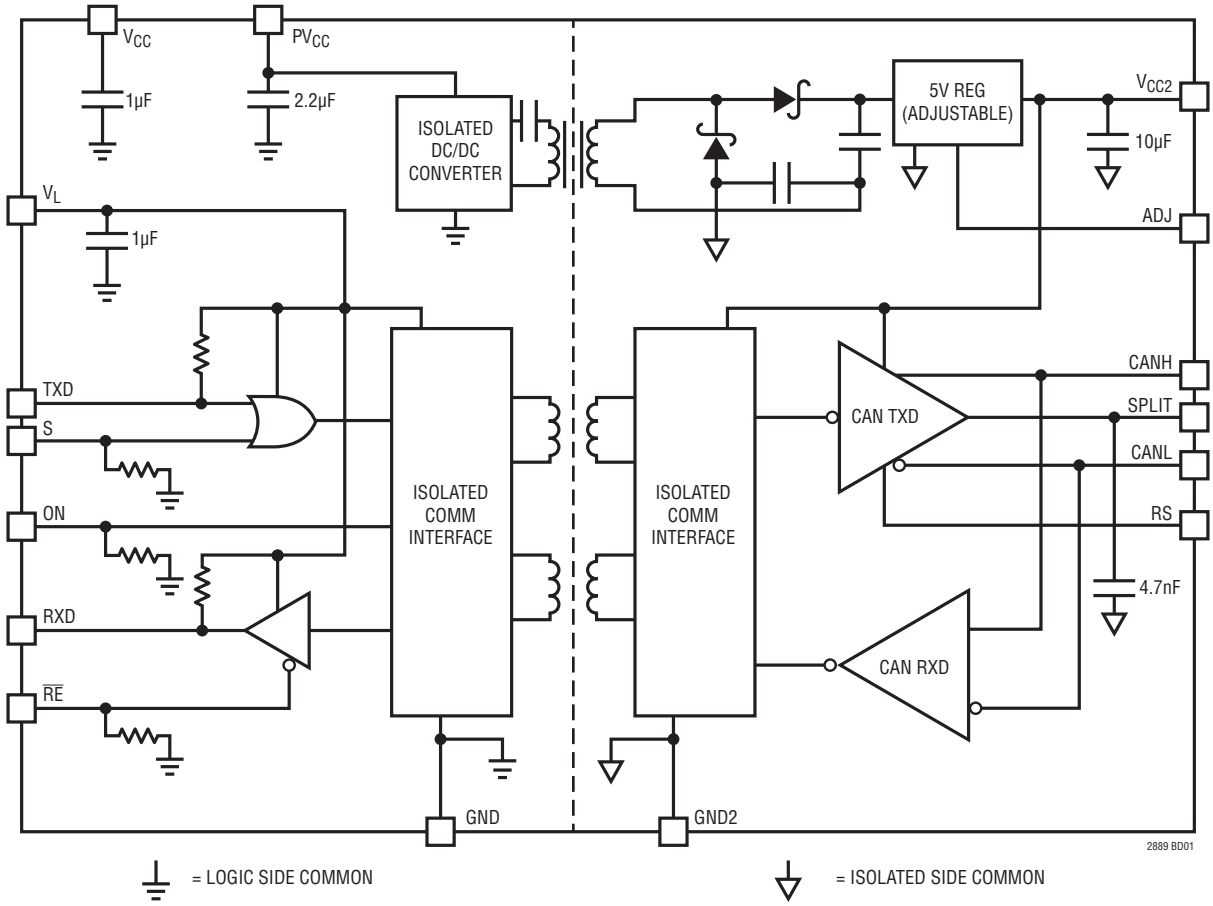


Figure 9. LTM2889 Simplified Block Diagram

APPLICATIONS INFORMATION

OVERVIEW

The LTM2889 isolated CAN µModule transceiver provides a galvanically-isolated robust CAN interface, powered by an integrated, regulated DC/DC converter, complete with decoupling capacitors. The LTM2889 is ideal for use in networks where grounds can take on different voltages. Isolation in the LTM2889 blocks high voltage differences, eliminates ground loops and is extremely tolerant of common mode transients between ground planes. Error-free operation is maintained through common mode events greater than 30kV/µs providing excellent noise isolation.

Isolator µModule Technology

The LTM2889 utilizes isolator µModule technology to translate signals and power across an isolation barrier. Signals on either side of the barrier are encoded into pulses and translated across the isolation boundary using coreless transformers formed in the µModule substrate. This system, complete with data refresh, error checking, safe shutdown on fail, and extremely high common mode immunity, provides a robust solution for bidirectional signal isolation. The µModule technology provides the means to combine the isolated signaling with multiple regulators and a powerful isolated DC/DC converter in one small package.

DC/DC Converter

The LTM2889 contains a fully integrated DC/DC converter, including the transformer, so that no external components are necessary. The logic side contains a full-bridge driver, running at 2MHz, and is AC-coupled to a single transformer primary. A series DC blocking capacitor prevents transformer saturation due to driver duty cycle imbalance. The transformer scales the primary voltage, and is rectified by a full-wave voltage doubler. This topology allows for a single diode drop, as in a center tapped full-wave bridge, and eliminates transformer saturation caused by secondary imbalances. The DC/DC converter is connected to a low dropout regulator (LDO) to provide a regulated 5V output.

V_{CC2} Output

The on-board DC/DC converter provides isolated 5V power to output V_{CC2}. V_{CC2} is capable of supplying up to 750mW of power at 5V in the LTM2889-5 option and up to 500mW of power in the LTM2889-3 option. This power is available to external applications. The amount of surplus current is dependent upon the implementation and current delivered to the CAN driver and line load. An example of available surplus current is shown in the Typical Performance Characteristics graph, V_{CC2} Surplus Current vs Temperature. V_{CC2} is bypassed internally with a 10µF capacitor.

3.3V V_{CC2} Output

The V_{CC2} supply may be adjusted to an output voltage of 3.3V by connecting a resistor divider between V_{CC2}, the ADJ pin, and GND2 as shown in Figure 10. Operating the CAN transceiver at 3.3V reduces PV_{CC} current and may reduce EMI when used in a system with other 3.3V CAN transceivers. For a 5V V_{CC2} output no resistor divider is used, and the ADJ pin should be left unconnected.

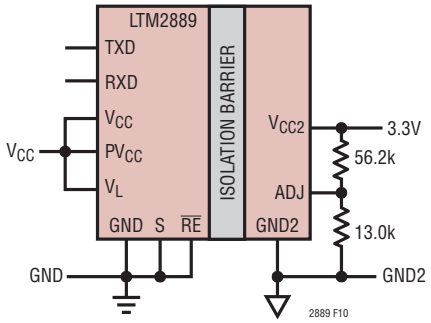


Figure 10. Adjusting V_{CC2} for 3.3V Output.

PV_{CC} Power Supply

The integrated DC/DC converter is powered by separate PV_{CC} supply pins. In typical operation, PV_{CC} is connected to the same supply as V_{CC}. The LTM2889 may be operated with an external isolated supply powering the isolated CAN transceiver instead of the internal converter. This is accomplished by applying an external source of isolated power between the V_{CC2} and GND2 pins, and dis-

APPLICATIONS INFORMATION

abling the internal converter by grounding the PV_{CC} pins (Figure 25). In this configuration, both the LTM2889-3 and the LTM2889-5 may be supplied with a voltage between 3V and 5.5V on the V_{CC} pin, and either 3.3V or 5V on the V_{CC2} pin. The ADJ pin should be left unconnected.

V_L Logic Supply

A separate logic supply pin V_L allows the LTM2889 to interface with any logic signal from 1.62V to 5.5V as shown in Figure 11. Simply connect the desired logic supply to V_L. There is no interdependency between V_{CC}, PV_{CC}, or V_L; they may simultaneously operate at any voltage within their specified operating ranges and sequence in any order. V_L is bypassed internally with a 1µF capacitor.

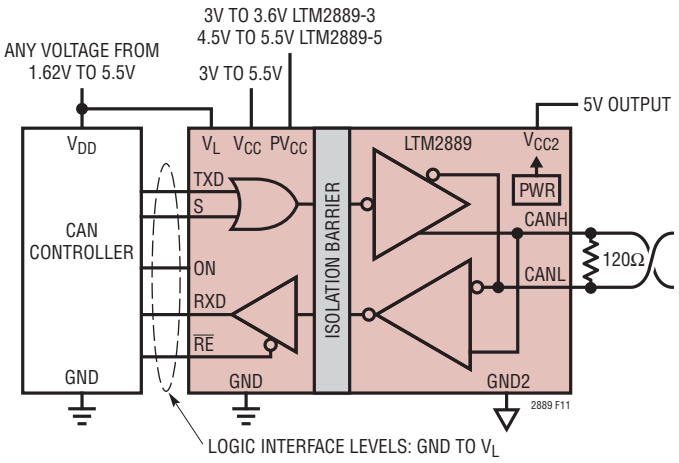


Figure 11. V_{CC} and V_L Are Independent

OPERATING MODES

The LTM2889 supports various modes of operation as summarized in Table 1.

Table 1. Operating Modes*

INPUTS				OUTPUTS		
ON	TXD	S	$\overline{RE}$	CANH, CANL	RXD	MODE
1	0	0	0	DOMINANT**	0**	NORMAL
1	1	0	0	RECESSIVE	1	NORMAL
1	X	1	0	RECESSIVE	1	SILENT
0	X	X	X	HI-Z	HI-Z	OFF
X	X	X	1		Hi-Z	

*1 = logic HIGH; 0 = logic LOW; X = either logic state

** if TXD dominant timeout timer has not expired

Normal Mode

With the ON pin high and S pin low, the LTM2889 operates in Normal mode. The transceiver can transmit and receive data via the bus lines CANH and CANL. The differential receiver delivers a logic low level on RXD if the bus lines are dominant or a logic high level if the bus lines are recessive. The slope of the output signals on the bus lines is controlled and optimized to minimize common mode perturbations and electromagnetic emissions (EME).

Silent Mode

Silent mode is entered by bringing the S pin high. In this state, the LTM2889 driver outputs become recessive, independent of the TXD input. As shown in the block diagram, the TXD and S pins are logically OR'd together into the data path of the LTM2889.

OFF Mode and Unpowered State

When the ON pin is low, the device enters OFF mode and all functions on both sides of the isolation boundary are shut down. The isolated DC/DC converter stops operating and the isolated supply voltage, V_{CC2} collapses. The CANH and CANL lines are not driven and their common mode bias releases control. RXD will be high-Z and passively pulled to V_L, whether V_L is powered or low. A device that is OFF draws no more than 10µA of current from PV_{CC}, V_{CC} and V_L.

CAN TRANSCEIVER

The LTM2889 contains a robust, high performance integrated CAN transceiver featuring fault protection, high ESD tolerance, and a wide common mode operating range.

±60V Fault Protection

The LTM2889 features ±60V fault protection on its CAN Bus interface pins (CANH, CANL, SPLIT) with respect to GND2. The high breakdown voltage provides protection during all states of operation, including dominant and recessive states, shutdown, and powered off. The driver outputs use a progressive foldback current limit to protect against overvoltage faults while still allowing high current output drive. The LTM2889 is protected from ±60V bus

APPLICATIONS INFORMATION

faults even with the loss of GND2 or V_{CC2} (GND2 open faults are not tested in production). In the case of V_{CC2} shorted to GND2, the transceiver is off and the bus pins remain in the high impedance state.

±36V Extended Common Mode Range

The LTM2889 CAN Bus receiver features an extended common mode operating range of –36V to 36V with respect to GND2 when operating from a 5V V_{CC2} supply, and –25V to 25V when operating from a 3.3V V_{CC2} supply. The wide common mode increases the reliability of operation in environments with high common mode voltages created by electrical noise or local ground potential differences between bus nodes on the isolated side of the network due to ground loops. This extended common mode range allows the LTM2889 to transmit and receive under conditions that would cause data errors and possible device damage in competing products.

±25kV ESD Protection

The LTM2889 features exceptionally robust ESD protection. The transceiver interface pins (CANH, CANL, SPLIT) feature protection with respect to GND2 to ±25kV HBM without latchup or damage, during all modes of operation or while unpowered. The LTM2889 features ±10kV HBM protection across the isolation barrier for discharges between any one of the interface pins (CANH, CANL, SPLIT, V_{CC2}, GND2) and any one of the supply pins referenced to GND (V_{CC}, PV_{CC}, V_L, GND).

4Mbps Operation

The LTM2889 features a high speed receiver and transmitter capable of operating up to 4Mbps. In order to operate at this data rate, the transmitter must be set at its maximum slew rate by pulling the RS pin low to GND2 with no more than 4k of resistance, including the output impedance of the buffer driving the RS input (see RS Pin and Variable Slew Rate Control below).

CAN Bus Driver

The driver provides full CAN compatibility. When TXD is low with the chip enabled (RS low), the dominant state is asserted on the CAN bus lines (subject to the TXD timeout t_{TOTXD}); the CANH driver pulls high and the CANL driver pulls low. When TXD is high and RS is low, the driver is in the recessive state; both the CANH and CANL drivers are in the Hi-Z state and the bus termination resistor equalizes the voltage on CANH and CANL. In the recessive state, the impedance on CANH and CANL is determined by the receiver input resistance, R_{IN}. When RS is high the transceiver is in shutdown; the CANH and CANL drivers are in the Hi-Z state, and the receiver input resistance R_{IN} is disconnected from the bus by a FET switch.

Transmit Dominant Timeout Function

The LTM2889 CAN transceiver includes a 2ms (typical) timer to limit the time that the transmitter can hold the bus in the dominant state. If TXD is held low, a dominant state is asserted on CANH and CANL until the TXD timer times out at t_{TOTXD}, after which the transmitter reverts to the recessive state. The timer is reset when TXD is brought high. The transmitter asserts a dominant state upon the next TXD low.

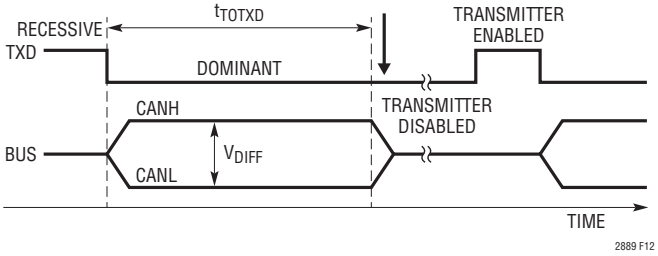


Figure 12. Transmitter Dominant Timeout Function

Driver Overvoltage, Overcurrent, and Overtemperature Protection

The driver outputs are protected from short circuits to any voltage within the absolute maximum range of –60V to 60V with respect to GND2. The driver includes a progressive foldback current limiting circuit that continuously reduces the driver current limit with increasing output fault voltage. The fault current is typically ±10mA for fault voltages of ±60V. Refer to the "Driver Output Current vs Differential Output Voltage (Dominant)" plot in the Typical Performance Characteristics section.

APPLICATIONS INFORMATION

The LTM2889 CAN transceiver also features thermal shutdown protection that disables the driver in case of excessive power dissipation during a fault on the CAN bus (see Notes 3 and 4). When the transceiver die temperature exceeds 170°C (typical), the transmitter is forced into the recessive state. All other functions remain active during the transceiver thermal shutdown, including the CAN bus receiver and the module isolated communication and power converter. Other chips in the LTM2889 also contain thermal shutdown circuits that will shut down all module operations at approximately 170°C.

Power-Up/Down Glitch-Free Outputs

The LTM2889 CAN transceiver employs a supply undervoltage detection circuit to control the activation of the circuitry on-chip. During power-up, the CANH, CANL, RXD and SPLIT outputs remain in the high impedance state until the supply reaches a voltage sufficient to reliably operate the transceiver. At this point, the transceiver activates if RS is low.

The receiver output goes active after a short delay t_{ENRX} and reflects the state at the CAN bus pins, and the SPLIT output goes active at approximately the same time. The transmitter powers up in the high-Z recessive state until the V_{CC2} supply reaches the power-good voltage, at which time the transmitter outputs become active and reflect the state of the TXD pin. This assures that the transmitter does not disturb the bus by glitching to the dominant state during power-up.

During power down, the reverse occurs; the supply undervoltage detection circuit senses low supply voltage and immediately puts the transceiver into shutdown. The CANH, CANL, RXD, and SPLIT outputs go to the high impedance state. The voltage on RXD is pulled high by an internal pull-up resistor.

Common Mode Voltage vs Supply Voltage

When operating from the default 5V V_{CC2} supply voltage the LTM2889 CAN transceiver adheres to the ISO 11898-2 CAN bus standard by maintaining drive levels that are symmetric around $V_{CC2}/2$ = 2.5V with respect to GND2. An internal common mode reference of $V_{CC2}/2$ is buffered to supply the termination of the receiver input resistors. A second buffer with a high voltage tolerant output supplies $V_{CC2}/2$ to the SPLIT output.

If the output from the internal isolated converter is set to 3.3V using a resistor divider on the ADJ pin (Figure 10), the 2.5V nominal common mode voltage specified in the ISO 11898-2 standard is too close to the 3.3V supply to provide symmetric drive levels while maintaining the necessary differential output voltage. To maintain driver symmetry the common mode reference voltage is lowered during 3.3V operation. The typical output common mode voltage is 1.95V in the dominant state. The internal common mode reference is set to $V_{CC2}/2$ + 0.3V = 1.95V to match the dominant state output common mode voltage. This reference is independently buffered to supply the termination of the receiver input resistors and the SPLIT voltage output.

As the LTM2889 CAN transceiver operates over a very wide common mode range, this small shift of –0.55V in the common mode when operating from 3.3V does not degrade data transmission or reception. An LTM2889 CAN transceiver operating at 3.3V may share a bus with other CAN transceivers operating at 5V. However, the electromagnetic emissions (EME) may be larger if transceivers powered by different voltages share a bus, due to the fluctuation in the common mode voltage from 1.95V (when a CAN transceiver on a 3.3V supply is dominant) to 2.5V (when a CAN transceiver on a 5V supply is dominant).

RS Pin and Variable Slew Rate Control

The driver features adjustable slew rate for improved EME performance. The slew rate is set by the amount of current that is sourced by the RS pin when it is pulled below approximately 1.1V (referenced to GND2). This allows the slew rate to be set by a single slew control resistor RSL in series with the RS pin (Figure 1).

The relationship between the series slew control resistor RSL and the transmitter slew rate can be observed in Figure 13. RSL ≤ 4k is recommended for high data rate communication. RSL should be less than 200k to ensure that the RS pin can be reliably pulled below V_{IL_RS} to enable the chip.

APPLICATIONS INFORMATION

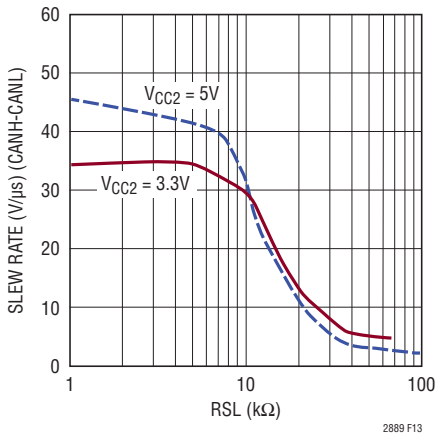


Figure 13. Slew Rate vs Slew Control Resistor RSL

When a voltage between 1.1V and V_{CC2} is applied, the RS pin acts as a high impedance receiver. A voltage above V_{IH_RS} puts the chip in shutdown, while a voltage below V_{IL_RS} but above 1.1V activates the chip and sets the transmitter to the minimum slew rate.

The slew control circuit on the RS pin is activated at applied voltages below 1.1V. The RS pin can be approximately modeled as a 1.1V voltage source with a series resistance of 2k and a current compliance limit of –100µA, and a 250k pull-up resistor to V_{CC2} (Figure 14). Lowering the voltage on RS increases the slew control current I_{SC} being drawn from the slew control circuit until the voltage reaches ~0.9V, where the current drawn from the circuit is ~ –100µA. Below an applied voltage of ~ 0.9V, the slew control circuit sources no additional current, and the current drawn from it remains at ~ –100µA down to 0V.

The total current I_{RS} drawn from the RS pin for input voltage $0.9V \le V_{RS} \le 1.1V$ is the sum of the internal pull-up resistor current I_{RS} and the slew control current I_{SC}.

$$I_{RS(0.9V \le V_{RS} \le 1.1V)} = I_{PU} + I_{SC}$$

$$= \frac{V_{CC2} - V_{RS}}{250k} + \frac{1.1V - V_{RS}}{2k}$$

The transmitter slew rate is controlled by the slew control current I_{SC} with increasing current magnitude corresponding to higher slew rates. The slew rate can be controlled using a single slew control resistor RSL in series with the RS pin. When the RS pin is pulled low towards ground by an external driver, RSL limits the amount of current drawn from the RS pin and sets the transmitter slew rate. Alternatively, the slew rate may be controlled by an external voltage or current source.

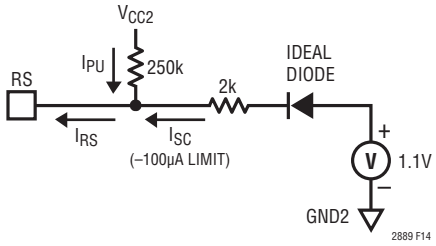


Figure 14. Equivalent Circuit of RS Pin

High Symmetry Driver with Variable Slew Rate

The electromagnetic emissions spectrum of a differential line transmitter is largely determined by the variation in the common mode voltage during switching, as the differential component of the emissions from the two lines cancel, while the common mode emissions of the two lines add. The LTM2889 transmitter has been designed to maintain highly symmetric transitions on the CANH and CANL lines to minimize the perturbation of the common mode voltage during switching (Figure 15), resulting in low EME. The common mode switching symmetry is guaranteed by the V_{SYM} specification.

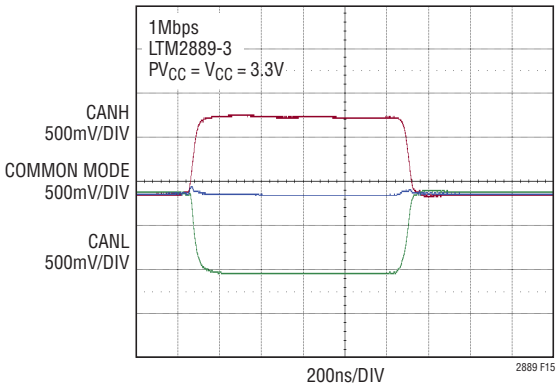


Figure 15. Low Perturbation of Common Mode Voltage During Switching

APPLICATIONS INFORMATION

In addition to full compliance with the ISO 11898-2 standard, LTM2889 meets the more stringent requirements of ISO 11898-5 for bus driver symmetry. This requires that the common mode voltage stay within the limits not only during the static dominant and recessive states, but during the bit transition states as well. Ultra-high speed peak detect circuits are used during manufacturing test to ensure that V_{SYM} limits are not exceeded at any point during the switching cycle.

The high frequency content may be reduced by choosing a lower data rate and a slower slew rate for the signal transitions. The LTM2889 CAN transceiver provides an approximate 20 to 1 reduction in slew rate, with a corresponding decrease in the high frequency content. The lowest slew rate is suitable for data communication at 200kbps or below, while the highest slew rate supports 4Mbps. The slew rate limit circuit maintains consistent control of transmitter slew rates across voltage and temperature to ensure predictable performance under all operating conditions. Figure 16 demonstrates the reduction in high frequency content of the common mode voltage achieved by the lowest slew rate compared to the highest slew rate when operating at 200kbps.

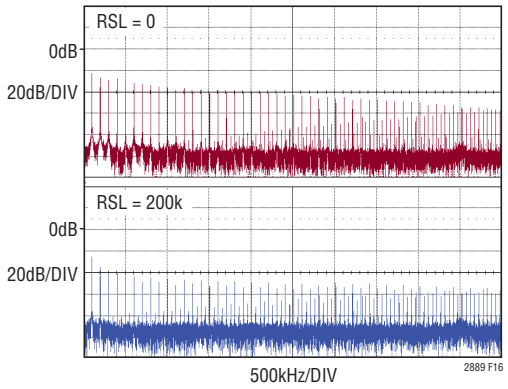


Figure 16. Power Spectrum of Common Mode Voltage Showing High Frequency Reduction of Lowest Slew Rate (RSL = 200k) Compared to Highest Slew Rate (RSL = 0)

SPLIT Pin Output for Split Termination Support

Split termination is an optional termination technique to reduce common mode voltage perturbations that can produce EME. A split terminator divides the single line-end termination resistor (nominally 120Ω) into two series resistors of half the value of the single termination resistor (Figure 2). The center point of the two resistors is connected to a low impedance voltage source that sets the recessive common mode voltage.

Split termination suppresses common mode voltage perturbations by providing a low impedance load to common mode noise sources such as transmitter noise or coupling to external noise sources. In the case of single resistor termination, the only load on a common mode noise source is the parallel impedance of the input resistors of the CAN transceivers on the bus. This results in a common mode impedance of several kilohms for a small network. The split termination, on the other hand, provides a common mode load equal to the parallel resistance of the two split termination resistors, or ¼ the resistance of the single termination resistor (30Ω). This low common mode impedance results in a reduction of the common mode noise voltage compared to the much higher common mode impedance of the single resistor termination.

The SPLIT pin on the LTM2889 provides a buffered voltage to bias the mid-point of the split termination resistors. The voltage on the SPLIT pin matches the common mode voltage established by the transmitter in the dominant state and the receiver input resistor bias during the recessive state: 2.5V when V_{CC2} = 5V and 1.95V when V_{CC2} = 3.3V. SPLIT is decoupled to GND2 with an internal 4.7nF capacitor to lower the AC impedance to better suppress fast transients. SPLIT is a high voltage fault tolerant output that tolerates the same ±60V overvoltage faults and ±25kV ESD discharges as CANH and CANL.

One disadvantage of the SPLIT termination is higher power supply current if the two terminating transceivers differ in their common mode voltage due to differences in V_{CC2} or GND2 potential or to chip to chip variations in the internal reference voltages. This will result in the transceiver with the higher common mode voltage sourcing current into the bus lines through its SPLIT pin, while the transceiver with the lower common mode voltage will sink current through its SPLIT pin.

APPLICATIONS INFORMATION

Ideal Passive Behavior to CAN Bus With Supply Off

When the power supply is removed or the chip is in shutdown, the CANH and CANL pins are in a high impedance state. The receiver inputs are isolated from the CANH and CANL nodes by FET switches which open in the absence of power, thereby preventing the resistor dividers on the receiver input from loading the bus. The high impedance state of the receiver is limited by ESD clamps inboard of the 40k input resistors to a typical range of –0.5V to 11V. For bus voltages outside this range, the current flowing into the receiver is governed by the conduction voltages of the ESD device and the 40k nominal receiver input resistance.

DeviceNet Compatibility

DeviceNet is a network standard based on the CAN bus. The DeviceNet standard places requirements on the transceiver that exceed those of the ISO 11898-2 standard. The LTM2889 meets the DeviceNet requirements listed in Table 2.

DeviceNet employs a 5-pin connector with conductors for Power+, Power–, CANH, CANL, and Drain. The power is 24VDC, and the Drain wire is connected to the cable shield for shielded cables. The Power– pin may be connected to LTM2889 GND2, but the Power+ must not be connected to the LTM2889 V_{CC2} pin.

Table 2: DeviceNet Requirements

PARAMETER	DeviceNet REQUIREMENT	ISO 11898-2 REQUIREMENT	LTM2889
Number of Nodes	64	N/A	166
Minimum Differential Input Resistance	20k	10k	50k
Differential Input Capacitance	25pF (Max)	10pF (Nom)	8.4pF (Typ) (Note 6)
Bus Pin Voltage Range (Survivable)	–25V to 18V	–3V to 16V (for 12V Battery)	–60V to 60V
Bus Pin Voltage Range (Operation)	–5V to 10V	–2V to 7V	–36V to 36V (V_{CC} = 5V)
Connector Mis-Wiring Tests, All Pin-Pin Combinations	±18V	N/A	±60V (See Below)

The DeviceNet mis-wiring tests involve connecting an 18V supply to each of the 20 possible pin pair/polarity combinations on the 5-pin connector. The ±60V tolerance of the LTM2889 with respect to GND2 ensures that the LTM2889 will pass all the mis-wiring tests without damage.

PCB Layout Considerations

The high integration of the LTM2889 makes PCB layout very simple. However, to optimize its electrical isolation characteristics, EMI, and thermal performance, some layout considerations are necessary.

- Under heavily loaded conditions PV_{CC} and GND current can exceed 300mA. Sufficient copper must be used on the PCB to insure resistive losses do not cause the supply voltage to drop below the minimum allowed level. Similarly, the V_{CC2} and GND2 conductors must be sized to support any external load current. These heavy copper traces will also help to reduce thermal stress and improve the thermal conductivity.
- Input and Output decoupling is not required, since these components are integrated within the package. An additional bulk capacitor with a value of 6.8µF to 22µF with 1Ω to 3Ω of ESR is recommended. The high ESR of this capacitor reduces board resonances and minimizes voltage spikes caused by hot plugging of the supply voltage. For EMI sensitive applications, an additional low ESL ceramic capacitor of 1µF to 4.7µF, placed as close to the power and ground terminals as possible, is recommended. Alternatively, a number of smaller value parallel capacitors may be used to reduce ESL and achieve the same net capacitance.
- Do not place copper on the PCB between the inner columns of pads. This area must remain open to withstand the rated isolation voltage.
- The use of solid ground planes for GND and GND2 is recommended for non-EMI critical applications to optimize signal fidelity, thermal performance, and to minimize RF emissions due to uncoupled PCB trace conduction. The drawback of using ground planes, where EMI is of concern, is the creation of a dipole antenna structure which can radiate differential voltages formed between GND and GND2. If ground planes are used it is recommended to minimize their area, and use contiguous planes as any openings or splits can exacerbate RF emissions.

APPLICATIONS INFORMATION

- For large ground planes a small capacitance (≤ 330pF) from GND to GND2, either discrete or embedded within the substrate, provides a low impedance current return path for the module parasitic capacitance, minimizing any high frequency differential voltages and substantially reducing radiated emissions. Discrete capacitance will not be as effective due to parasitic ESL. In addition, voltage rating, leakage, and clearance must be considered for component selection. Embedding the capacitance within the PCB substrate provides a near ideal capacitor and eliminates component selection issues; however, the PCB must be 4 layers. Care must be exercised in applying either technique to insure the voltage rating of the barrier is not compromised. The PCB layout in Figures 17-21 show the low EMI demo board for the LTM2889. The demo board uses a combination of EMI mitigation techniques, including both embedded PCB bridge capacitance and discrete GND to GND2 capacitors (C3 + C4). Two safety rated type Y2 capacitors are used in series, manufactured by Murata, part number GA342QR7GF471KW01L. The embedded capacitor effectively suppresses emissions above 400MHz, whereas the discrete capacitors are more effective below 400MHz. EMI performance is shown in Figure 22, measured using a Gigahertz Transverse Electromagnetic (GTEM) cell and method detailed in IEC 61000-4-20, "Testing and Measurement Techniques – Emission and Immunity Testing in Transverse Electromagnetic Waveguides."

RF, MAGNETIC FIELD IMMUNITY

The isolator µModule technology used within the LTM2889 has been independently evaluated, and successfully passed the RF and magnetic field immunity testing requirements per European Standard EN 55024, in accordance with the following test standards:

EN 61000-4-3 Radiated, Radio-Frequency, Electromagnetic Field Immunity

EN 61000-4-8 Power Frequency Magnetic Field Immunity

EN 61000-4-9 Pulse Magnetic Field Immunity

Tests were performed using an unshielded test card designed per the data sheet PCB layout recommendations. Specific limits per test are detailed in Table 3.

Table 3.

TEST	FREQUENCY	FIELD STRENGTH
EN61000-4-3 Annex D	80MHz to 16Hz	10V/m
	1.4MHz to 2Hz	3V/m
	2MHz to 2.7Hz	1V/m
EN61000-4-8 Level 4	50MHz to 60Hz	30A/m
EN61000-4-8 Level 5	60Hz	100A/m*
EN61000-4-9 Level 5	Pulse	100A/m

*Non IEC method

Operation Above 105°C (LTM2889H)

Operation of the H temperature grade LTM2889H above 105°C is limited by the internal power dissipation of the module, and depends on the PV_{CC} voltage range option, the external I_{CC2} load current, and whether the CAN transceiver is on or off. Refer to the Typical Performance Characteristics chart labeled Derating for 125°C Maximum Internal Operating Temperature on page 13. The CAN transceiver of the LTM2889H may operate up to 125°C if V_{CC2} is supplied by an external power supply and the PV_{CC} pins are grounded. Refer to PV_{CC} Power Supply on page 16.

APPLICATIONS INFORMATION

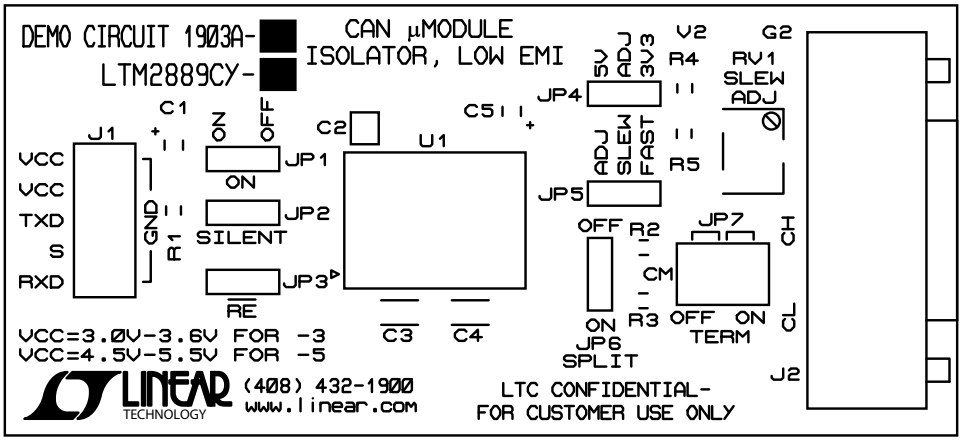


Figure 17. Low EMI Demo Board Layout

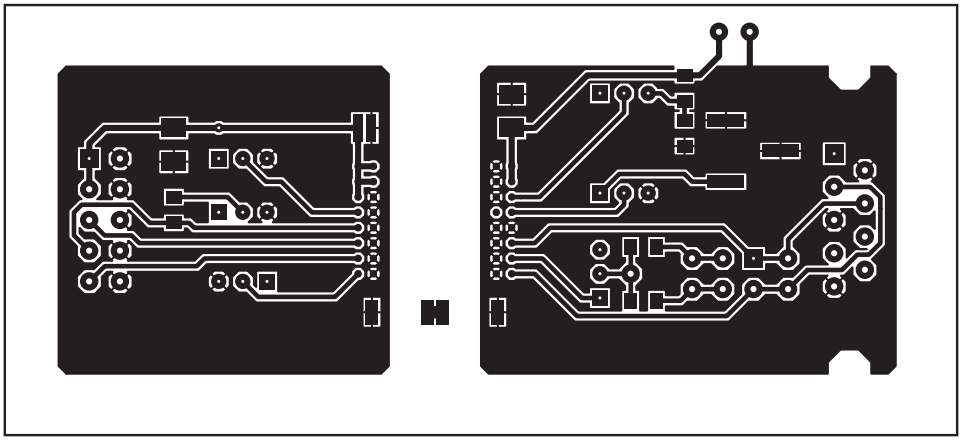


Figure 18. Low EMI Demo Board Layout (DC1746A), Top Layer

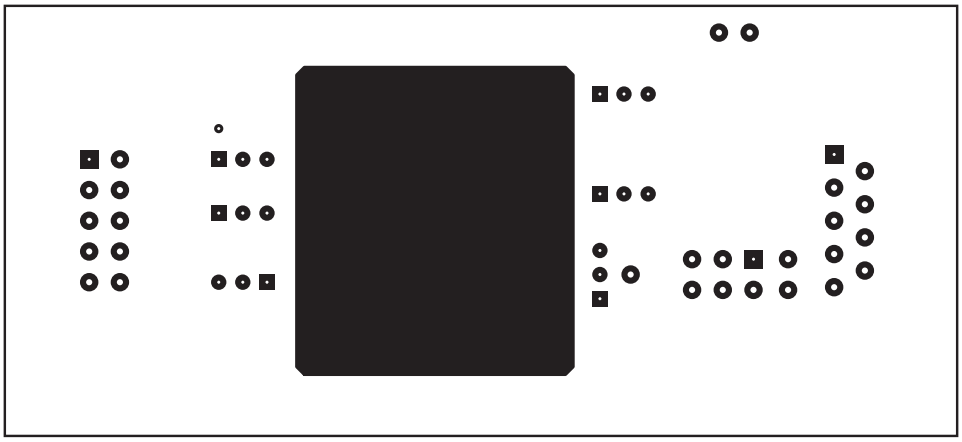


Figure 19. Low EMI Demo Board Layout (DC1746A), Inner Layer 1

APPLICATIONS INFORMATION

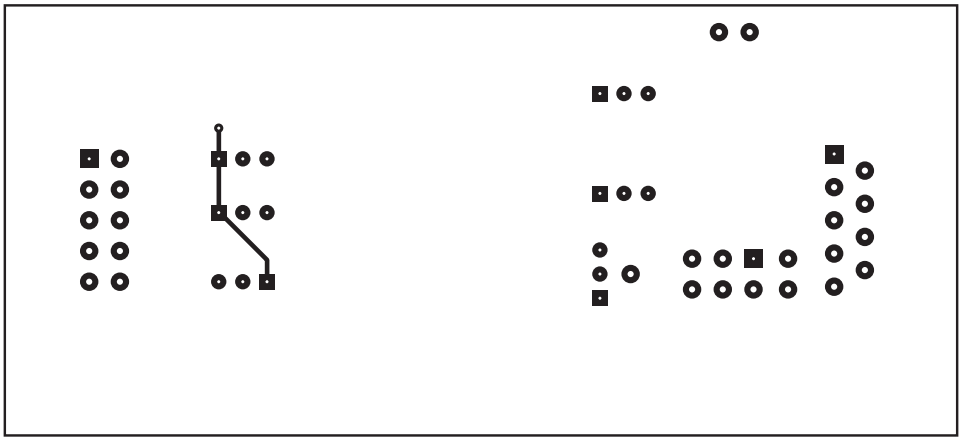


Figure 20. Low EMI Demo Board Layout (DC1746A), Inner Layer 2

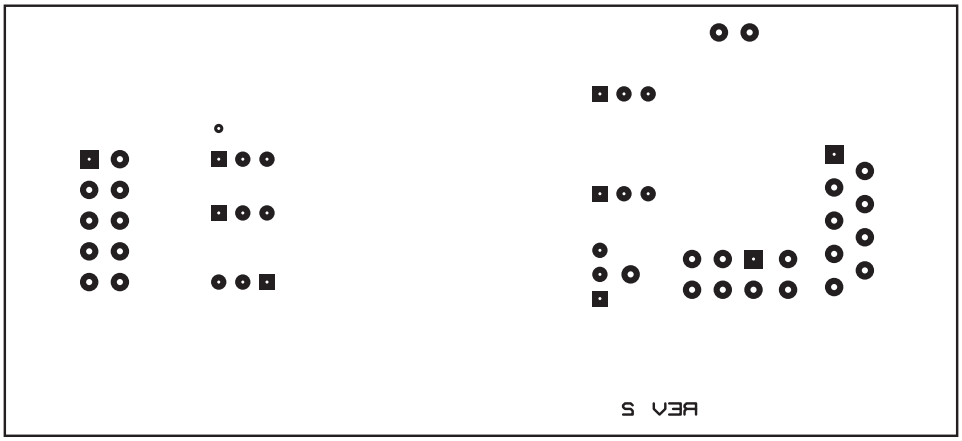


Figure 21. Low EMI Demo Board Layout (DC1746A), Bottom Layer

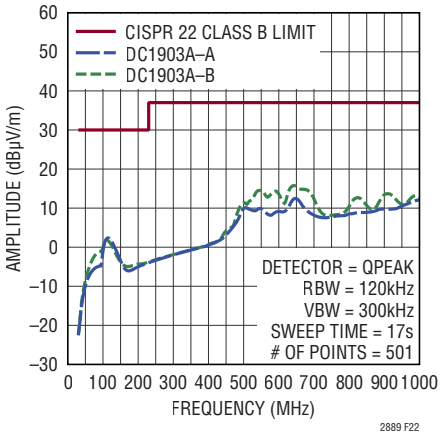


Figure 22. Low EMI Demo Board Emissions

TYPICAL APPLICATIONS

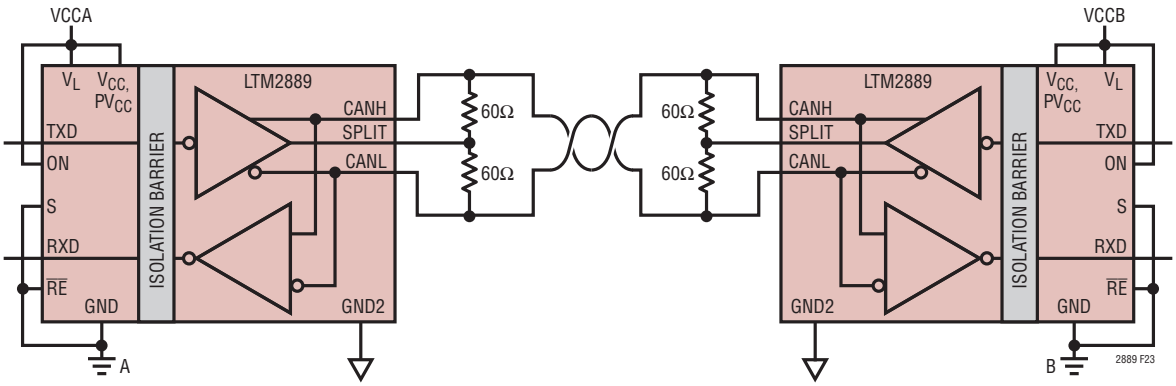


Figure 23. Point-to-Point Isolated CAN Communications on an Unshielded Twisted Pair

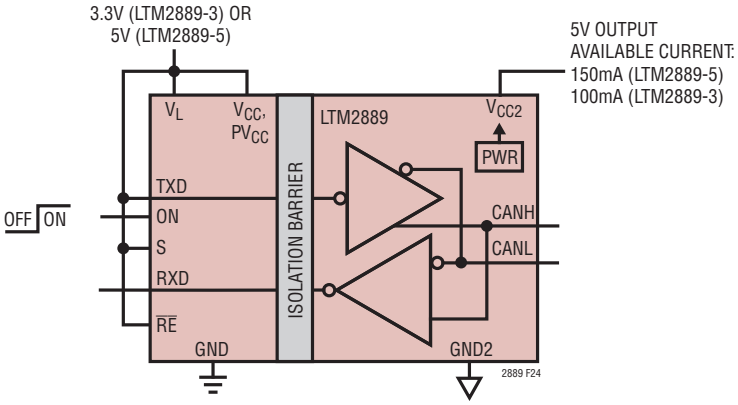


Figure 24. Using the LTM2889 as a Dedicated Isolated 5V Supply

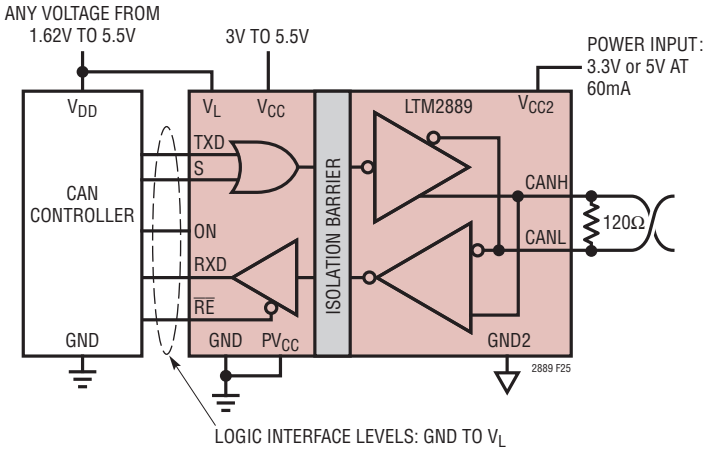
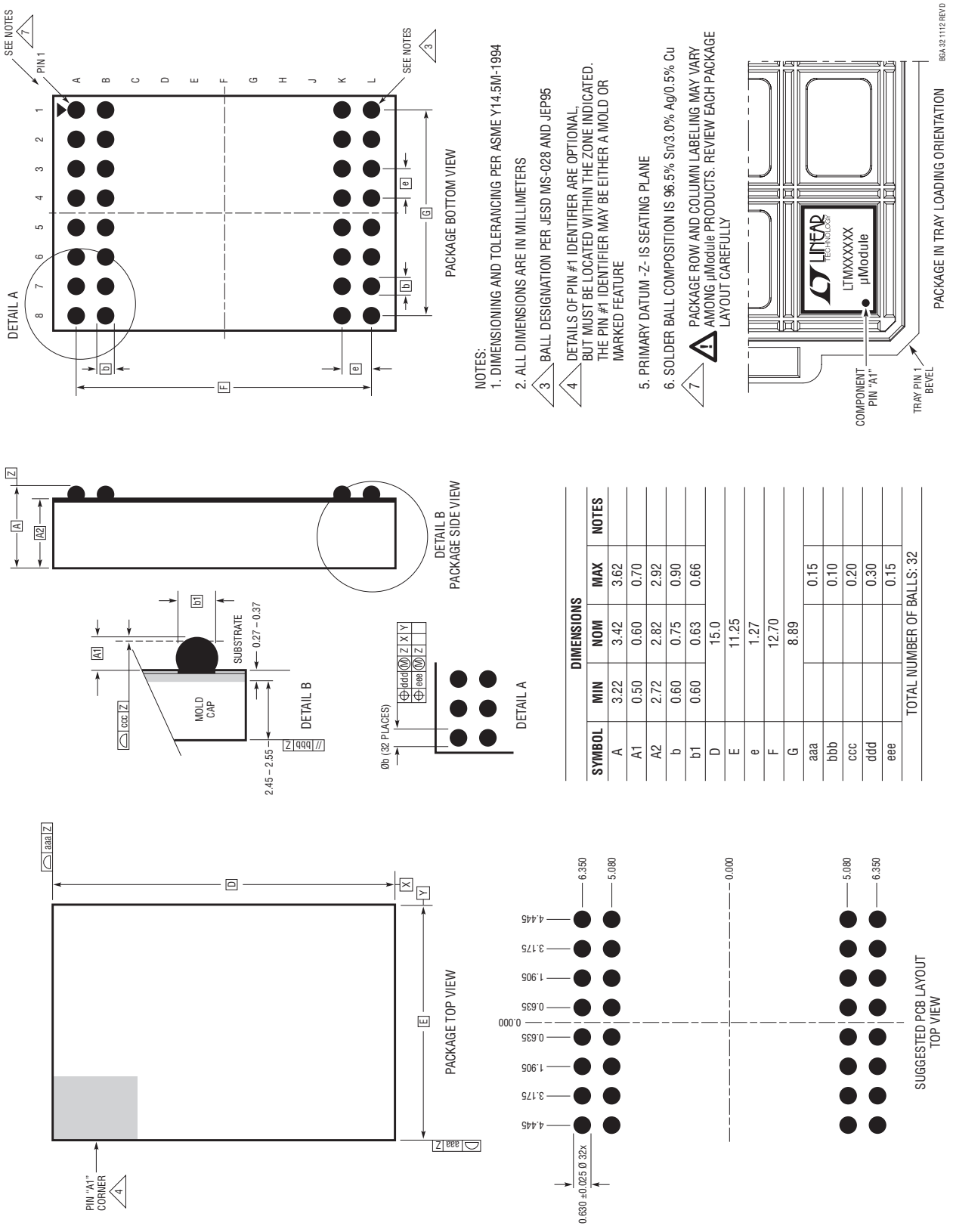


Figure 25. Supplying V_{CC2} From an External Supply

PACKAGE DESCRIPTION

Please refer to http://www.linear.com/product/LTM2889#packaging for the most recent package drawings.



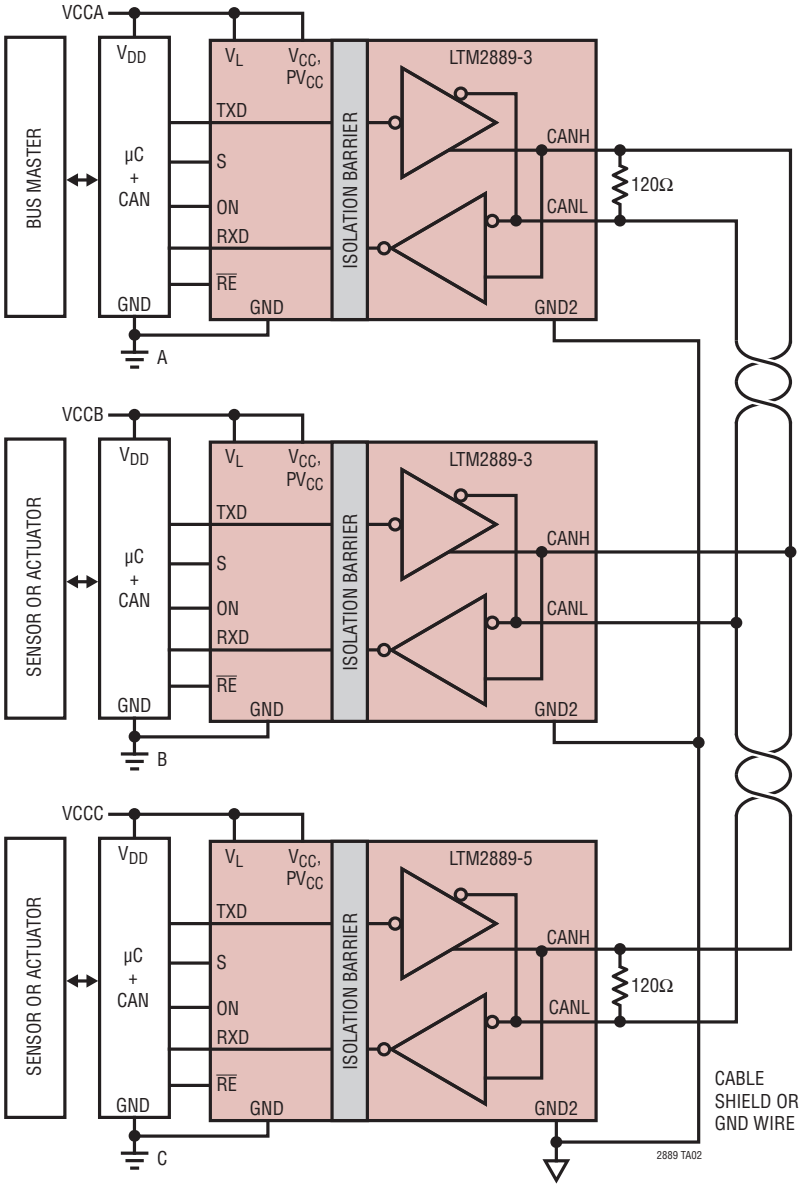
DIMENSIONS				
SYMBOL	MIN	NOM	MAX	NOTES
A	3.22	3.42	3.62	
A1	0.50	0.60	0.70	
A2	2.72	2.82	2.92	
b	0.60	0.75	0.90	
b1	0.60	0.63	0.66	
D		15.0		
E		11.25		
e		1.27		
F		12.70		
G		8.89		
aaa			0.15	
bbb			0.10	
ccc			0.20	
ddd			0.30	
eee			0.15	

2889fa

REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
A	03/17	Added UL-CSA File Number	1

TYPICAL APPLICATION



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC2875	±60V, ±25kV ESD, Fault Protected 3.3V or 5V 25kV ESD High Speed CAN Transceiver	Protected from Overvoltage Line Faults to ±60V, ±25kV ESD, up to 4Mbps
LTM2881	Complete Isolated RS485/RS422 μModule Transceiver + Power	Integrated Selectable Termination, 20Mbps, ±15kV ESD, 2500V_{RMS} Isolation with Power
LTM2882	Dual Isolated RS232 μModule Transceiver + Power	1Mbps, ±10kV ESD, 2500V_{RMS} Isolation with Power
LTM2883	SPI/Digital or I^2C μModule Isolator with Integrated DC/DC Converter	2500V_{RMS} Isolation with Adjustable ±12.5V and 5V Power in BGA Package

LT 0317 REV A • PRINTED IN USA
www.linear.com/LTM2889