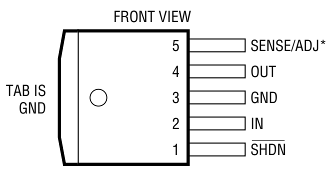
ABSOLUTE MAXIMUM RATINGS (Note 1)

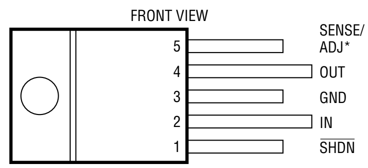
IN Pin Voltage .... ±20V
OUT Pin Voltage .... ±20V
Input to Output Differential Voltage (Note 12) .... ±20V
SENSE Pin Voltage .... ±20V
ADJ Pin Voltage .... ±7V
$\overline{\text{SHDN}}$ Pin Voltage .... ±20V
Output Short-Circuit Duration .... Indefinite
Operating Junction Temperature Range
  E Grade .... –40°C to 125°C
  MP Grade .... –55°C to 125°C
Storage Temperature Range .... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) .... 300°C

PACKAGE/ORDER INFORMATION



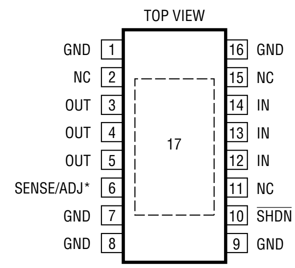
Q PACKAGE
5-LEAD PLASTIC DD

*PIN 5 = SENSE FOR LT1764A-1.5/LT1764A-1.8/LT1764A-2.5/LT1764A-3.3
= ADJ FOR LT1764A
T_{JMAX} = 150°C, θ_{JA} = 30°C/W



TAB IS GND
T PACKAGE
5-LEAD PLASTIC TO-220

*PIN 5 = SENSE FOR LT1764A-1.5/LT1764A-1.8/LT1764A-2.5/LT1764A-3.3
= ADJ FOR LT1764A
T_{JMAX} = 150°C, θ_{JA} = 50°C/W



FE PACKAGE
16-LEAD PLASTIC TSSOP
PIN 17 IS GND
T_{JMAX} = 150°C, θ_{JA} = 38°C/W

*PIN 6 = SENSE FOR LT1764A-1.5/LT1764A-1.8/LT1764A-2.5/LT1764A-3.3
= ADJ FOR LT1764A

ORDER PART NUMBER	ORDER PART NUMBER	ORDER PART NUMBER	FE PART MARKING
LT1764AEQ LT1764AEQ-1.5 LT1764AEQ-1.8 LT1764AEQ-2.5 LT1764AEQ-3.3 LT1764AMPQ	LT1764AET LT1764AET-1.5 LT1764AET-1.8 LT1764AET-2.5 LT1764AET-3.3	LT1764AEFE LT1764AEFE-1.5 LT1764AEFE-1.8 LT1764AEFE-2.5 LT1764AEFE-3.3	LT1764AEFE LT1764AEFE-1.5 LT1764AEFE-1.8 LT1764AEFE-2.5 LT1764AEFE-3.3

Order Options Tape and Reel: Add #TR
Lead Free: Add #PBF   Lead Free Tape and Reel: Add #TRPBF
Lead Free Part Marking: http://www.linear.com/leadfree/

Consult LTC Marketing for parts specified with wider operating temperature ranges.

ELECTRICAL CHARACTERISTICS

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are T_A = 25°C. (Note 2)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Minimum Input Voltage (Notes 3, 11)	I_{LOAD} = 0.5A			1.7		V
	I_{LOAD} = 1.5A			1.9		V
	E Grade: I_{LOAD} = 3A	●		2.3	2.7	V
	MP Grade: I_{LOAD} = 3A	●		2.3	2.8	V
Regulated Output Voltage (Note 4)	LT1764A-1.5 V_{IN} = 2.21V, I_{LOAD} = 1mA		1.477	1.500	1.523	V
	2.7V < V_{IN} < 20V, 1mA < I_{LOAD} < 3A	●	1.447	1.500	1.545	V
	LT1764A-1.8 V_{IN} = 2.3V, I_{LOAD} = 1mA		1.773	1.800	1.827	V
	2.8V < V_{IN} < 20V, 1mA < I_{LOAD} < 3A	●	1.737	1.800	1.854	V

ELECTRICAL CHARACTERISTICS

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are $T_A = 25°C$. (Note 2)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
	LT1764A-2.5 $V_{IN} = 3V$, $I_{LOAD} = 1mA$		2.462	2.500	2.538	V
	$3.5V < V_{IN} < 20V$, $1mA < I_{LOAD} < 3A$	●	2.412	2.500	2.575	V
	LT1764A-3.3 $V_{IN} = 3.8V$, $I_{LOAD} = 1mA$		3.250	3.300	3.350	V
	$4.3V < V_{IN} < 20V$, $1mA < I_{LOAD} < 3A$	●	3.183	3.300	3.400	V
ADJ Pin Voltage (Notes 3, 4)	LT1764A $V_{IN} = 2.21V$, $I_{LOAD} = 1mA$		1.192	1.210	1.228	V
	E Grade: $2.7V < V_{IN} < 20V$, $1mA < I_{LOAD} < 3A$	●	1.168	1.210	1.246	V
	MP Grade: $2.8V < V_{IN} < 20V$, $1mA < I_{LOAD} < 3A$	●	1.168	1.210	1.246	V
Line Regulation	LT1764A-1.5 $\Delta V_{IN} = 2.21V$ to $20V$, $I_{LOAD} = 1mA$	●		2.5	10	mV
	LT1764A-1.8 $\Delta V_{IN} = 2.3V$ to $20V$, $I_{LOAD} = 1mA$	●		3	10	mV
	LT1764A-2.5 $\Delta V_{IN} = 3V$ to $20V$, $I_{LOAD} = 1mA$	●		4	10	mV
	LT1764A-3.3 $\Delta V_{IN} = 3.8V$ to $20V$, $I_{LOAD} = 1mA$	●		4.5	10	mV
	LT1764A (Note 3) $\Delta V_{IN} = 2.21V$ to $20V$, $I_{LOAD} = 1mA$	●		2	10	mV
Load Regulation	LT1764A-1.5 $V_{IN} = 2.7V$, $\Delta I_{LOAD} = 1mA$ to $3A$			3	7	mV
	$V_{IN} = 2.7V$, $\Delta I_{LOAD} = 1mA$ to $3A$	●			23	mV
	LT1764A-1.8 $V_{IN} = 2.8V$, $\Delta I_{LOAD} = 1mA$ to $3A$			4	8	mV
	$V_{IN} = 2.8V$, $\Delta I_{LOAD} = 1mA$ to $3A$	●			25	mV
	LT1764A-2.5 $V_{IN} = 3.5V$, $\Delta I_{LOAD} = 1mA$ to $3A$			4	10	mV
	$V_{IN} = 3.5V$, $\Delta I_{LOAD} = 1mA$ to $3A$	●			30	mV
	LT1764A-3.3 $V_{IN} = 4.3V$, $\Delta I_{LOAD} = 1mA$ to $3A$			4	12	mV
	$V_{IN} = 4.3V$, $\Delta I_{LOAD} = 1mA$ to $3A$	●			40	mV
	LT1764A (Note 3) $V_{IN} = 2.7V$, $\Delta I_{LOAD} = 1mA$ to $3A$			2	5	mV
	E Grade: $V_{IN} = 2.7V$, $\Delta I_{LOAD} = 1mA$ to $3A$	●			20	mV
	MP Grade: $V_{IN} = 2.8V$, $\Delta I_{LOAD} = 1mA$ to $3A$	●			20	mV
Dropout Voltage $V_{IN} = V_{OUT(NOMINAL)}$ (Notes 5, 6, 11)	$I_{LOAD} = 1mA$			0.02	0.05	V
	$I_{LOAD} = 1mA$	●			0.10	V
	$I_{LOAD} = 100mA$			0.07	0.13	V
	$I_{LOAD} = 100mA$	●			0.18	V
	$I_{LOAD} = 500mA$			0.14	0.20	V
	$I_{LOAD} = 500mA$	●			0.27	V
	$I_{LOAD} = 1.5A$			0.25	0.33	V
	$I_{LOAD} = 1.5A$	●			0.40	V
	$I_{LOAD} = 3A$			0.34	0.45	V
	$I_{LOAD} = 3A$	●			0.66	V
GND Pin Current $V_{IN} = V_{OUT(NOMINAL)} + 1V$ (Notes 5, 7)	$I_{LOAD} = 0mA$	●		1	1.5	mA
	$I_{LOAD} = 1mA$	●		1.1	1.6	mA
	$I_{LOAD} = 100mA$	●		3.5	5	mA
	$I_{LOAD} = 500mA$	●		11	18	mA
	$I_{LOAD} = 1.5A$	●		40	75	mA
	$I_{LOAD} = 3A$	●		120	200	mA
Output Voltage Noise	$C_{OUT} = 10\mu F$, $I_{LOAD} = 3A$, BW = 10Hz to 100kHz			40		μV_{RMS}
ADJ Pin Bias Current	(Notes 3, 8)			3	10	µA
Shutdown Threshold	V_{OUT} = Off to On	●		0.9	2	V
	V_{OUT} = On to Off	●	0.25	0.75		V
$\overline{SHDN}$ Pin Current (Note 9)	$V_{\overline{SHDN}} = 0V$			0.01	1	µA
	$V_{\overline{SHDN}} = 20V$			7	30	µA
Quiescent Current in Shutdown	$V_{IN} = 6V$, $V_{\overline{SHDN}} = 0V$			0.01	1	µA
Ripple Rejection	$V_{IN} - V_{OUT} = 1.5V$ (Avg), $V_{RIPPLE} = 0.5V_{P-P}$, $f_{RIPPLE} = 120Hz$, $I_{LOAD} = 1.5A$		55	63		dB

ELECTRICAL CHARACTERISTICS

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are T_A = 25°C. (Note 2)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Current Limit	V_{IN} = 7V, V_{OUT} = 0V			4		A
	E Grade: LT1764A; LT1764A-1.5; V_{IN} = 2.7V, ΔV_{OUT} = –0.1V	●	3.1			A
	MP Grade: LT1764A V_{IN} = 2.8V, ΔV_{OUT} = –0.1V	●	3.1			A
Input Reverse Leakage Current	V_{IN} = –20V, V_{OUT} = 0V	●			1	mA
Reverse Output Current (Note 10)	LT1764A-1.5 V_{OUT} = 1.5V, V_{IN} < 1.5V LT1764A-1.8 V_{OUT} = 1.8V, V_{IN} < 1.8V LT1764A-2.5 V_{OUT} = 2.5V, V_{IN} < 2.5V LT1764A-3.3 V_{OUT} = 3.3V, V_{IN} < 3.3V LT1764A (Note 3) V_{OUT} = 1.21V, V_{IN} < 1.21V			600 600 600 600 300	1200 1200 1200 1200 600	µA µA µA µA µA

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The LT1764A regulators are tested and specified under pulse load conditions such that $T_J \approx T_A$. The LT1764A (E grade) is 100% tested at T_A = 25°C; performance at –40°C and 125°C is assured by design, characterization and correlation with statistical process controls. The LT1764A (MP grade) is 100% tested and guaranteed over the –55°C to 125°C temperature range.

Note 3: The LT1764A (adjustable version) is tested and specified for these conditions with the ADJ pin connected to the OUT pin.

Note 4. Operating conditions are limited by maximum junction temperature. The regulated output voltage specification will not apply for all possible combinations of input voltage and output current. When operating at maximum input voltage, the output current range must be limited. When operating at maximum output current, the input voltage range must be limited.

Note 5: To satisfy requirements for minimum input voltage, the LT1764A (adjustable version) is tested and specified for these conditions with an external resistor divider (two 4.12k resistors) for an output voltage of 2.42V. The external resistor divider will add a 300µA DC load on the output.

Note 6: Dropout voltage is the minimum input to output voltage differential needed to maintain regulation at a specified output current. In dropout, the output voltage will be equal to: $V_{IN} – V_{DROPOUT}$.

Note 7: GND pin current is tested with $V_{IN} = V_{OUT(NOMINAL)}$ + 1V or V_{IN} = 2.7V (E grade) or V_{IN} = 2.8V (MP grade), whichever is greater, and a current source load. The GND pin current will decrease at higher input voltages.

Note 8: ADJ pin bias current flows into the ADJ pin.

Note 9: $\overline{\text{SHDN}}$ pin current flows into the $\overline{\text{SHDN}}$ pin.

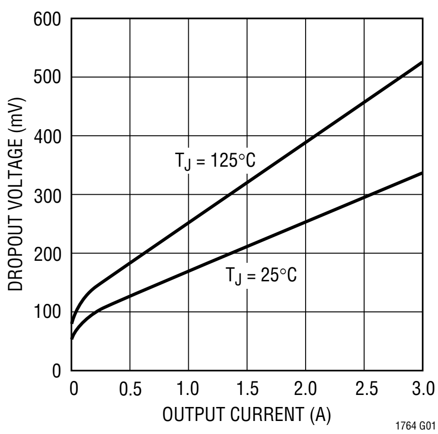
Note 10: Reverse output current is tested with the IN pin grounded and the OUT pin forced to the rated output voltage. This current flows into the OUT pin and out the GND pin.

Note 11. For the LT1764A, LT1764A-1.5 and LT1764A-1.8 dropout voltage will be limited by the minimum input voltage specification under some output voltage/load conditions.

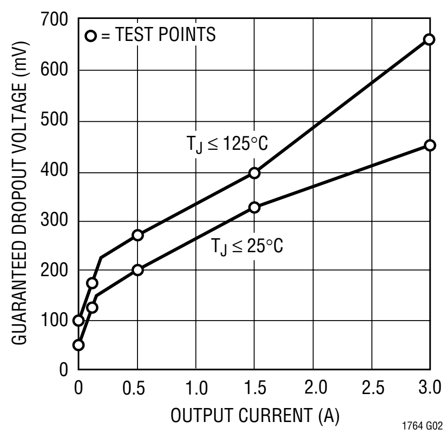
Note 12. All combinations of absolute maximum input voltage and absolute maximum output voltage cannot be achieved. The absolute maximum differential from input to output is ±20V. For example, with V_{IN} = 20V, V_{OUT} cannot be pulled below ground.

TYPICAL PERFORMANCE CHARACTERISTICS

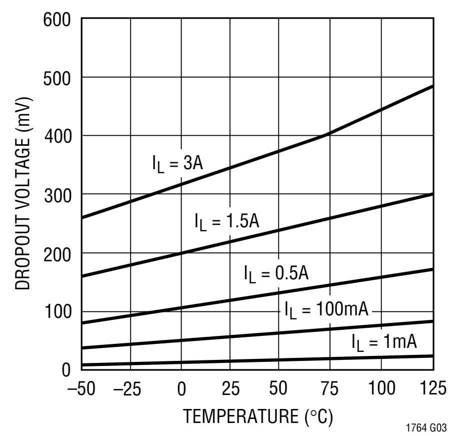
Typical Dropout Voltage



Guaranteed Dropout Voltage

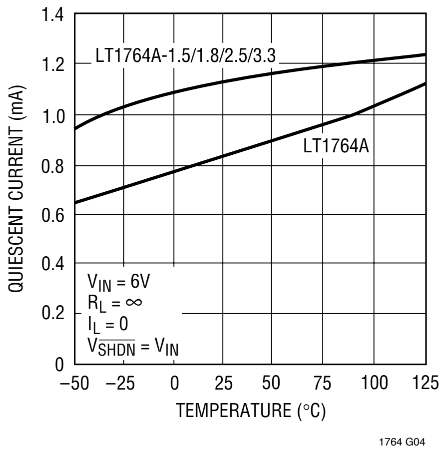


Dropout Voltage

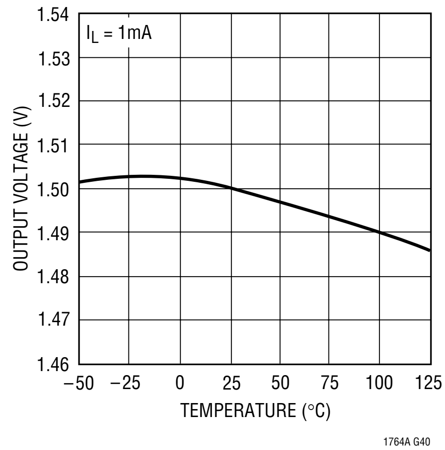


TYPICAL PERFORMANCE CHARACTERISTICS

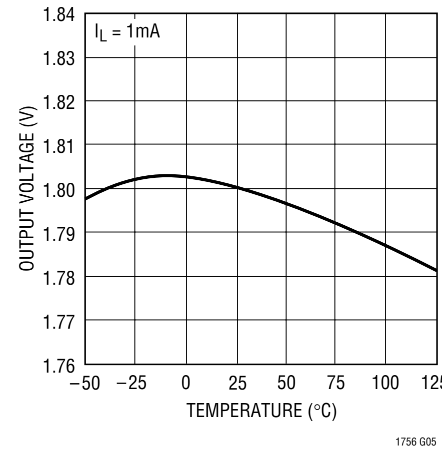
Quiescent Current



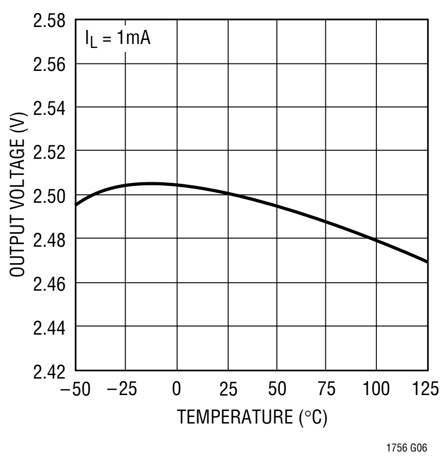
LT1764A-1.5 Output Voltage



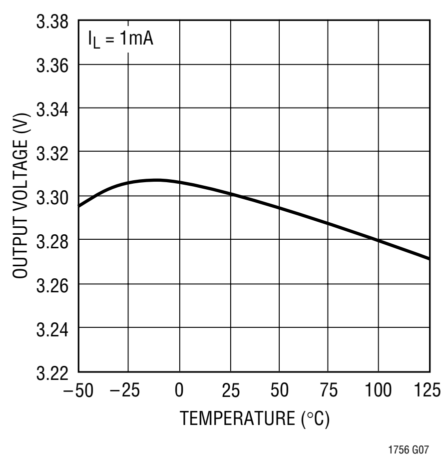
LT1764A-1.8 Output Voltage



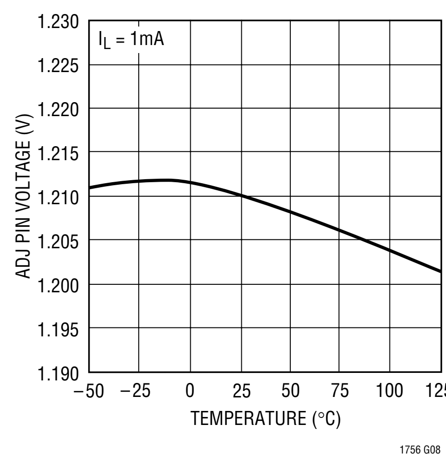
LT1764A-2.5 Output Voltage



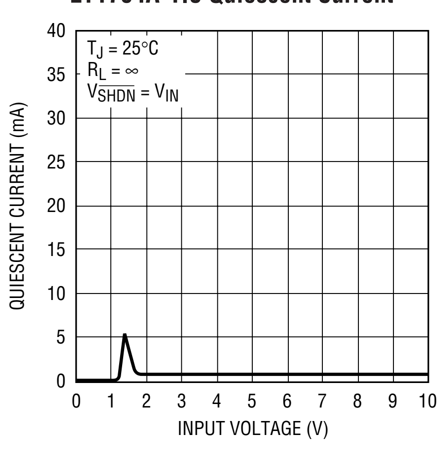
LT1764A-3.3 Output Voltage



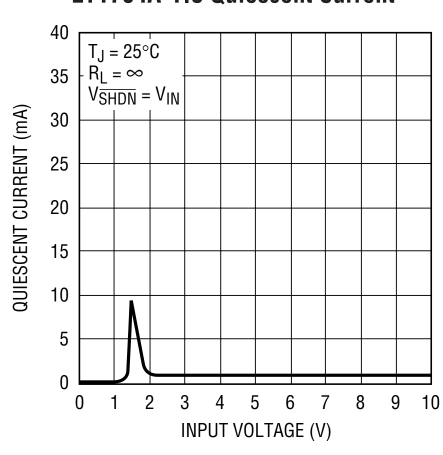
LT1764A ADJ Pin Voltage



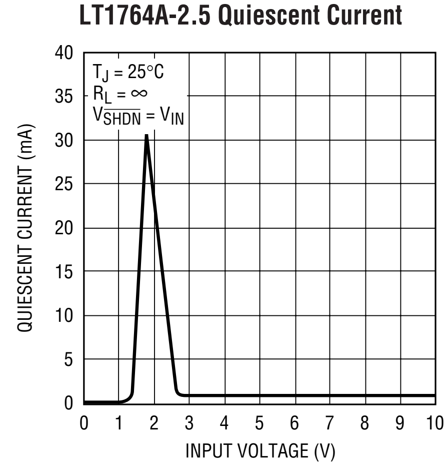
LT1764A-1.5 Quiescent Current



LT1764A-1.8 Quiescent Current

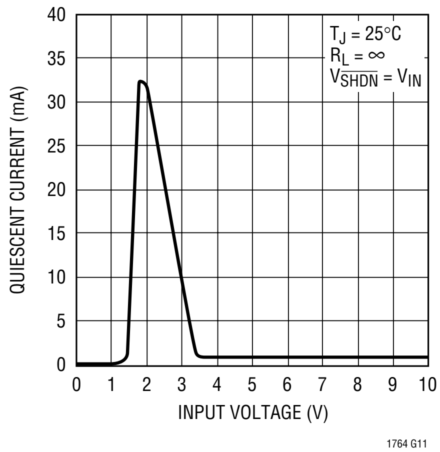


LT1764A-2.5 Quiescent Current

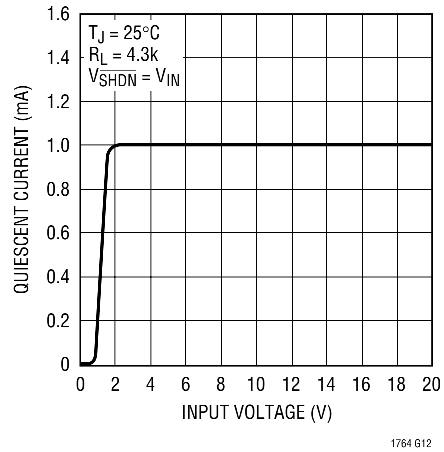


TYPICAL PERFORMANCE CHARACTERISTICS

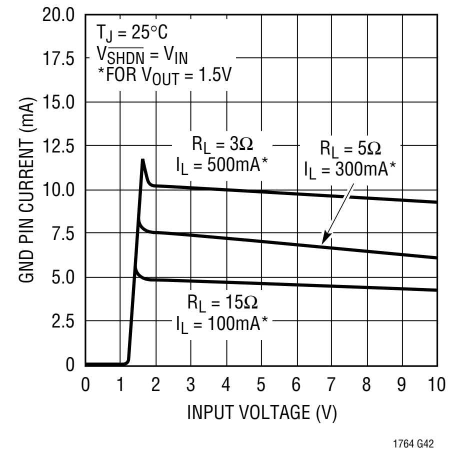
LT1764A-3.3 Quiescent Current



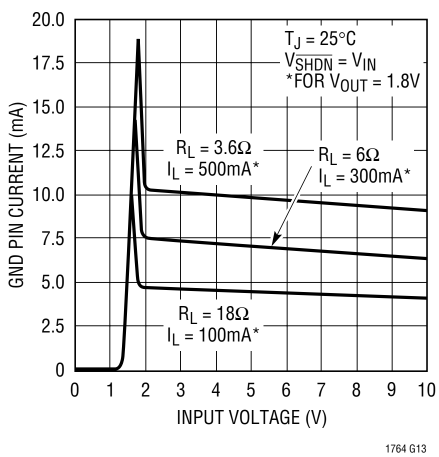
LT1764A Quiescent Current



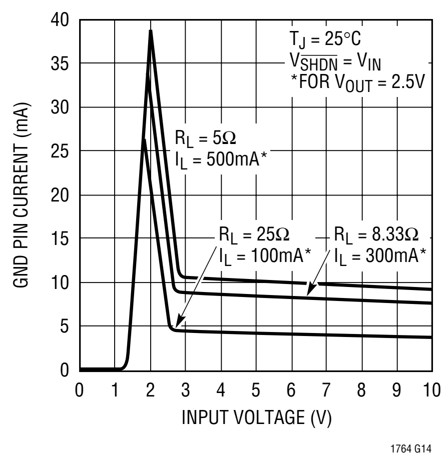
LT1764A-1.5 GND Pin Current



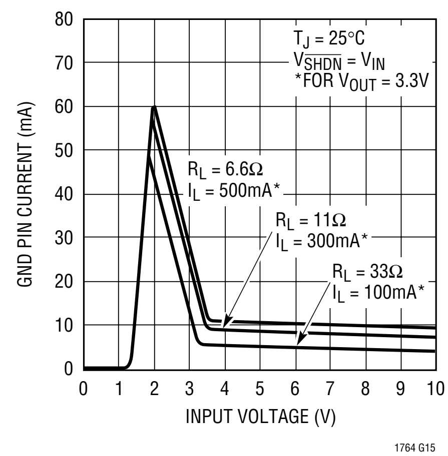
LT1764A-1.8 GND Pin Current



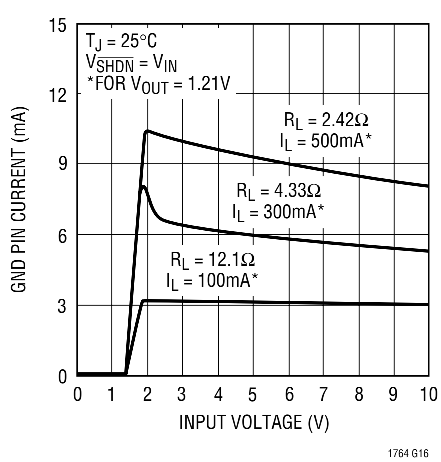
LT1764A-2.5 GND Pin Current



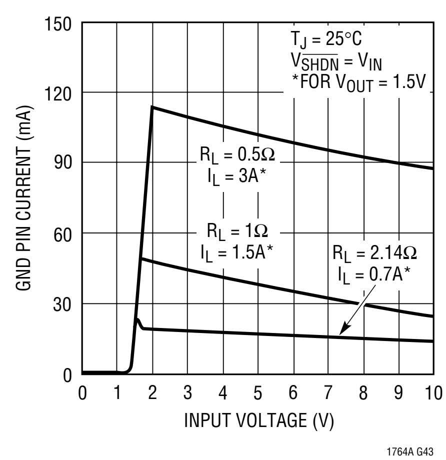
LT1764A-3.3 GND Pin Current



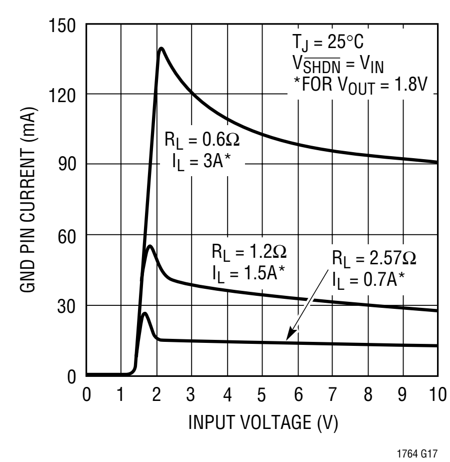
LT1764A GND Pin Current



LT1764A-1.5 GND Pin Current

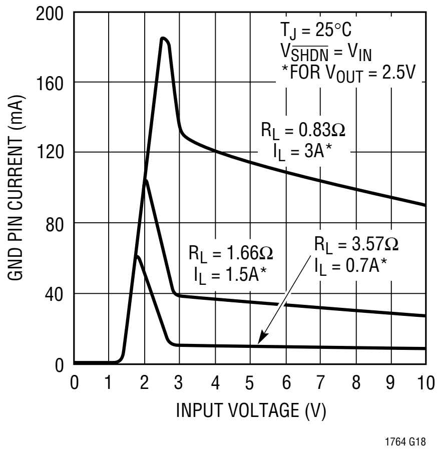


LT1764A-1.8 GND Pin Current

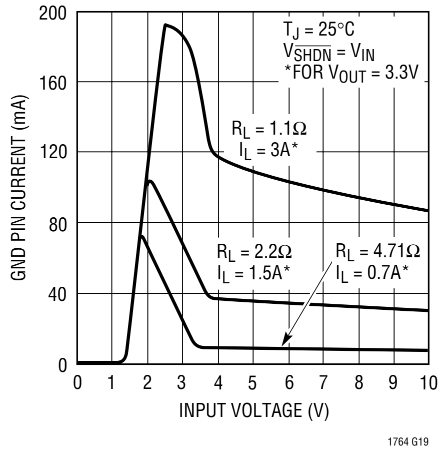


TYPICAL PERFORMANCE CHARACTERISTICS

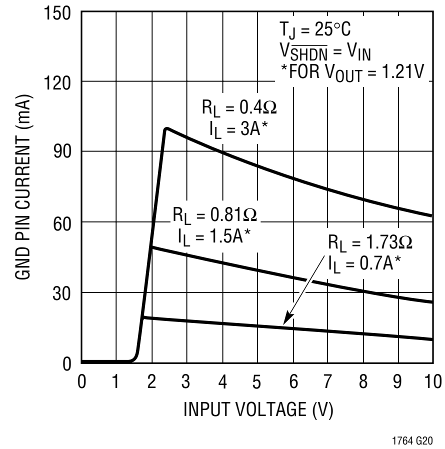
LT1764A-2.5 GND Pin Current



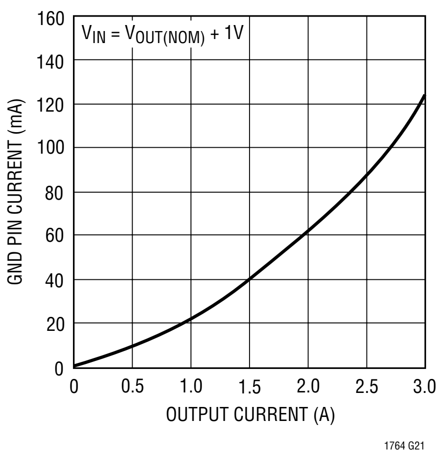
LT1764A-3.3 GND Pin Current



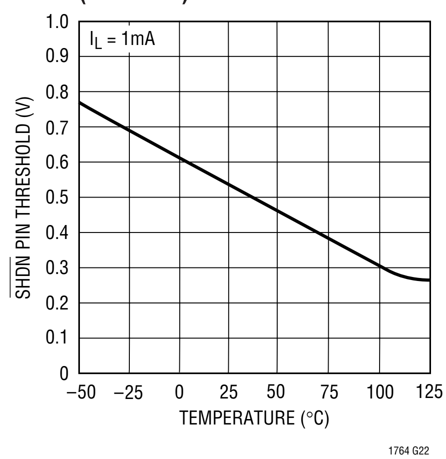
LT1764A GND Pin Current



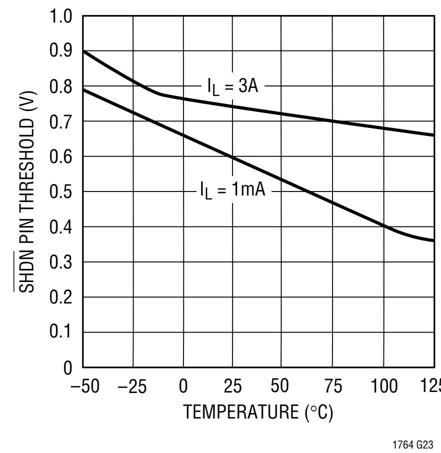
GND Pin Current vs I_{LOAD}



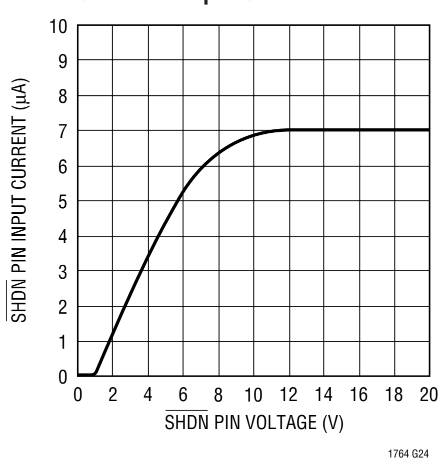
$\overline{SHDN}$ Pin Threshold (On-to-Off)



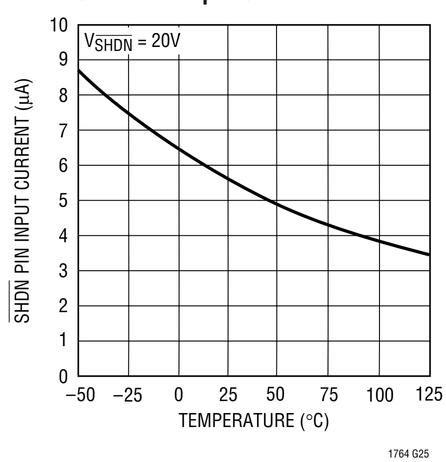
$\overline{SHDN}$ Pin Threshold (Off-to-On)



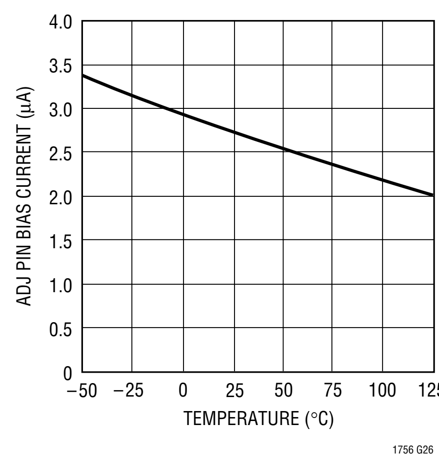
$\overline{SHDN}$ Pin Input Current



$\overline{SHDN}$ Pin Input Current

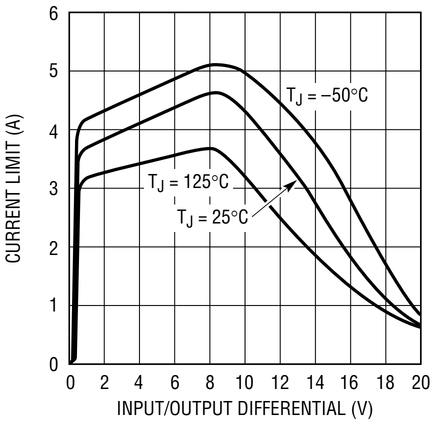


ADJ Pin Bias Current

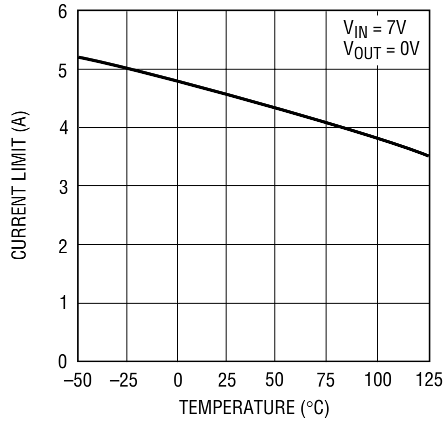


TYPICAL PERFORMANCE CHARACTERISTICS

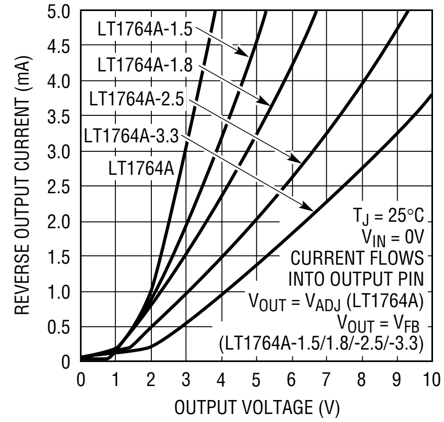
Current Limit



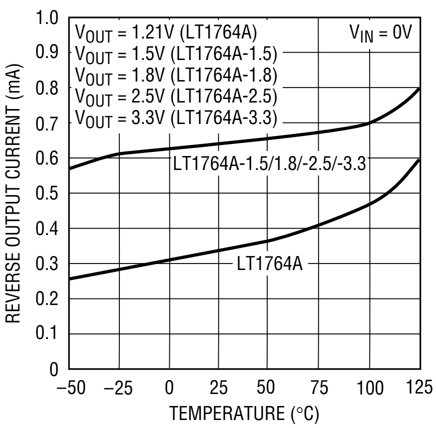
Current Limit



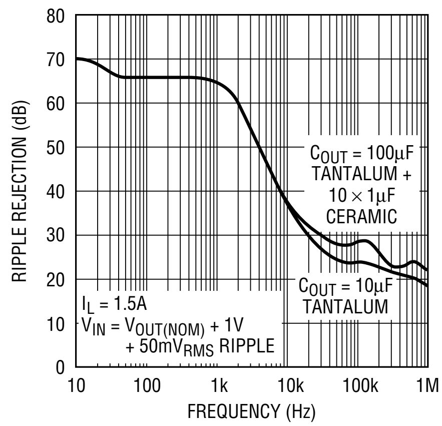
Reverse Output Current



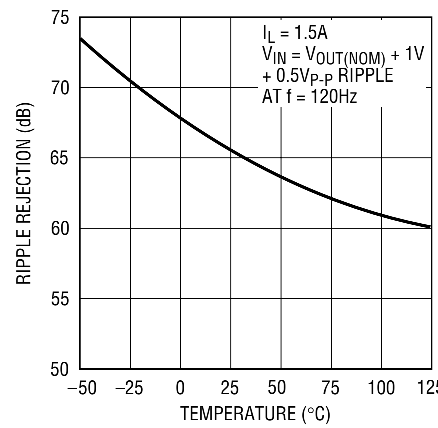
Reverse Output Current



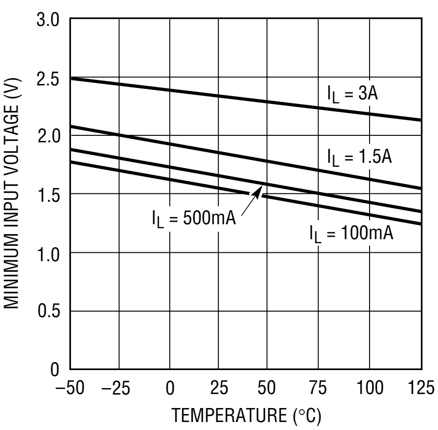
Ripple Rejection



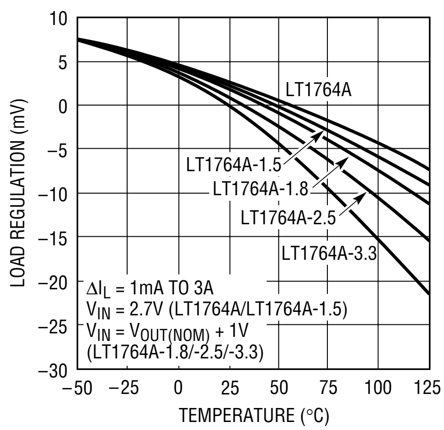
Ripple Rejection



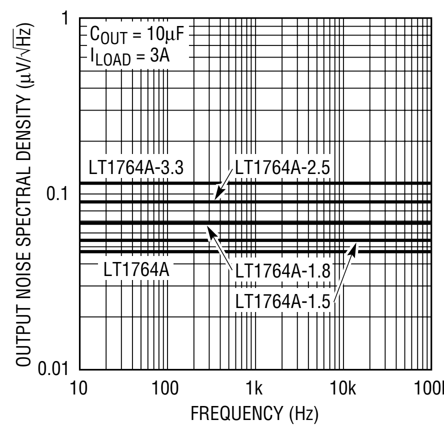
LT1764A Minimum Input Voltage



Load Regulation

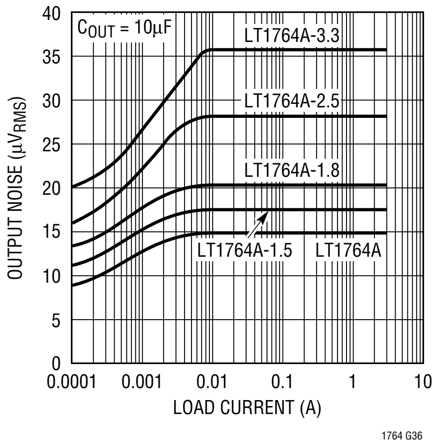


Output Noise Spectral Density

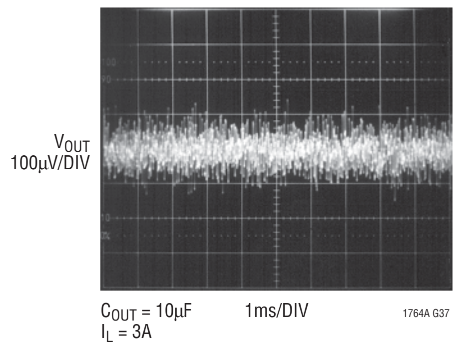


TYPICAL PERFORMANCE CHARACTERISTICS

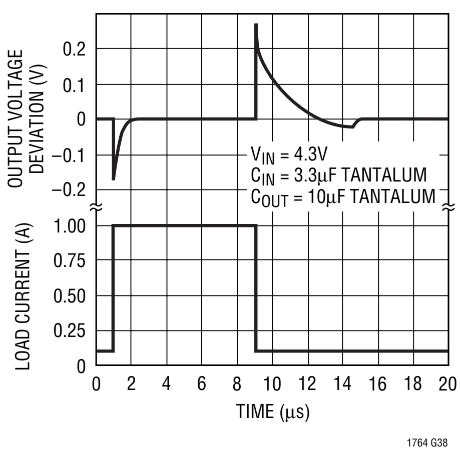
RMS Output Noise vs Load Current (10Hz to 100kHz)



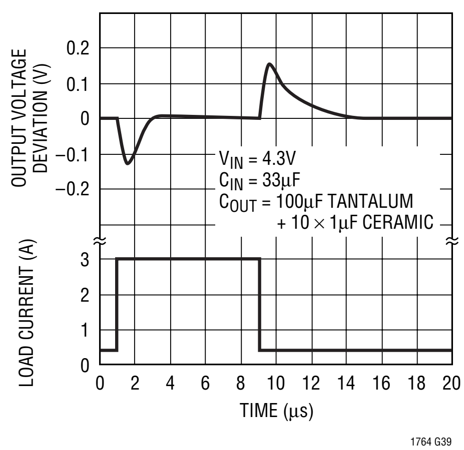
LT1764A-3.3 10Hz to 100kHz Output Noise



LT1764A-3.3 Transient Response



LT1764A-3.3 Transient Response



PIN FUNCTIONS DD/TO-220/TSSOP

SHDN (Pin 1/1/10): Shutdown. The SHDN pin is used to put the LT1764A regulators into a low power shutdown state. The output will be off when the SHDN pin is pulled low. The SHDN pin can be driven either by 5V logic or open-collector logic with a pull-up resistor. The pull-up resistor is required to supply the pull-up current of the open-collector gate, normally several microamperes, and the SHDN pin current, typically 7μA. If unused, the SHDN pin must be connected to V_{IN}. The device will be in the low power shutdown state if the SHDN pin is not connected.

IN (Pin 2/Pin 2/Pins 12, 13, 14): Input. Power is supplied to the device through the IN pin. A bypass capacitor is required on this pin if the device is more than six inches away from the main input filter capacitor. In general, the output impedance of a battery rises with frequency, so it is advisable to include a bypass capacitor in battery-powered circuits. A bypass capacitor in the range of 1μF to 10μF is sufficient. The LT1764A regulators are designed to withstand reverse voltages on the IN pin with respect to ground and the OUT pin. In the case of a reverse input, which can happen if a battery is plugged in backwards, the device will act as if there is a diode in series with its input. There will be no reverse current flow into the regulator and no reverse voltage will appear at the load. The device will protect both itself and the load.

NC (Pins 2, 11, 15) TSSOP Only: No Connect.

GND (Pin 3/Pin 3/Pins 1, 7, 8, 9, 16, 17): Ground.

OUT (Pin 4/Pin 4/Pins 3, 4, 5): Output. The output supplies power to the load. A minimum output capacitor of 10μF is required to prevent oscillations. Larger output capacitors will be required for applications with large transient loads to limit peak voltage transients. See the Applications Information section for more information on output capacitance and reverse output characteristics.

SENSE (Pin 5/Pin 5/Pin 6): Sense. For fixed voltage versions of the LT1764A (LT1764A-1.5/LT1764A-1.8/LT1764A-2.5/LT1764A-3.3), the SENSE pin is the input to the error amplifier. Optimum regulation will be obtained at the point where the SENSE pin is connected to the OUT pin of the regulator. In critical applications, small voltage drops are caused by the resistance (R_P) of PC traces between the regulator and the load. These may be eliminated by connecting the SENSE pin to the output at the load as shown in Figure 1 (Kelvin Sense Connection). Note that the voltage drop across the external PC traces will add to the dropout voltage of the regulator. The SENSE pin bias current is 600μA at the nominal rated output voltage. The SENSE pin can be pulled below ground (as in a dual supply system where the regulator load is returned to a negative supply) and still allow the device to start and operate.

ADJ (Pin 5/Pin 5/Pin 6): Adjust. For the adjustable LT1764A, this is the input to the error amplifier. This pin is internally clamped to ±7V. It has a bias current of 3μA which flows into the pin. The ADJ pin voltage is 1.21V referenced to ground and the output voltage range is 1.21V to 20V.

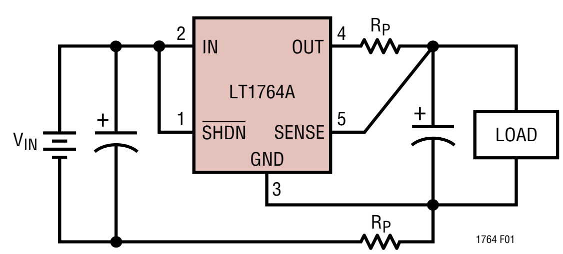


Figure 1. Kelvin Sense Connection

APPLICATIONS INFORMATION

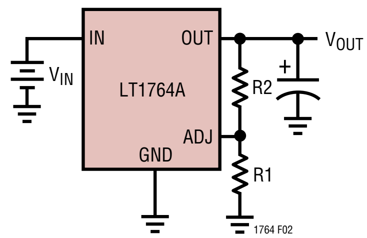
The LT1764A series are 3A low dropout regulators optimized for fast transient response. The devices are capable of supplying 3A at a dropout voltage of 340mV. The low operating quiescent current (1mA) drops to less than 1μA in shutdown. In addition to the low quiescent current, the LT1764A regulators incorporate several protection features which make them ideal for use in battery-powered systems. The devices are protected against both reverse input and reverse output voltages. In battery backup applications where the output can be held up by a backup battery when the input is pulled to ground, the LT1764A-X acts like it has a diode in series with its output and prevents reverse current flow. Additionally, in dual supply applications where the regulator load is returned to a negative supply, the output can be pulled below ground by as much as 20V and still allow the device to start and operate.

Adjustable Operation

The adjustable version of the LT1764A has an output voltage range of 1.21V to 20V. The output voltage is set by the ratio of two external resistors as shown in Figure 2. The device servos the output to maintain the voltage at the ADJ pin at 1.21V referenced to ground. The current in R1 is then equal to 1.21V/R1 and the current in R2 is the current in R1 plus the ADJ pin bias current. The ADJ pin bias current, 3μA at 25°C, flows through R2 into the ADJ pin. The output voltage can be calculated using the formula in Figure 2. The value of R1 should be less than 4.17k to minimize errors in the output voltage caused by the ADJ pin bias current. Note that in shutdown the output is turned off and the divider current will be zero.

The adjustable device is tested and specified with the ADJ pin tied to the OUT pin for an output voltage of 1.21V. Specifications for output voltages greater than 1.21V will be proportional to the ratio of the desired output voltage to 1.21V: V_{OUT}/1.21V. For example, load regulation for an output current change of 1mA to 3A is –3mV typical at V_{OUT} = 1.21V. At V_{OUT} = 5V, load regulation is:

$$(5V/1.21V)(–3mV) = –12.4mV$$



$$V_{OUT} = 1.21V\left(1+\frac{R2}{R1}\right)+(I_{ADJ})(R2)$$

$V_{ADJ} = 1.21V$

$I_{ADJ} = 3\mu A$ AT 25°C

OUTPUT RANGE = 1.21V TO 20V

Figure 2. Adjustable Operation

Output Capacitors and Stability

The LT1764A regulator is a feedback circuit. Like any feedback circuit, frequency compensation is needed to make it stable. For the LT1764A, the frequency compensation is both internal and external—the output capacitor. The size of the output capacitor, the type of the output capacitor, and the ESR of the particular output capacitor all affect the stability.

In addition to stability, the output capacitor also affects the high frequency transient response. The regulator loop has a finite band width. For high frequency transient loads, recovery from a transient is a combination of the output capacitor and the bandwidth of the regulator. The LT1764A was designed to be easy to use and accept a wide variety of output capacitors. However, the frequency compensation is affected by the output capacitor and optimum frequency stability may require some ESR, especially with ceramic capacitors.

For ease of use, low ESR polytantalum capacitors (POSCAP) are a good choice for both the transient response and stability of the regulator. These capacitors have intrinsic ESR that improves the stability. Ceramic capacitors have extremely low ESR, and while they are a good choice in many cases, placing a small series resistance element will sometimes achieve optimum stability and minimize ringing. In all cases, a minimum of 10μF is required while the maximum ESR allowable is 3Ω.

The place where ESR is most helpful with ceramics is low output voltage. At low output voltages, below 2.5V, some ESR helps the stability when ceramic output capacitors are used. Also, some ESR allows a smaller capacitor value to be used. When small signal ringing occurs with ceramics due to insufficient ESR, adding ESR or increas-

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ing the capacitor value improves the stability and reduces the ringing. Table 1 gives some recommended values of ESR to minimize ringing caused by fast, hard current transitions.

Table 1. Capacitor Minimum ESR

V_{OUT}	10µF	22µF	47µF	100µF
1.2V	10mΩ	5mΩ	3mΩ	0mΩ
1.5V	7mΩ	5mΩ	3mΩ	0mΩ
1.8V	5mΩ	5mΩ	3mΩ	0mΩ
2.5V	0mΩ	0mΩ	0mΩ	0mΩ
3.3V	0mΩ	0mΩ	0mΩ	0mΩ
≥ 5V	0mΩ	0mΩ	0mΩ	0mΩ

Figures 3 through 8 show the effect of ESR on the transient response of the regulator. These scope photos show the transient response for the LT1764A at three different output voltages with various capacitors and various values of ESR. The output load conditions are the same for all traces. In all cases there is a DC load of 1A. The load steps up to 2A at the first transition and steps back to 1A at the second transition.

At the worst case point of $1.2V_{OUT}$ with 10µF C_{OUT} (Figure 3), a minimum amount of ESR is required. While 5mΩ is enough to eliminate most of the ringing, a value closer to 20mΩ provides a more optimum response. At 2.5V output with 10µF C_{OUT} (Figure 4) the output rings at the transitions with 0Ω ESR but still settles to within 10mV in 20µs after the 1A load step. Once again a small value of ESR will provide a more optimum response.

At $5V_{OUT}$ with 10µF C_{OUT} (Figure 5) the response is well damped with 0Ω ESR.

With a C_{OUT} of 100µF at 0Ω ESR and an output of 1.2V (Figure 6), the output rings although the amplitude is only $10mV_{p-p}$. With C_{OUT} of 100µF it takes only 5mΩ to 20mΩ of ESR to provide good damping at 1.2V output. Performance at 2.5V and 5V output with 100µF C_{OUT} shows similar characteristics to the 10µF case (see Figures 7-8). At $2.5V_{OUT}$ 5mΩ to 20mΩ can improve transient response. At $5V_{OUT}$ the response is well damped with 0Ω ESR.

Capacitor types with inherently higher ESR can be combined with 0mΩ ESR ceramic capacitors to achieve both good high frequency bypassing and fast settling time. Figure 9 illustrates the improvement in transient response that can be seen when a parallel combination of ceramic and POSCAP capacitors are used. The output voltage is at the worst case value of 1.2V. Trace A, is with a 10µF ceramic output capacitor and shows significant ringing with a peak amplitude of 25mV. For Trace B, a 22µF/45mΩ POSCAP is added in parallel with the 10µF ceramic. The output is well damped and settles to within 10mV in less than 5µs.

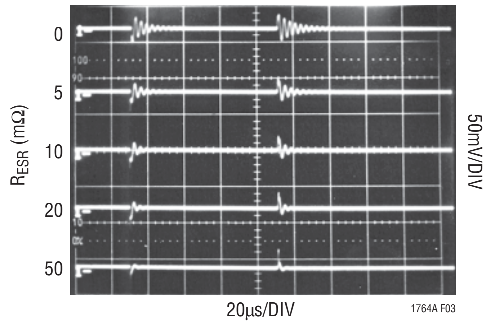
For Trace C, a 100µF/35mΩ POSCAP is connected in parallel with the 10µF ceramic capacitor. In this case the peak output deviation is less than 20mV and the output settles in about 5µs. For improved transient response the value of the bulk capacitor (tantalum or aluminum electrolytic) should be greater than twice the value of the ceramic capacitor.

Tantalum and Polytantalum Capacitors

There is a variety of tantalum capacitor types available, with a wide range of ESR specifications. Older types have ESR specifications in the hundreds of mΩ to several Ohms. Some newer types of polytantalum with multi-electrodes have maximum ESR specifications as low as 5mΩ. In general the lower the ESR specification, the larger the size and the higher the price. Polytantalum capacitors have better surge capability than older types and generally lower ESR. Some types such as the Sanyo TPE and TPB series have ESR specifications in the 20mΩ to 50mΩ range, which provide near optimum transient response.

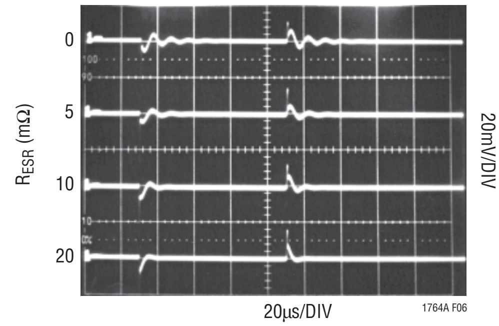
Aluminum Electrolytic Capacitors

Aluminum electrolytic capacitors can also be used with the LT1764. These capacitors can also be used in conjunction with ceramic capacitors. These tend to be the cheapest and lowest performance type of capacitors. Care must be used in selecting these capacitors as some types can have ESR which can easily exceed the 3Ω maximum value.



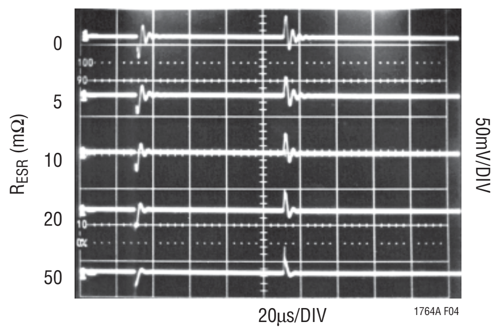
V_{OUT} = 1.2V
I_{OUT} = 1A WITH
1A PULSE
C_{OUT} = 10µF CERAMIC

Figure 3



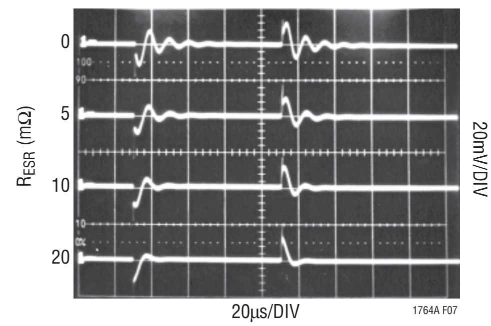
V_{OUT} = 1.2V
I_{OUT} = 1A WITH
1A PULSE
C_{OUT} = 100µF CERAMIC

Figure 6



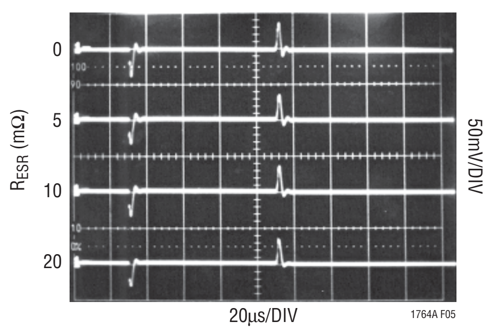
V_{OUT} = 2.5V
I_{OUT} = 1A WITH
1A PULSE
C_{OUT} = 10µF CERAMIC

Figure 4



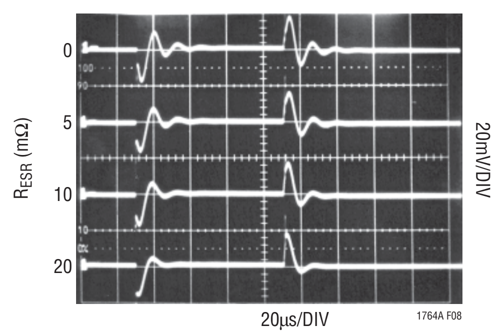
V_{OUT} = 2.5V
I_{LOAD} = 1A WITH
1A PULSE
C_{OUT} = 100µF CERAMIC

Figure 7



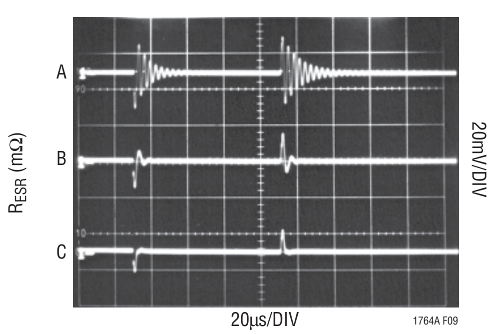
V_{OUT} = 5V
I_{OUT} = 1A WITH
1A PULSE
C_{OUT} = 10µF CERAMIC

Figure 5



V_{OUT} = 5V
I_{LOAD} = 1A WITH
1A PULSE
C_{OUT} = 100µF CERAMIC

Figure 8



V_{OUT} = 1.2V
I_{OUT} = 1A WITH 1A PULSE
C_{OUT} =
A = 10µF CERAMIC
B = 10µF CERAMIC IN PARALLEL WITH 22µF/
45mΩ POLY
C = 10µF CERAMIC IN PARALLEL WITH 100µF/
35mΩ POLY

Figure 9

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Ceramic Capacitors

Extra consideration must be given to the use of ceramic capacitors. Ceramic capacitors are manufactured with a variety of dielectrics, each with different behavior over temperature and applied voltage. The most common dielectrics used are Z5U, Y5V, X5R and X7R. The Z5U and Y5V dielectrics are good for providing high capacitances in a small package, but exhibit strong voltage and temperature coefficients as shown in Figures 3 and 4. When used with a 5V regulator, a 10µF Y5V capacitor can exhibit an effective value as low as 1µF to 2µF over the operating temperature range. The X5R and X7R dielectrics result in more stable characteristics and are more suitable for use as the output capacitor. The X7R type has better stability across temperature, while the X5R is less expensive and is available in higher values.

Voltage and temperature coefficients are not the only sources of problems. Some ceramic capacitors have a piezoelectric response. A piezoelectric device generates voltage across its terminals due to mechanical stress, similar to the way a piezoelectric accelerometer or microphone works. For a ceramic capacitor the stress can be induced by vibrations in the system or thermal transients.

"FREE" Resistance with PC Traces

The resistance values shown in Table 1 can easily be made using a small section of PC trace in series with the output capacitor. The wide range of noncritical ESR makes it easy to use PC trace. The trace width should be sized to handle the RMS ripple current associated with the load. The output capacitor only sources or sinks current for a few microseconds during fast output current transitions. There

Table 2. PC Trace Resistors

		10mΩ	20mΩ	30mΩ
0.5oz C_U	Width	0.011" (0.28mm)	0.011" (0.28mm)	0.011" (0.28mm)
	Length	0.102" (2.6mm)	0.204" (5.2mm)	0.307" (7.8mm)
1.0oz C_U	Width	0.006" (0.15mm)	0.006" (0.15mm)	0.006" (0.15mm)
	Length	0.110" (2.8mm)	0.220" (5.6mm)	0.330" (8.4mm)
2.0oz C_U	Width	0.006" (0.15mm)	0.006" (0.15mm)	0.006" (0.15mm)
	Length	0.224" (5.7mm)	0.450" (11.4mm)	0.670" (17mm)

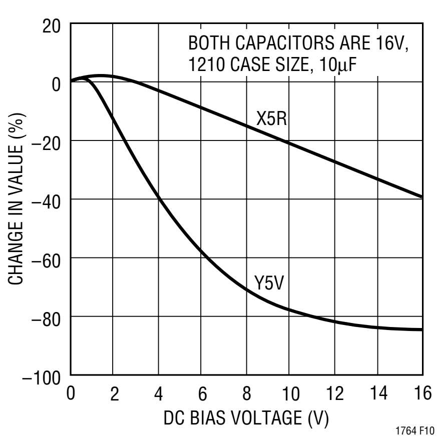

Figure 3. Ceramic Capacitor DC Bias Characteristics

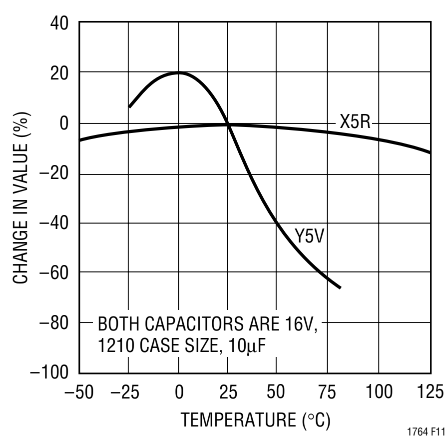

Figure 4. Ceramic Capacitor Temperature Characteristics

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is no DC current in the output capacitor. Worst case ripple current will occur if the output load is a high frequency (>100kHz) square wave with a high peak value and fast edges (< 1µs). Measured RMS value for this case is 0.5 times the peak-to-peak current change. Slower edges or lower frequency will significantly reduce the RMS ripple current in the capacitor.

This resistor should be made using one of the inner layers of the PC board which are well defined. The resistivity is determined primarily by the sheet resistance of the copper laminate with no additional plating steps. Table 2 gives some sizes for 0.75A RMS current for various copper thicknesses. More detailed information regarding resistors made from PC traces can be found in Application Note 69, Appendix A.

Overload Recovery

Like many IC power regulators, the LT1764A-X has safe operating area protection. The safe area protection decreases the current limit as input-to-output voltage increases and keeps the power transistor inside a safe operating region for all values of input-to-output voltage. The protection is designed to provide some output current at all values of input-to-output voltage up to the device breakdown.

When power is first turned on, as the input voltage rises, the output follows the input, allowing the regulator to start up into very heavy loads. During the start-up, as the input voltage is rising, the input-to-output voltage differential is small, allowing the regulator to supply large output currents. With a high input voltage, a problem can occur wherein removal of an output short will not allow the output voltage to recover. Other regulators, such as the LT1085, also exhibit this phenomenon, so it is not unique to the LT1764A series.

The problem occurs with a heavy output load when the input voltage is high and the output voltage is low. Common situations are immediately after the removal of a short circuit or when the $\overline{\text{SHDN}}$ pin is pulled high after the input voltage has already been turned on. The load line for such a load may intersect the output current curve at two points. If this happens, there are two stable output operating points for the regulator. With this double intersection, the input power supply may need to be cycled down to zero and brought up again to make the output recover.

Output Voltage Noise

The LT1764A regulators have been designed to provide low output voltage noise over the 10Hz to 100kHz bandwidth while operating at full load. Output voltage noise is typically $50nV\sqrt{Hz}$ over this frequency bandwidth for the LT1764A (adjustable version). For higher output voltages (generated by using a resistor divider), the output voltage noise will be gained up accordingly. This results in RMS noise over the 10Hz to 100kHz bandwidth of $15\mu V_{RMS}$ for the LT1764A increasing to $37\mu V_{RMS}$ for the LT1764A-3.3.

Higher values of output voltage noise may be measured when care is not exercised with regards to circuit layout and testing. Crosstalk from nearby traces can induce unwanted noise onto the output of the LT1764A-X. Power supply ripple rejection must also be considered; the LT1764A regulators do not have unlimited power supply rejection and will pass a small portion of the input noise through to the output.

Thermal Considerations

The power handling capability of the device is limited by the maximum rated junction temperature (125°C). The power dissipated by the device is made up of two components:

1. Output current multiplied by the input/output voltage differential: $(I_{OUT})(V_{IN} – V_{OUT})$, and
2. GND pin current multiplied by the input voltage: $(I_{GND})(V_{IN})$.

The GND pin current can be found using the GND Pin Current curves in the Typical Performance Characteristics. Power dissipation will be equal to the sum of the two components listed above.

The LT1764A series regulators have internal thermal limiting designed to protect the device during overload conditions. For continuous normal conditions, the maximum junction temperature rating of 125°C must not be exceeded. It is important to give careful consideration to

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all sources of thermal resistance from junction to ambient. Additional heat sources mounted nearby must also be considered.

For surface mount devices, heat sinking is accomplished by using the heat spreading capabilities of the PC board and its copper traces. Surface mount heatsinks and plated through-holes can also be used to spread the heat generated by power devices.

The following table lists thermal resistance for several different board sizes and copper areas. All measurements were taken in still air on 1/16" FR-4 board with one ounce copper.

Table 3. Q Package, 5-Lead DD

COPPER AREA			THERMAL RESISTANCE
TOPSIDE*	BACKSIDE	BOARD AREA	(JUNCTION-TO-AMBIENT)
2500mm^2	2500mm^2	2500mm^2	23°C/W
1000mm^2	2500mm^2	2500mm^2	25°C/W
125mm^2	2500mm^2	2500mm^2	33°C/W

*Device is mounted on topside.

T Package, 5-Lead TO-220
Thermal Resistance (Junction-to-Case) = 2.5°C/W

Calculating Junction Temperature

Example: Given an output voltage of 3.3V, an input voltage range of 4V to 6V, an output current range of 0mA to 500mA and a maximum ambient temperature of 50°C, what will the maximum junction temperature be?

The power dissipated by the device will be equal to:

$$I_{OUT(MAX)}(V_{IN(MAX)} - V_{OUT}) + I_{GND}(V_{IN(MAX)})$$

where,

$I_{OUT(MAX)} = 500mA$
$V_{IN(MAX)} = 6V$
I_{GND} at ($I_{OUT} = 500mA$, $V_{IN} = 6V$) = 10mA

So,

$$P = 500mA(6V - 3.3V) + 10mA(6V) = 1.41W$$

Using a DD package, the thermal resistance will be in the range of 23°C/W to 33°C/W depending on the copper area. So the junction temperature rise above ambient will be approximately equal to:

$$1.41W(28°C/W) = 39.5°C$$

The maximum junction temperature will then be equal to the maximum junction temperature rise above ambient plus the maximum ambient temperature or:

$$T_{JMAX} = 50°C + 39.5°C = 89.5°C$$

Protection Features

The LT1764A regulators incorporate several protection features which make them ideal for use in battery-powered circuits. In addition to the normal protection features associated with monolithic regulators, such as current limiting and thermal limiting, the devices are protected against reverse input voltages, reverse output voltages and reverse voltages from output to input.

Current limit protection and thermal overload protection are intended to protect the device against current overload conditions at the output of the device. For normal operation, the junction temperature should not exceed 125°C.

The input of the device will withstand reverse voltages of 20V. Current flow into the device will be limited to less than 1mA and no negative voltage will appear at the output. The device will protect both itself and the load. This provides protection against batteries which can be plugged in backward.

The output of the LT1764A-X can be pulled below ground without damaging the device. If the input is left open circuit or grounded, the output can be pulled below ground by 20V. For fixed voltage versions, the output will act like a large resistor, typically 5k or higher, limiting current flow to typically less than 600µA. For adjustable versions, the output will act like an open circuit; no current will flow out of the pin. If the input is powered by a voltage source, the output will source the short-circuit current of the device and will protect itself by thermal limiting. In this case, grounding the SHDN pin will turn off the device and stop the output from sourcing the short-circuit current.

The ADJ pin of the adjustable device can be pulled above or below ground by as much as 7V without damaging the device. If the input is left open circuit or grounded, the ADJ pin will act like an open circuit when pulled below ground and like a large resistor (typically 5k) in series with a diode when pulled above ground.

APPLICATIONS INFORMATION

In situations where the ADJ pin is connected to a resistor divider that would pull the ADJ pin above its 7V clamp voltage if the output is pulled high, the ADJ pin input current must be limited to less than 5mA. For example, a resistor divider is used to provide a regulated 1.5V output from the 1.21V reference when the output is forced to 20V. The top resistor of the resistor divider must be chosen to limit the current into the ADJ pin to less than 5mA when the ADJ pin is at 7V. The 13V difference between OUT and ADJ pins divided by the 5mA maximum current into the ADJ pin yields a minimum top resistor value of 2.6k.

In circuits where a backup battery is required, several different input/output conditions can occur. The output voltage may be held up while the input is either pulled to ground, pulled to some intermediate voltage, or is left open circuit. Current flow back into the output will follow the curve shown in Figure 5.

When the IN pin of the LT1764A-X is forced below the OUT pin or the OUT pin is pulled above the IN pin, input current will typically drop to less than 2μA. This can happen if the input of the device is connected to a discharged (low voltage) battery and the output is held up by either a backup battery or a second regulator circuit. The state of the SHDN pin will have no effect on the reverse output current when the output is pulled above the input.

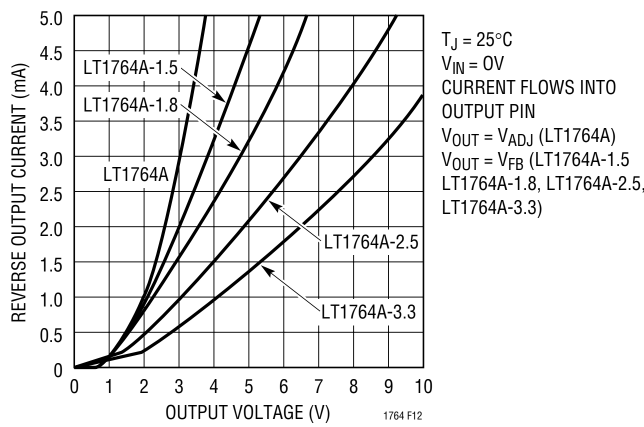
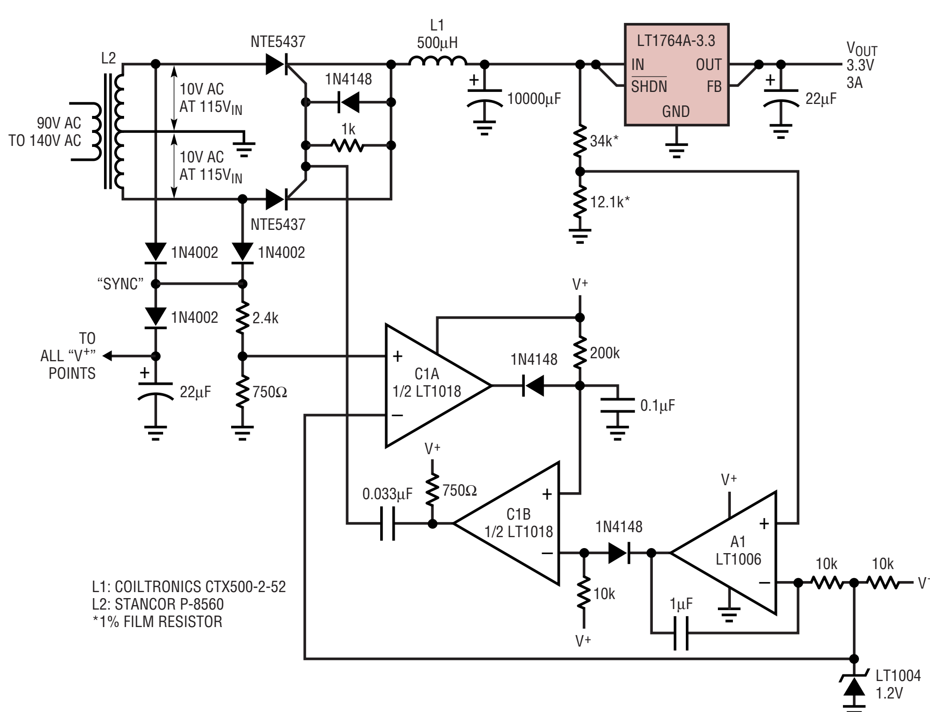


Figure 5. Reverse Output Current

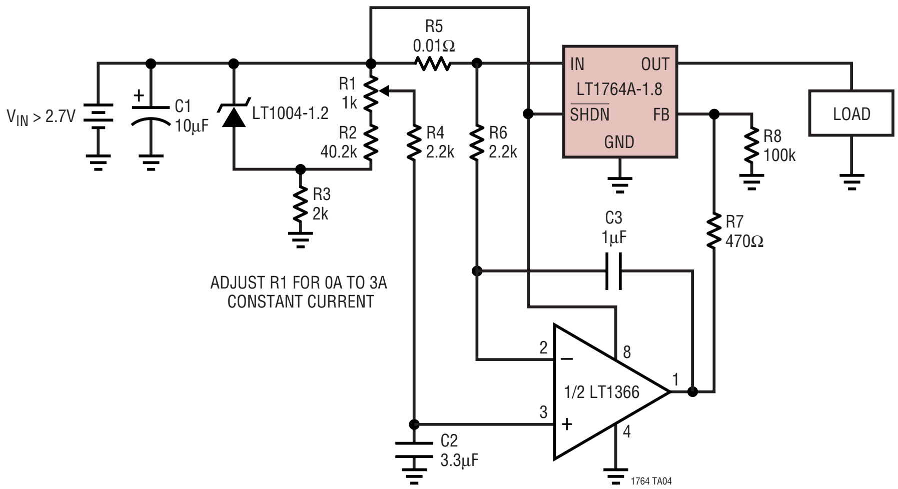
TYPICAL APPLICATIONS

SCR Preregulator Provides Efficiency Over Line Variations



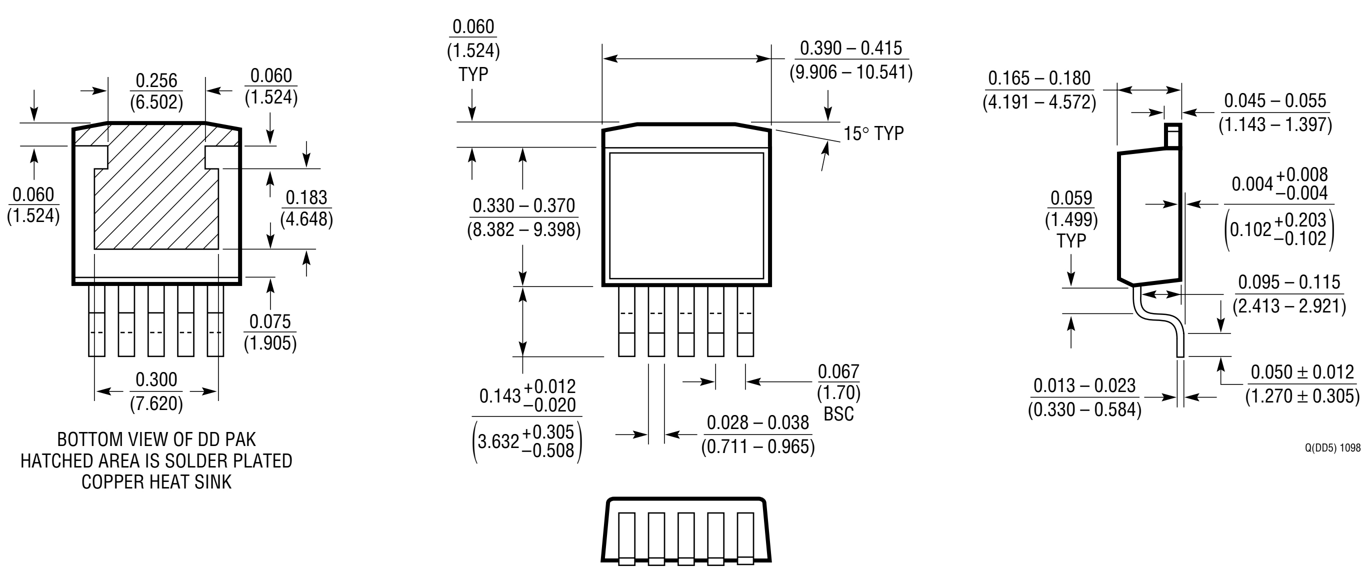
TYPICAL APPLICATIONS

Adjustable Current Source



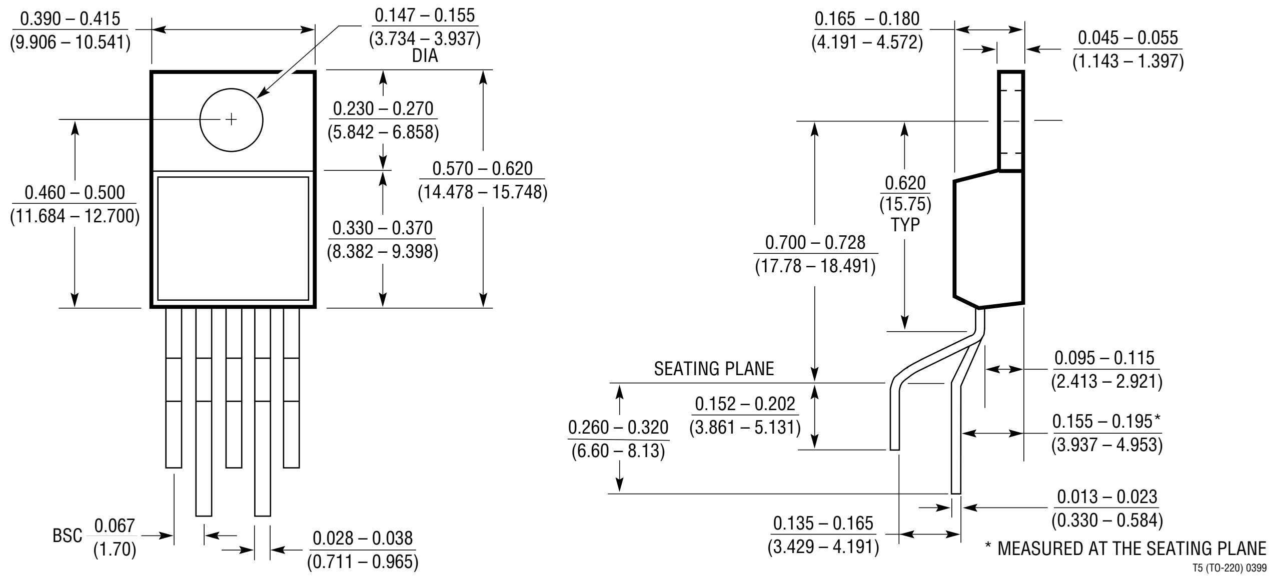
PACKAGE DESCRIPTION

Q Package
5-Lead Plastic DD Pak
(Reference LTC DWG # 05-08-1461)



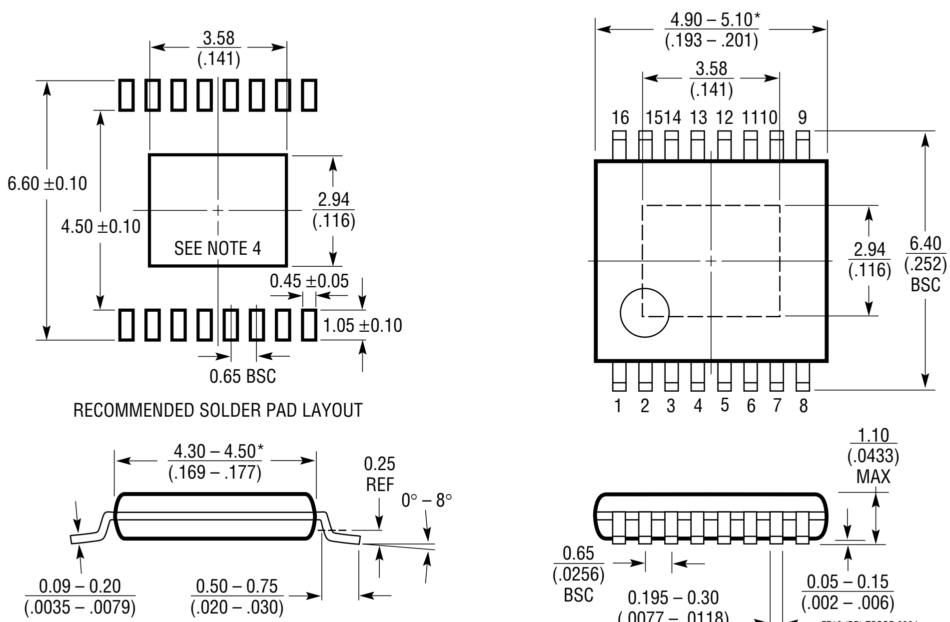
PACKAGE DESCRIPTION

T Package
5-Lead Plastic TO-220 (Standard)
(Reference LTC DWG # 05-08-1421)



FE Package
16-Lead Plastic TSSOP (4.4mm)
(Reference LTC DWG # 05-08-1663)

Exposed Pad Variation BB

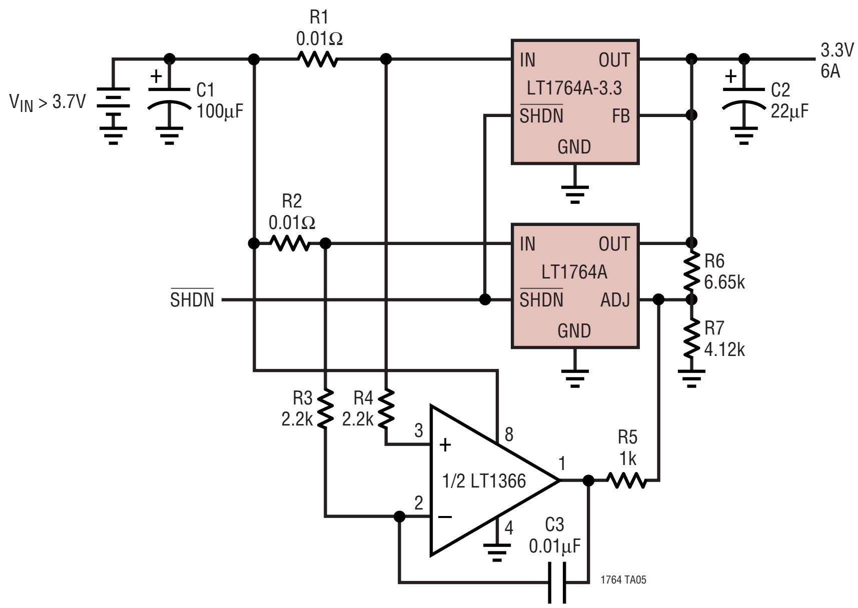


NOTE:
1. CONTROLLING DIMENSION: MILLIMETERS
2. DIMENSIONS ARE IN $\frac{\text{MILLIMETERS}}{\text{(INCHES)}}$
3. DRAWING NOT TO SCALE
4. RECOMMENDED MINIMUM PCB METAL SIZE FOR EXPOSED PAD ATTACHMENT

*DIMENSIONS DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.150mm (.006") PER SIDE

TYPICAL APPLICATION

Paralleling of Regulators for Higher Output Current



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT1120	125mA Low Dropout Regulator with 20µA I_Q	Includes 2.5V Reference and Comparator
LT1121	150mA Micropower Low Dropout Regulator	30µA I_Q, SOT-223 Package
LT1129	700mA Micropower Low Dropout Regulator	50µA Quiescent Current
LT1175	500mA Negative Low Dropout Micropower Regulator	45µA I_Q, 0.26V Dropout Voltage, SOT-223 Package
LT1374	4.5A, 500kHz Step-Down Converter	4.5A, 0.07Ω Internal Switch, SO-8 Package
LT1521	300mA Low Dropout Micropower Regulator with Shutdown	15µA I_Q, Reverse Battery Protection
LT1529	3A Low Dropout Regulator with 50µA I_Q	500mV Dropout Voltage
LT1573	UltraFast™ Transient Response Low Dropout Regulator	Drives External PNP
LT1575	UltraFast Transient Response Low Dropout Regulator	Drives External N-Channel MOSFET
LTC1735	Synchronous Step-Down Converter	High Efficiency, OPTI-LOOP® Compensation
LT1761 Series	100mA, Low Noise, Low Dropout Micropower Regulators in SOT-23	20µA Quiescent Current, 20µV_{RMS} Noise, ThinSOT™ Package
LT1762 Series	150mA, Low Noise, LDO Micropower Regulators	25µA Quiescent Current, 20µV_{RMS} Noise, MSOP Package
LT1763 Series	500mA, Low Noise, LDO Micropower Regulators	30µA Quiescent Current, 20µV_{RMS} Noise, SO-8 Package
LT1962	300mA, Low Noise, LDO Micropower Regulator	20µV_{RMS} Noise, MSOP Package
LT1963A	1.5A, Low Noise, Fast Transient Response LDO	40µV_{RMS} Noise, SOT-223 Package
LT1964	200mA, Low Noise, Negative LDO Micropower Regulator	30µV_{RMS} Noise, ThinSOT Package

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LT 0706 REV B • PRINTED IN USA