

ORDER NUMBER:**LPC47S422-MS FOR 100 PIN, QFP LEAD-FREE ROHS COMPLIANT PACKAGE**

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General Description

The LPC47S422 is a 3.3V PC99 compliant Super I/O controller. The LPC47S422 implements the LPC interface, a pin reduced ISA interface which provides the same or better performance as the ISA/X-bus with a substantial savings in pins used. The part provides 39 GPIO pins, an SMBus controller, a fan speed control output, a fan tachometer input, four ISA IRQs that can be routed to any of the serial IRQs, and an X-Bus interface.

The LPC47S422 incorporates a keyboard interface, SMSC's true CMOS 765B floppy disk controller, advanced digital data separator, two 16C550 compatible UARTs, one Multi-Mode parallel port which includes ChiProtect circuitry plus EPP and ECP, and Intelligent Power Management. The true CMOS 765B core provides 100% compatibility with IBM PC/XT and PC/AT architectures in addition to providing data overflow and underflow protection. The SMSC advanced digital data separator incorporates SMSC's patented data separator technology, allowing for ease of testing and use. The on-chip UARTs are compatible with the NS16C550. The parallel port is compatible with IBM PC/AT architecture, as well as IEEE 1284 EPP and ECP. The LPC47S422 incorporates sophisticated power control circuitry (PCC). The PCC supports multiple low power down modes.

The LPC47S422 supports the ISA Plug-and-Play Standard (Version 1.0a) and provides the recommended functionality to support Windows '95/'98 and PC99. The I/O Address, DMA Channel and Hardware IRQ of each logical device in the LPC47S422 may be reprogrammed through the internal configuration registers. There are 480 I/O address location options, a Serialized IRQ interface, and three DMA channels.

Block Diagram

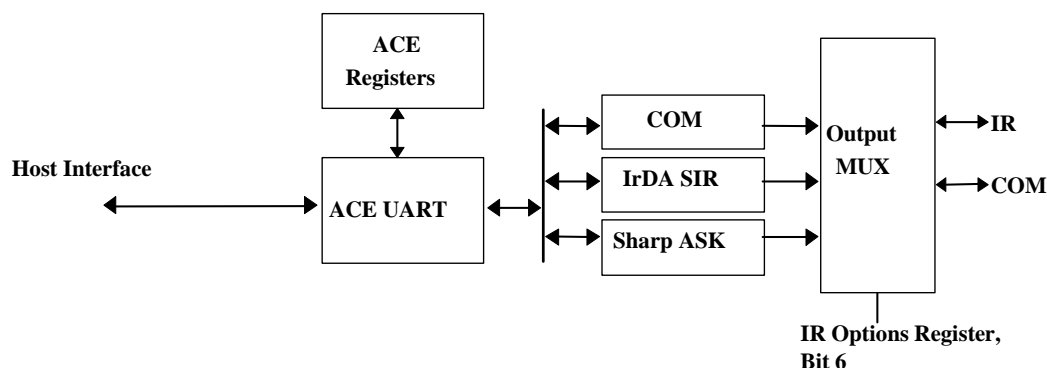


Figure 1 LPC47S422 Block Diagram

Package Outline

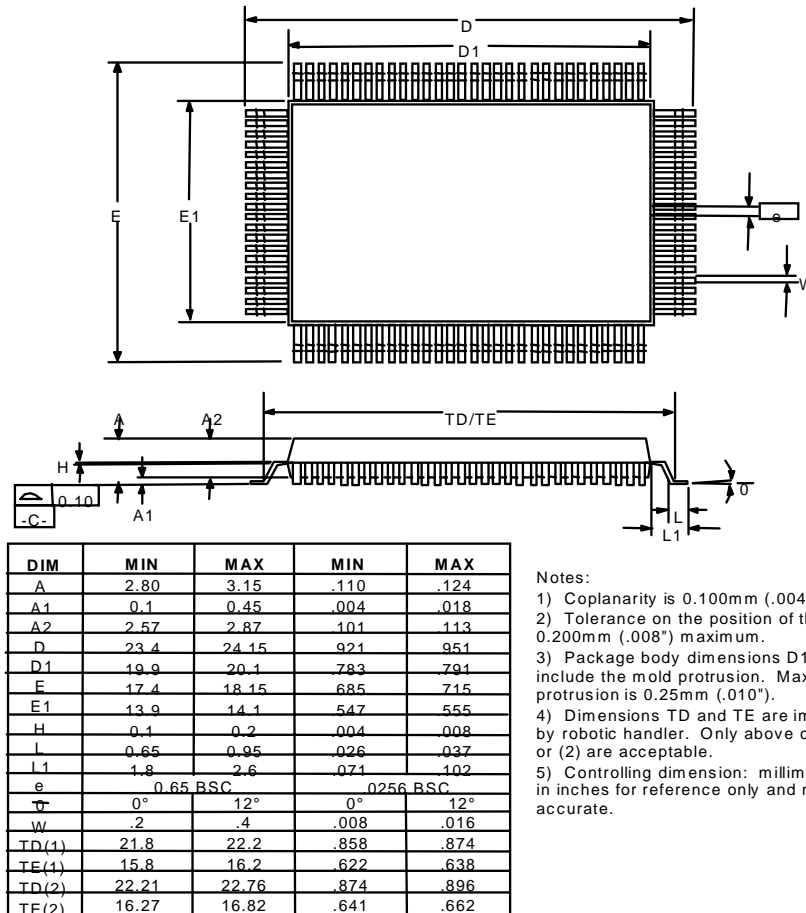


Figure 2 LPC47S422 100 Pin QFP Package Outline and Parameters