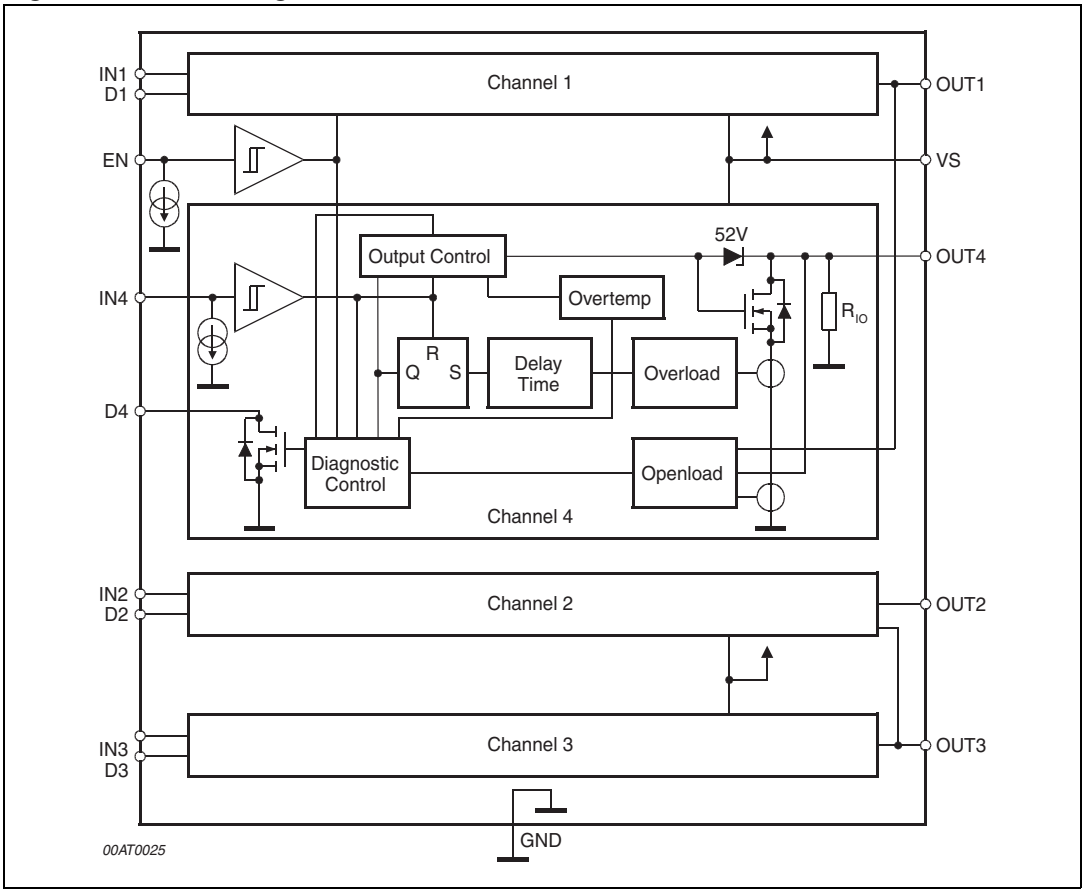
Contents

List of tables

List of figures

1 Block diagram

Figure 1. Block diagram



2 Pins description

Figure 2. Pins connection (top view)

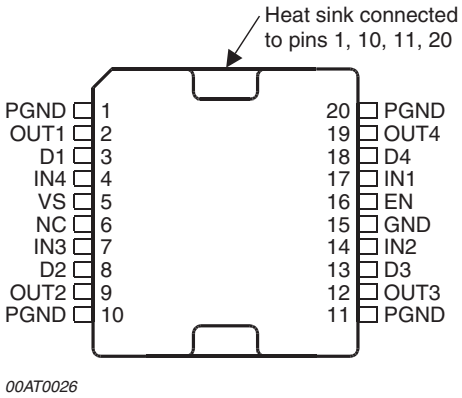


Table 2. Pins description

N°	Pin	Function
1	PGND	Power Ground
2	Out1	Output 1 (5A)
3	D1	Diagnostic 1
4	IN4	Input 4
5	VS	Supply Voltage
6	NC	Not Connected
7	IN3	Input 3
8	D2	Diagnostic 2
9	Out2	Output 2 (5A)
10	PGND	Power Ground
11	PGND	Power Ground
12	Out3	Output 3 (3A)
13	D3	Diagnostic 3
14	IN2	Input 2
15	GND	Signal Ground
16	EN	Common Enable
17	IN1	Input 1
18	D4	Diagnostic 4
19	Out4	Output 4 (3A)
20	PGND	Power Ground

3 Electrical specifications

3.1 Absolute maximum ratings

Table 3. Absolute maximum ratings

Symbol	Parameter	Conditions	Value	Unit
V_S	DC supply voltage		-0.3 to 32	V
V_{SP}	Supply voltage pulse (duration <200ms)		-0.3 to 45	V
$\|dV_S/dt\|$	Supply voltage slope		10	V/µs
$V_{IN, EN}$	Input voltage	$\|I\|$ 10mA	-1.5 to 6	V
V_D	Diagnostic DC output voltage	$\|I\|$ 50mA	-0.3 to 16	V
V_{ODC}	DC output voltage		-0.3 to 45	V
$I_{O1, 2}$	DC output current out 1, 2		>5 (Min.) internal limited (Max.)	A
$I_{O3, 4}$	DC output current out 3, 4		>3 (Min.) internal limited (Max.)	A
$I_{OR1, 2}$	Reverse output current		-5	A
$I_{OR3, 4}$	Reverse output current		-3	A
$E_{O1, 2}$	Switch-off energy for inductive loads	t_{EO} = 250µs,(1)	50	mJ
$E_{O3, 4}$		T = 5ms	30	mJ
ΔV_{GND}	GND potential difference	T_j = -40 to 150°C	±0.3	V
T_{jEO}	Junction temperature during switch-off	$\Sigma t \leq$ 30 min	175	°C
		$\Sigma t \leq$ 15 min	190	°C
T_j	Junction temperature		-40 to T_{jDIS}	°C
T_{stg}	Storage temperature		-55 to 150	°C
T_{jDIS}	Thermal disable junction temperature threshold		180 to 210	°C
ESD	Electrostatical discharging	MIL883C	+-2	kV
ESD	OUT1 - 4	vs. Common-GND (PGNDs + GND)	+-4	kV

1. t_{EO} is the clamping time (see *Figure 3*)

3.2 Thermal data

Table 4. Thermal data

Symbol	Parameter	Value	Unit
$R_{Th\ j\text{-}case}$	Thermal resistance junction to case	3	°C/W

3.3 Electrical characteristics (operating range)

The electrical characteristics are valid within the below defined operating range, unless otherwise specified.

Table 5. Electrical characteristics (operating range)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
V_S	Board supply voltage		4.5	12	32	V
T_{j1}	Junction temperature		-40		150	°C
T_{j2}		$\Sigma t \leq 15min$ (1) over life time	150		T_{jDIS}	°C

1. Parameters guaranteed by correlation

3.4 Electrical characteristics

Table 6. Electrical characteristics

(V_S = 4.5 to 32V; -40°C ≤ T_{j1} ≤ 150°C < T_{j2} ≤ T_{jDIS}, unless otherwise specified.)

Symbol	Parameter	Test conditions	Values T_{j1}			Values T_{j2}		Unit
			Min.	Typ.	Max.	Min.	Max.	
Supply								
$I_{VS\ OFF}$	DC supply current Off	EN = 1.0V		5	10			mA
$I_{VS\ ON}$	DC supply current On	$V_s \leq 14V$; V_{IN}, V_{EN} = 2V		8				mA
Diagnostic outputs D1 - D4								
V_{DL}	Diagnostic output low voltage	$I_D \leq 3mA$		0.65	1.0		1.5	V
I_{DLE}	Diagnostic output leakage current	V_D = 14V (1)		0.1	2		20	µA
Outputs Out 1 - Out 4								
$R_{DSON\ 1,\ 2}$	Output On resistance	T_j = 25°C T_j = 150°C V_S > 9.5V $I_{O1,2}$ = 2A		200	300 500			mΩ
$R_{DSON\ 3,\ 4}$		T_j = 25°C T_j = 150°C V_S > 9.5V $I_{O3,4}$ = 1.3A		300	450 750			mΩ
V_Z	Z-diode clamping voltage	$I_{OCL} \geq 200mA$	45		60			V
R_O	Output pull down resistor	VS > 9.5V EN = 0V	10		40		50	kΩ
$V_{OUV\ 1-4}$	Open load voltage threshold	V_{IN} = 1V	0.525 x V_S	0.55 x V_S	0.575 x V_S			V

Table 6. Electrical characteristics (continued)

(V_S = 4.5 to 32V; -40°C ≤ T_{j1} ≤ 150°C < T_{j2} ≤ T_{jDIS}, unless otherwise specified.)

Symbol	Parameter	Test conditions	Values T_{j1}			Values T_{j2}		Unit
			Min.	Typ.	Max.	Min.	Max.	
$V_{OUV\ hys\ 1-4}$	Hysteresis			0.003 x V_S				V
$\Delta V_{OUV\ 1-4,\ 2-3,\ 4-1,\ 3-2}$	Open load difference voltage threshold	$V_{IN1,4/2,3}$ = 1V $V_S \leq$ 16V $V_{Oc} \geq$ 4.5V V_{OC} = output voltage of other channel	V_{OC} - 1.0V	V_{OC} - 1.25V	V_{OC} - 1.5V			V
$\Delta V_{OUV\ hys\ 1-4,\ 2-3,\ 4-1,\ 3-2}$	Open load hysteresis			40				mV
$I_{OUC\ 1,\ 2,\ 3,\ 4}$	Open load current threshold	V_{EN}=V_{IN}=2V; V_S=6.5 - 16V	160	320	480			mA
$I_{OOC\ 1,\ 2}$	Over load current threshold	V_S > 6.5V; V_{OUT} = 32V	5	10				A
$I_{OOC\ 3,\ 4}$			3	6				A
T_{SD}	Thermal shut down		180	195	210			°C
T_{SD-hys}	Thermal shut down hysteresis			20				°C
I_{OUT-LE}	OUT leakage current	V_{OUT} = 20V V_S = 0V			5			µA
Inputs IN1-4, EN								
$V_{IN,EN\ L}$	Logic input/enable low voltage		-0.3		1			V
$V_{IN,EN\ H}$	Logic input/enable high voltage	IN, EN	2.0		6			V
$V_{EN,IN\ hys}$	Logic input hysteresis		50	100				mV
I_{IN}	Input sink current	2V < V_{IN}, V_{EN} < 6V (2) V_{IN}, V_{EN} < V_s	10	20	40			µA
I_{EN}	Enable sink current		10	20	40			µA
Timing								
t_{ON}	Output delay ON time	I_O = 1A V_S = 12V (3) *Figure 4*		4	25			µs
$t_{f,r}$	Output fall and rise time	I_O = 1A V_S = 12V *Figure 4*	3	10	30			µs
t_{OFF}	Output delay OFF time	I_O = 1A V_S = 12V (3) *Figure 4*	5	15	30			µs

Table 6. Electrical characteristics (continued)

(V_S = 4.5 to 32V; -40°C ≤ T_{j1} ≤ 150°C < T_{j2} ≤ T_{jDIS}, unless otherwise specified.)

Symbol	Parameter	Test conditions	Values T_{j1}			Values T_{j2}		Unit
			Min.	Typ.	Max.	Min.	Max.	
$t_{DH-L, Diag}$	Diag. delay output OFF time	(3) *Figure 4*	8		65		90	µs
$t_{D\ IOU}$	Diagnostic open load delay time	9V< V_S <16V, *Figure 5*		8	50			µs
t_{DOL}	Diagnostic overload delay switch-OFF time	9V< V_S <16V, *Figure 5*	6		65			µs
t_{filt}	Filter time		4		24			µs
PGND								
$PGND_{loss,h}$	Power GND loss threshold high			3				V
$PGND_{loss,l}$	Power GND loss threshold low			2				V

1. The diagnostic output is short circuit protected up to V_D = 16V
2. Open pins (EN, IN) are detected as low
3. V_S = 9 to 16V ∧ $I_{OUC} \leq I_O \leq I_{OOC}$

3.5 Diagnostic

Table 7. Diagnostic

Conditions		EN	IN	OUT	DIAG.
Normal function		L	X	off	L
		H	L	off	L
		H	H	on	H
GND short	V_{Otyp} < 0.55VS	L	X	off	H
Load bypass	$\Delta V_{O1-4/2-3} \geq$ 1.25V	H	L	off	H
Open load	$I_{O1,2,3,4typ}$ < 320mA	H	H	on	L
$T_{jtyp} \geq$ 190°C Overtemperature		X	X	off	L
Over load	$I_{Omin\ 1,2}$ > 5A $I_{Omin\ 3,4}$ > 3A	H	H	off	L
SGND or PGND loss	channel off	X	L	off	H
SGND or PGND loss	channel on	H	H	off	L

3.6 Circuit description

The L9349 is a quad low side driver for inductive loads like valves in automotive environment. The internal pull down current sources at the ENable and INput pins assure in case of open input conditions that the device is switched off. An output voltage slope limitation for du/dt is implemented to reduce the EMI. An integrated active flyback voltage limitation clamps the output voltage during the flyback phase to 50 V.

Each driver is protected against short circuit at V_{OUT} < 32V and thermal overload. In short circuit condition the output will be disabled after a short delay time t_{DOL}. The thermal disable for T_J > 180°C of the output will be reset if the junction temperature decreases about 20°C below the disable threshold temperature.

The overtemperature, overload and groundloss information is stored until IN is low.

For the real time error diagnosis the voltage and the current of the outputs are compared with internal fixed values V_{OUV} for OFF and I_{OUC} for ON conditions to recognize open load ($R_L \geq 20K\Omega$, $R_L > 38\Omega$) in OFF and ON conditions.

Also the output voltages V_{O1-4} are compared to each other output in OFF condition with a fixed offset of ΔV_{OUV} to recognize load bypasses. The ΔV_{OUV} diagnoses is suppressed during the flyback phases of the compared output. The outputs 1 and 4 are compared for ΔV_{OUV} and also outputs 2 and 3 are compared.

The diagnostic output level in connection with different ENable and INput conditions allows to recognize different fail states, like overtemp, short to V_S, short to GND, bypass to GND and disconnected load (see *Table 7: Diagnostic*).

The diagnostic output is protected against short circuit. Exceeding the over load current threshold I_{OOC}, the output current will be limited internally during the diagnostic overload delay switch-off time t_{DOL}.

The device complies the I_{SO} pulses imposed to the supply voltage of the valves without any failures of the functionality. Therefore some diagnostic functions are internal filtered. The following table shows the corresponding filter time for each detected signal.

Table 8. Corresponding filter time for each detected signal

	ON State EN and IN = HIGH	OFF State EN or IN, = LOW	min. Filter time	Reset done by
Overloading of output (also shorted load to supply)	X		4µs	INx = “LOW”
Open load (under voltage detection)		X	-	
Open load (under current detection)	X		-	
Overtemperature	X		4µs	INx = “LOW”
Power-signal GND-loss	X		4µs	INx = “LOW”
Power-signal GND-loss		X	4µs	
Openload difference		X	4µs	

Figure 3. t_{EO} clamping time

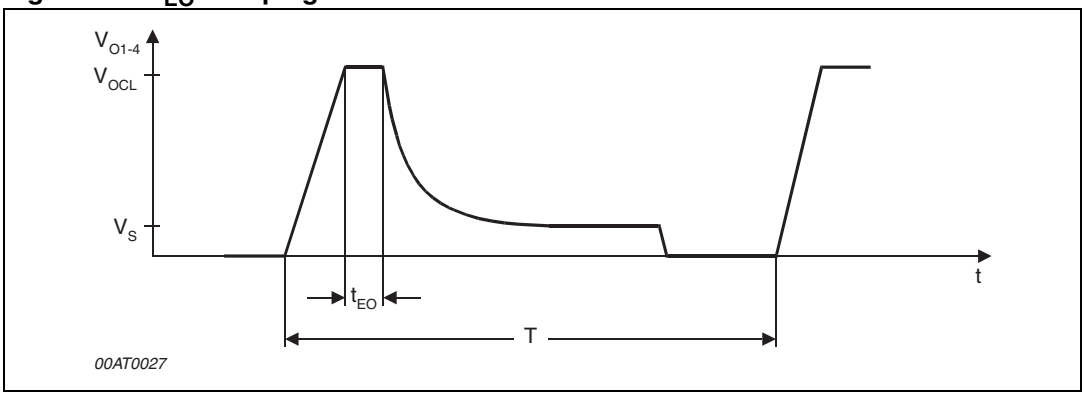


Figure 4. Output slope (resistive load for testing)

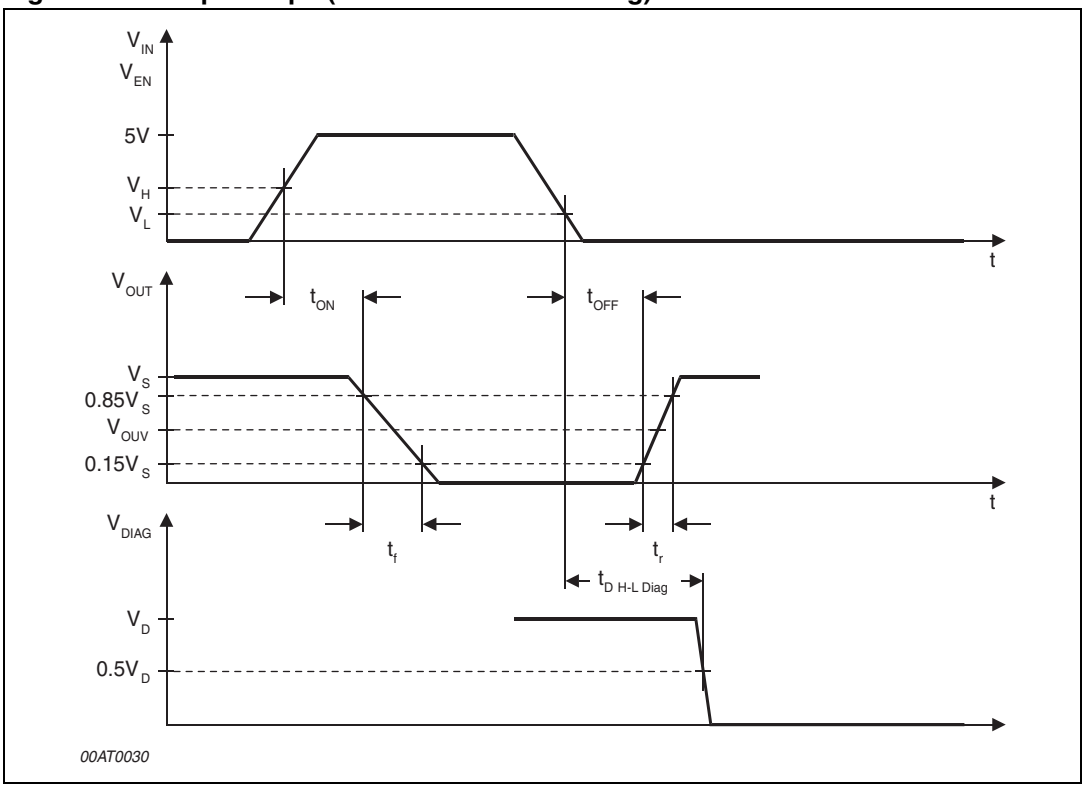


Figure 5. Timing (t_{DOL}, t_{DIOU})

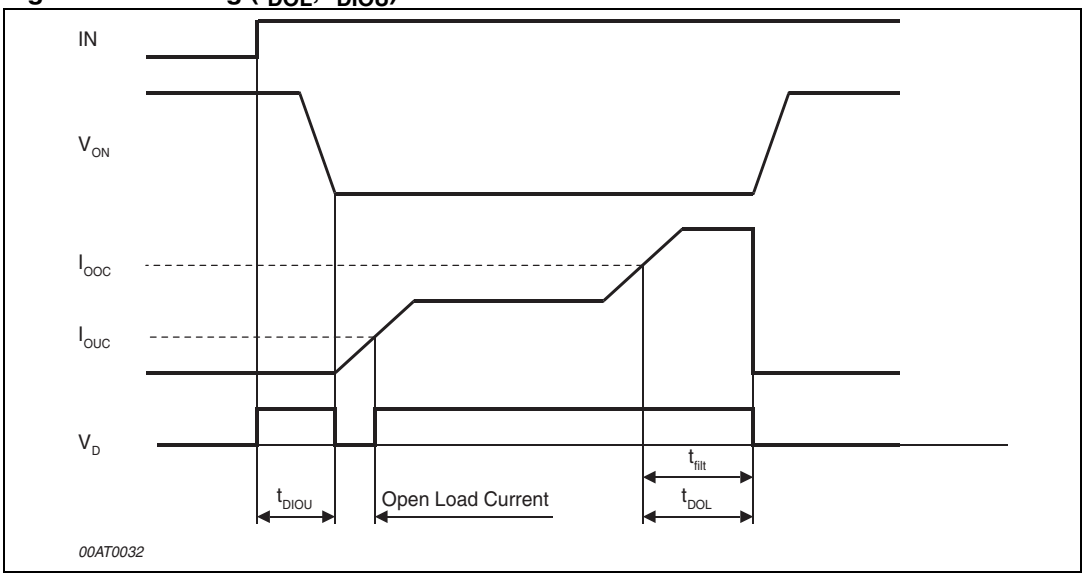


Figure 6. Block diagram - Open load voltage detection

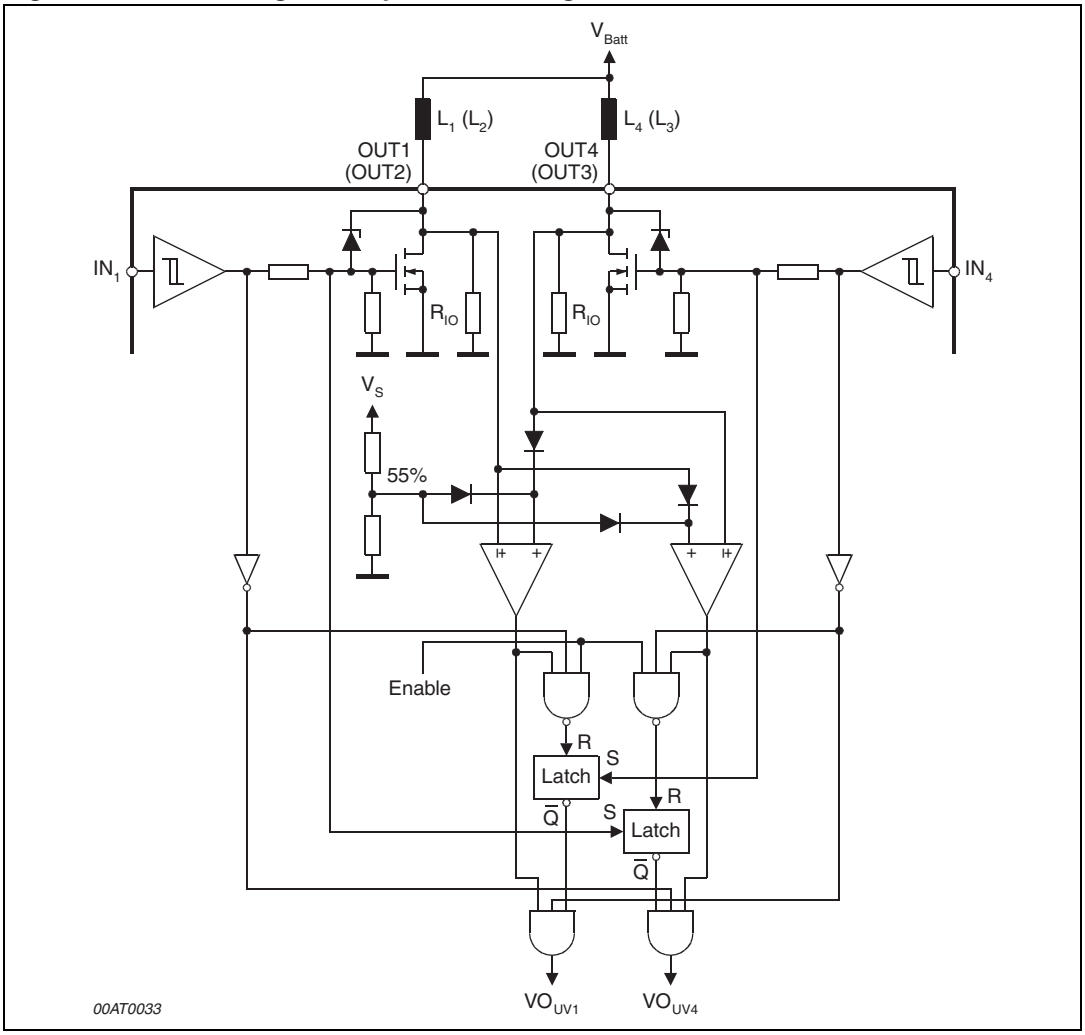


Figure 7. Logic diagram

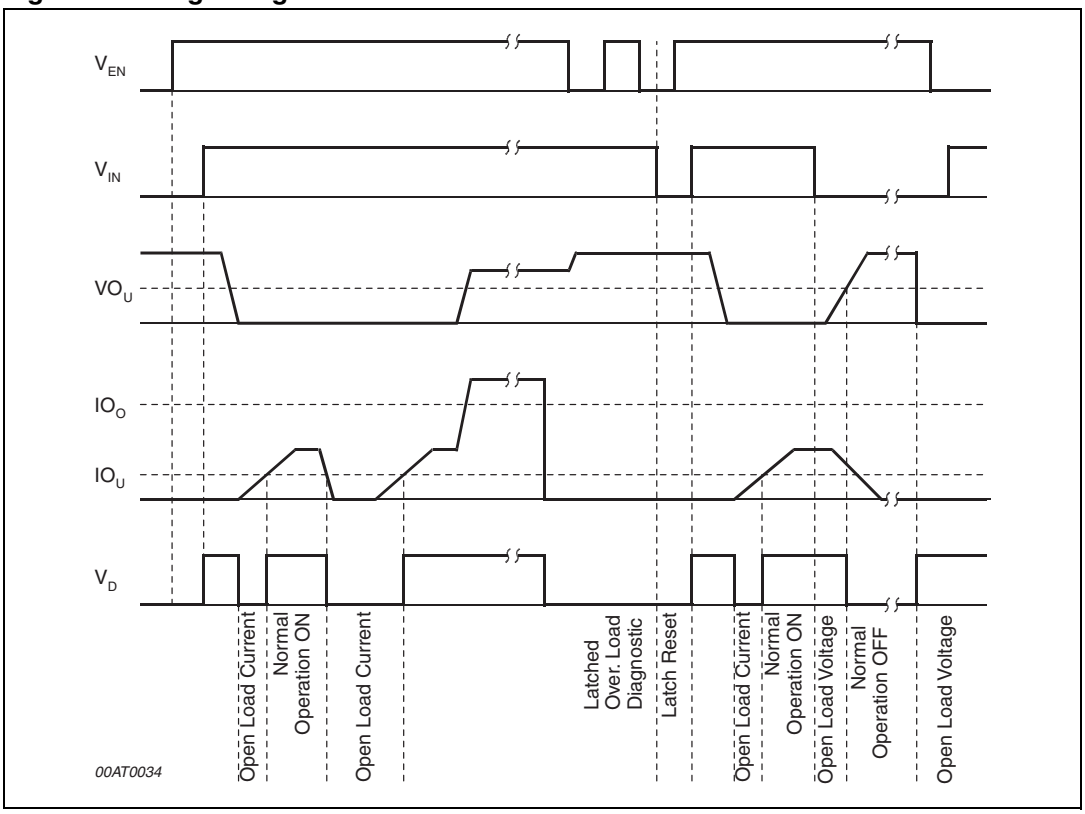
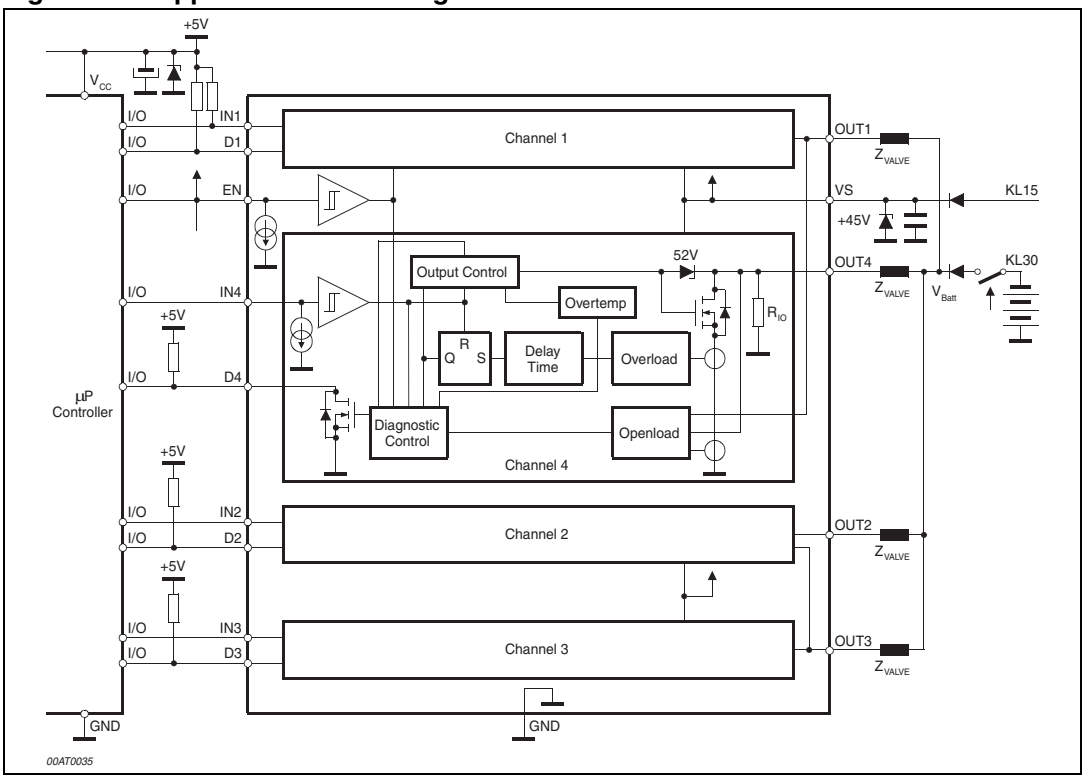


Figure 8. Application circuit diagram



4 Package information

In order to meet environmental requirements, ST (also) offers these devices in ECOPACK® packages. ECOPACK® packages are lead-free. The category of second Level Interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label.

ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com.

Figure 9. PowerSO-20 mechanical data and package dimensions

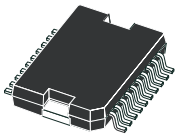
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			3.6			0.142
a1	0.1		0.3	0.004		0.012
a2			3.3			0.130
a3	0		0.1	0.000		0.004
b	0.4		0.53	0.016		0.021
c	0.23		0.32	0.009		0.013
D (1)	15.8		16	0.622		0.630
D1 (2)	9.4		9.8	0.370		0.386
E	13.9		14.5	0.547		0.570
e		1.27			0.050	
e3		11.43			0.450	
E1 (1)	10.9		11.1	0.429		0.437
E2			2.9			0.114
E3	5.8		6.2	0.228		0.244
G	0		0.1	0.000		0.004
H	15.5		15.9	0.610		0.626
h			1.1			0.043
L	0.8		1.1	0.031		0.043
N	8˚(typ.)					
S	8˚(max.)					
T		10			0.394	

(1) "D and E1" do not include mold flash or protusions.
- Mold flash or protusions shall not exceed 0.15mm (0.006")
- Critical dimensions: "E", "G" and "a3".

(2) For subcontractors, the limit is the one quoted in jedec MO-166

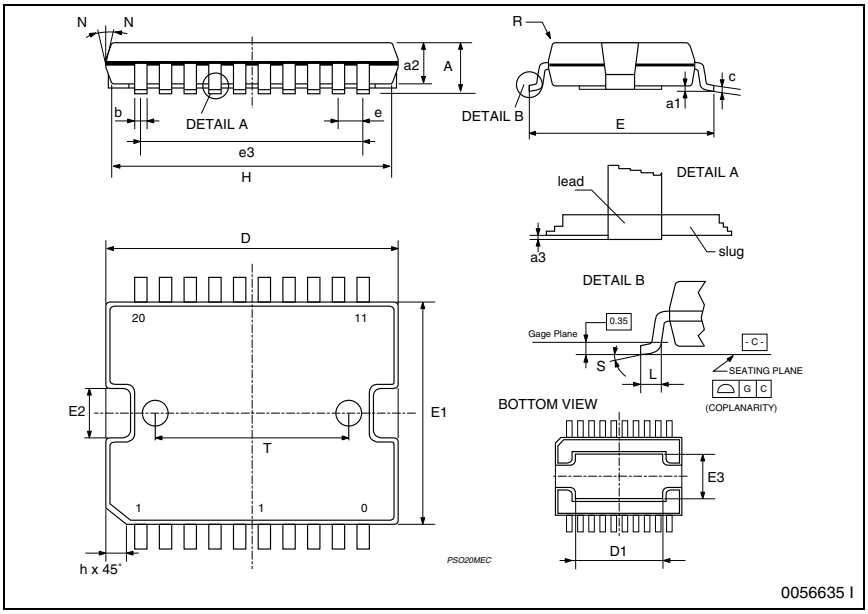
OUTLINE AND MECHANICAL DATA

Weight: 1.9gr



JEDEC MO-166

PowerSO-20



5 Revision history

Table 9. Document revision history

Date	Revision	Changes
20-Sep-2002	4	Initial release.
09-Sep-2008	5	Document reformatted. Updated feature and description on page 1. Added *Table 1: Device summary on page 1*. Updated *Table 3: Absolute maximum ratings on page 7*.
20-Sep-2013	6	Updated disclaimer.

Please Read Carefully:

Information in this document is provided solely in connection with ST products. STMicroelectronics NV and its subsidiaries (“ST”) reserve the right to make changes, corrections, modifications or improvements, to this document, and the products and services described herein at any time, without notice.

All ST products are sold pursuant to ST’s terms and conditions of sale.

Purchasers are solely responsible for the choice, selection and use of the ST products and services described herein, and ST assumes no liability whatsoever relating to the choice, selection or use of the ST products and services described herein.

No license, express or implied, by estoppel or otherwise, to any intellectual property rights is granted under this document. If any part of this document refers to any third party products or services it shall not be deemed a license grant by ST for the use of such third party products or services, or any intellectual property contained therein or considered as a warranty covering the use in any manner whatsoever of such third party products or services or any intellectual property contained therein.

UNLESS OTHERWISE SET FORTH IN ST’S TERMS AND CONDITIONS OF SALE ST DISCLAIMS ANY EXPRESS OR IMPLIED WARRANTY WITH RESPECT TO THE USE AND/OR SALE OF ST PRODUCTS INCLUDING WITHOUT LIMITATION IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE (AND THEIR EQUIVALENTS UNDER THE LAWS OF ANY JURISDICTION), OR INFRINGEMENT OF ANY PATENT, COPYRIGHT OR OTHER INTELLECTUAL PROPERTY RIGHT.

ST PRODUCTS ARE NOT DESIGNED OR AUTHORIZED FOR USE IN: (A) SAFETY CRITICAL APPLICATIONS SUCH AS LIFE SUPPORTING, ACTIVE IMPLANTED DEVICES OR SYSTEMS WITH PRODUCT FUNCTIONAL SAFETY REQUIREMENTS; (B) AERONAUTIC APPLICATIONS; (C) AUTOMOTIVE APPLICATIONS OR ENVIRONMENTS, AND/OR (D) AEROSPACE APPLICATIONS OR ENVIRONMENTS. WHERE ST PRODUCTS ARE NOT DESIGNED FOR SUCH USE, THE PURCHASER SHALL USE PRODUCTS AT PURCHASER’S SOLE RISK, EVEN IF ST HAS BEEN INFORMED IN WRITING OF SUCH USAGE, UNLESS A PRODUCT IS EXPRESSLY DESIGNATED BY ST AS BEING INTENDED FOR “AUTOMOTIVE, AUTOMOTIVE SAFETY OR MEDICAL” INDUSTRY DOMAINS ACCORDING TO ST PRODUCT DESIGN SPECIFICATIONS. PRODUCTS FORMALLY ESCC, QML OR JAN QUALIFIED ARE DEEMED SUITABLE FOR USE IN AEROSPACE BY THE CORRESPONDING GOVERNMENTAL AGENCY.

Resale of ST products with provisions different from the statements and/or technical features set forth in this document shall immediately void any warranty granted by ST for the ST product or service described herein and shall not create or extend in any manner whatsoever, any liability of ST.

ST and the ST logo are trademarks or registered trademarks of ST in various countries.
Information in this document supersedes and replaces all information previously supplied.
The ST logo is a registered trademark of STMicroelectronics. All other names are the property of their respective owners.

STMicroelectronics group of companies

Australia - Belgium - Brazil - Canada - China - Czech Republic - Finland - France - Germany - Hong Kong - India - Israel - Italy - Japan - Malaysia - Malta - Morocco - Philippines - Singapore - Spain - Sweden - Switzerland - United Kingdom - United States of America

www.st.com