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REVISION HISTORY

9/2017—Rev. A to Rev. B

Changed CP-24-2 to CP-24-16 ..... Throughout
Changes to Table 3 5
Updated Outline Dimensions 15
Changes to Ordering Guide 15

3/2017—Rev. 00.0912 to Rev. A

This Hittite Microwave Products data sheet has been reformatted to meet the styles and standards of Analog Devices, Inc.

Changes to Title, Features Section, Applications Section, and General Description Section 1
Changes to Table 1 3
Added Table 2; Renumbered Sequentially 4
Changes to Table 3 5
Added Figure 2 and Thermal Resistance Section; Renumbered Sequentially 5
Deleted Bias Voltage Table and Control Voltage Table; Renumbered Sequentially 5
Added Figure 3 6
Changes to Table 5 6
Added Insertion Loss, Return Loss, State Error, and Relative Phase Section 7
Changes to Figure 9, Figure 10, Figure 12, and Figure 13 7
Deleted Application Circuit Figure 8
Added Figure 14, Figure 15, and Figure 17 8
Changes to Figure 16 8
Added Figure 20 and Figure 23 9
Changes to Figure 21 and Figure 22 9
Added Figure 26 and Figure 29 10
Added Theory of Operation Section, Serial or Parallel Mode Selection Section, Table 8, and Figure 30 11
Changes to Table 6, Power Supply Section, Power-Up Interface Section, Table 7, Serial Mode Interface Section 11
Added RF Input and Output Section and AGCx Pins Section 12
Changes to Figure 31, Parallel Mode Interface Section, Direct Parallel Mode Section, Latched Parallel Mode Section, and Figure 32 12
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Added Figure 34 14
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SPECIFICATIONS

V_{DD} = 3 V to 5 V, control input voltage (V_{CTL}) = 0 V or V_{DD}, T_{CASE} = 25°C, 50 Ω system, unless otherwise noted.

Table 1.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
FREQUENCY RANGE			0.1		6.0	GHz
INSERTION LOSS		0.1 GHz to 3 GHz		1.6	2.4	dB
		3 GHz to 6.0 GHz		2.3	3.8	dB
ATTENUATION		0.1 GHz to 6.0 GHz				
Range		Between minimum and maximum attenuation states		31.5		dB
Step Size		Between any successive attenuation states		0.5		dB
Step Error		Between any successive attenuation states		<±0.2		dB
State Error		All attenuation states, referenced to insertion loss state				
		0.1 GHz to 0.8 GHz	−(0.1 + 5% of attenuation state)		+(0.1 + 5% of attenuation state)	dB
		0.8 GHz to 6.0 GHz	−(0.3 + 3% of attenuation state)		+(0.3 + 3% of attenuation state)	dB
RETURN LOSS (ATTIN and ATTOUT)		All attenuation states, 0.1 GHz to 6.0 GHz		15		dB
RELATIVE PHASE		Between minimum and maximum attenuation states				
		100 MHz to 3 GHz		25		Degrees
		3 GHz to 6.0 GHz		50		Degrees
SWITCHING CHARACTERISTICS		Between all attenuation states				
Rise and Fall Time	t_{RISE}, t_{FALL}	10% to 90% of RF output		60		ns
On and Off Time	t_{ON}, t_{OFF}	50% V_{CTL} to 90% of RF output		90		ns
INPUT LINEARITY[1]		All attenuation states, 250 MHz to 6.0 GHz				
0.1 dB Compression	P0.1dB	V_{DD} = 3 V		33		dBm
		V_{DD} = 5 V		27		dBm
Third-Order Intercept	IP3	V_{DD} = 3 V to 5 V, 10 dBm per tone, 1 MHz spacing		55		dBm
SUPPLY CURRENT	I_{DD}	V_{DD} = 3 V to 5 V		3		mA
DIGITAL CONTROL INPUTS		P/S, CLK, SERIN, LE, D0 to D5, PUP1, and PUP2 pins				
Voltage						
Low	V_{INL}	V_{DD} = 3 V	0		0.5	V
		V_{DD} = 5 V	0		0.8	V
High	V_{INH}	V_{DD} = 3 V	2		3	V
		V_{DD} = 5 V	2		5	V
Current		V_{DD} = 3 V to 5 V				
Low	I_{INL}			15		µA
High	I_{INH}			65		µA
DIGITAL CONTROL OUTPUT		SEROUT				
Voltage						
Low	V_{OUTL}			0		V
High	V_{OUTH}			V_{DD}		V
Current						
Low	I_{OUTL}				1	mA
High	I_{OUTH}				1	mA

[1] Input linearity performance degrades at frequencies less than 250 MHz; see Figure 18 to Figure 29.

TIMING SPECIFICATIONS

See Figure 31 and Figure 32 for the timing diagrams.

Table 2.

Parameter	Description	Min	Typ	Max	Unit
t_{SCK}	Minimum serial period	70			ns
t_{CS}	Control setup time	15			ns
t_{CH}	Control hold time		20		ns
t_{LN}	LE setup time	15			ns
t_{LEW}	Minimum LE pulse width		10		ns
t_{LES}	Minimum LE pulse spacing		630		ns
t_{CKN}	Serial clock hold time from LE		0		ns
t_{PH}	Data hold time from LE		10		ns
t_{PS}	Data setup time to LE		2		ns

ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Rating
Supply Voltage	5.6 V
Digital Control Input Voltage	−1 V to V_{DD} + 1 V
RF Input Power[1] (All Attenuation States, f = 250 MHz to 6.0 GHz, T_{CASE} = 85°C)	0.56 W
V_{DD} = 3 V	25 dBm
V_{DD} = 5 V	28 dBm
Continuous Power Dissipation, P_{DISS} (T_{CASE} = 85°C)	0.56 W
Temperature	
Junction, T_J	150°C
Storage	−65°C to +150°C
Reflow[2] ((Moisture Sensitivity Level 1 (MSL1) Rating)	260°C
ESD Sensitivity	
Human Body Model (HBM)	250 V (Class 1A)

[1] For power derating at frequencies less than 250 MHz, see Figure 2.
[2] See the Ordering Guide for more information.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

Only one absolute maximum rating can be applied at any one time.

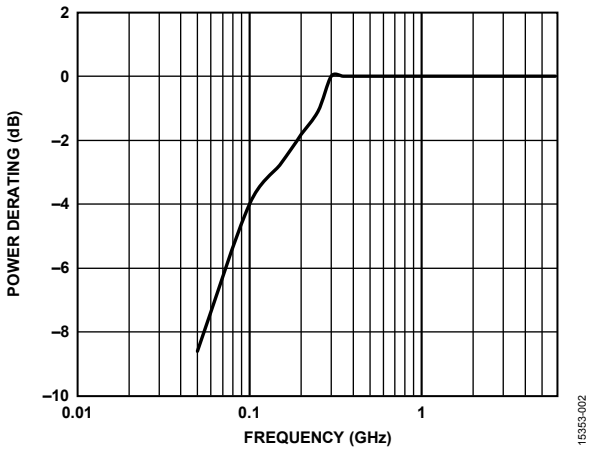


Figure 2. Power Derating at Frequencies Less Than 250 MHz

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

θ_{JC} is the junction to case thermal resistance.

Table 4. Thermal Resistance

Package Type	θ_{JC}	Unit
CP-24-16[1]	116	°C/W

[1] Thermal impedance simulated values are based on a JEDEC 2S2P thermal test board with nine thermal vias. See JEDEC JESD51.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

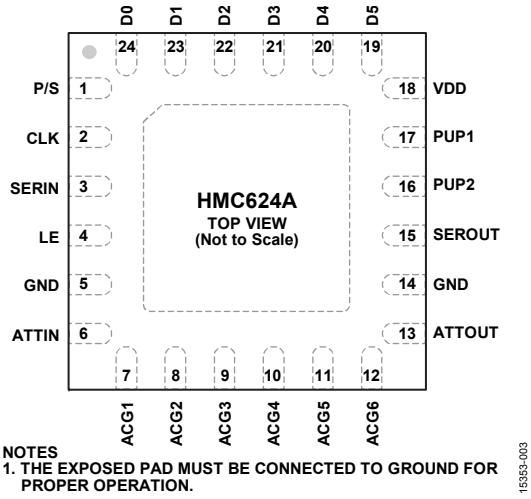


Figure 3. Pin Configuration

Table 5. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	P/S	Parallel/Serial Mode Select. For parallel mode operation, set this pin to low. For serial mode operation, set this pin to high.
2	CLK	Serial Interface Clock Input.
3	SERIN	Serial Interface Data Input.
4	LE	Latch Enable Input.
5, 14	GND	Ground. These pins must be connected to ground.
6	ATTIN	Attenuator RF Input. This pin can also be used as an output because the design is bidirectional. ATTIN is dc-coupled and ac matched to 50 Ω. An external dc blocking capacitor is required.
7 to 12	ACG1 to ACG6	AC Grounding Capacitor Pins. These pins can be left unconnected when operating above 700 MHz. For frequencies less than 700 MHz, connect capacitors larger than 100 pF as close to the ACGx pins as possible. Select the capacitor value for the lowest frequency of operation.
13	ATTOUT	Attenuator RF Output. This pin can also be used as an input because the design is bidirectional. ATTOUT is dc-coupled and ac matched to 50 Ω. An external dc blocking capacitor is required.
15	SEROUT	Serial Interface Data Output. Serial input data is delayed by six clock cycles.
16, 17	PUP2, PUP1	Power-Up State Selection Pins. These pins set the attenuation value at power-up (see Table 7).
18	VDD	Power Supply.
19 to 24	D5 to D0	Parallel Control Voltage Inputs. These pins select the required attenuation (see Table 6). There is no internal pull-up or pull-down resistor on these pins; therefore, they must always be kept at a valid logic level (V_{IH} or V_{IL}) and not be left floating.
	EPAD	Exposed Pad. The exposed pad must be connected to ground for proper operation.

INTERFACE SCHEMATICS

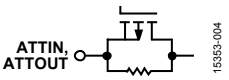


Figure 4. ATTIN, ATTOUT Interface Schematic

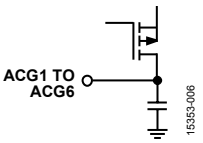


Figure 6. ACGx Pin Interface Schematic

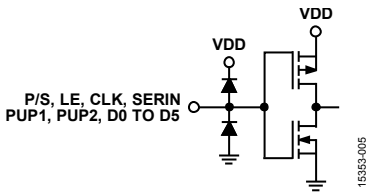


Figure 5. Digital Control Input Interface

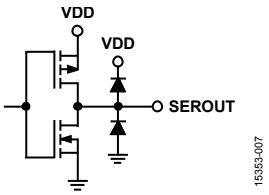


Figure 7. SEROUT Pin Interface

TYPICAL PERFORMANCE CHARACTERISTICS

INSERTION LOSS, RETURN LOSS, STATE ERROR, STEP ERROR, AND RELATIVE PHASE

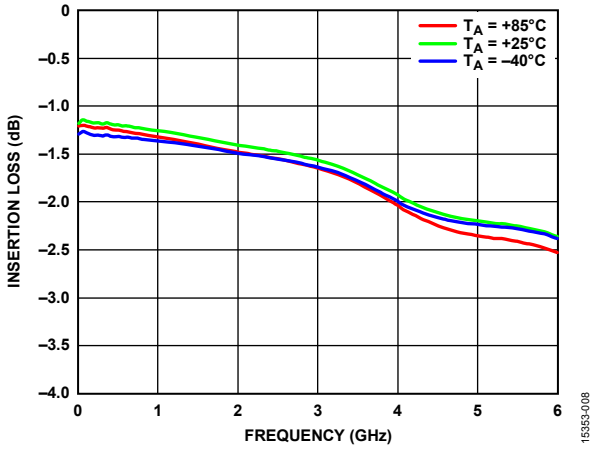


Figure 8. Insertion Loss vs. Frequency over Temperature

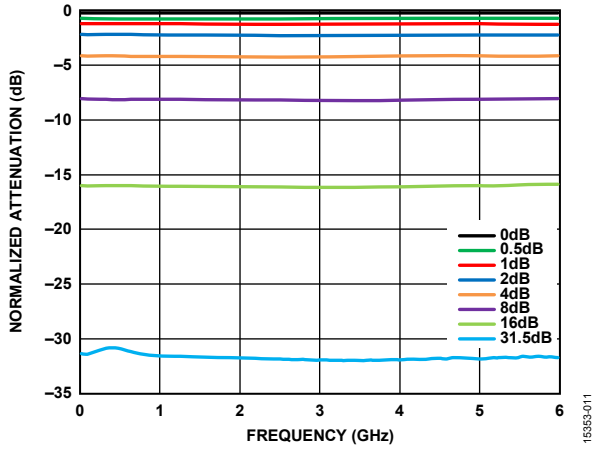


Figure 11. Normalized Attenuation vs. Frequency over Major Attenuation States

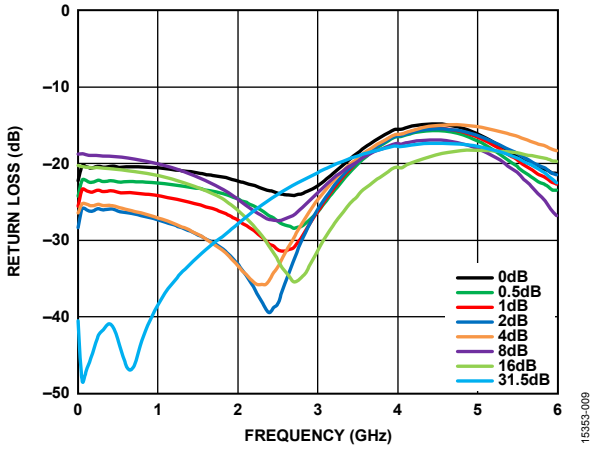


Figure 9. Input Return Loss vs. Frequency over Major Attenuation States

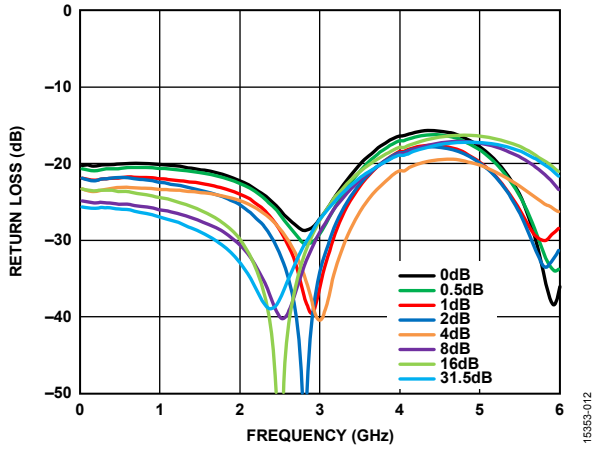


Figure 12. Output Return Loss vs. Frequency over Major Attenuation States

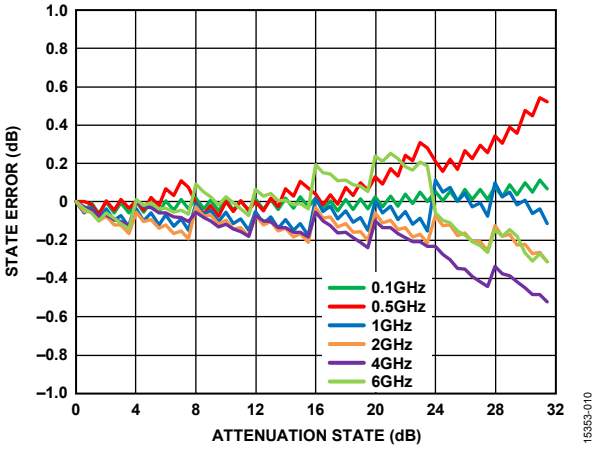


Figure 10. State Error vs. Attenuation State over Frequency

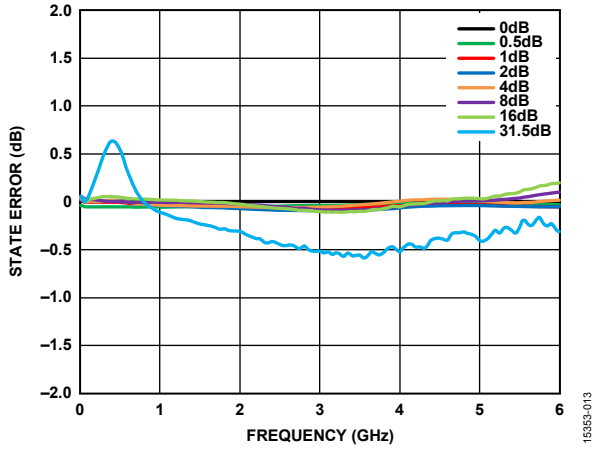


Figure 13. State Error vs. Frequency over Major Attenuation States

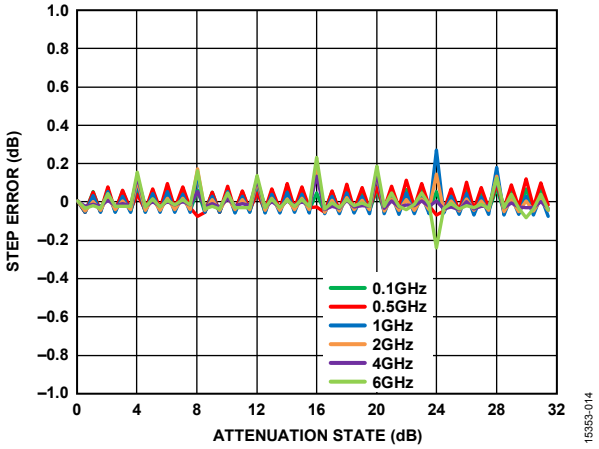


Figure 14. Step Error vs. Attenuation State over Frequency

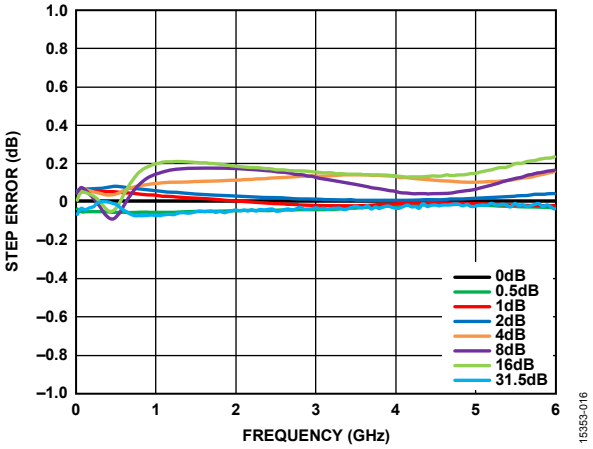


Figure 16. Step Error vs. Frequency over Major Attenuation States

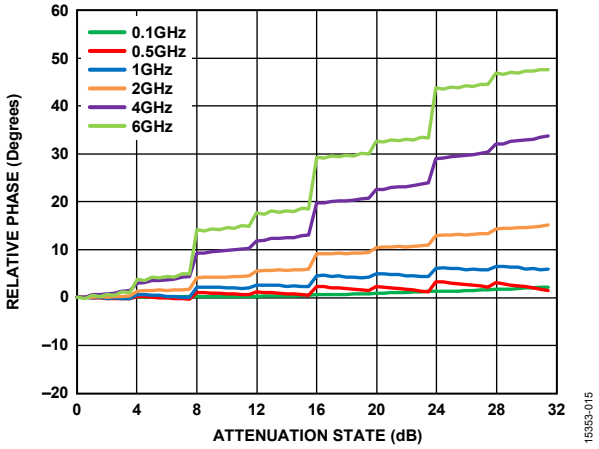


Figure 15. Relative Phase vs. Attenuation State over Frequency

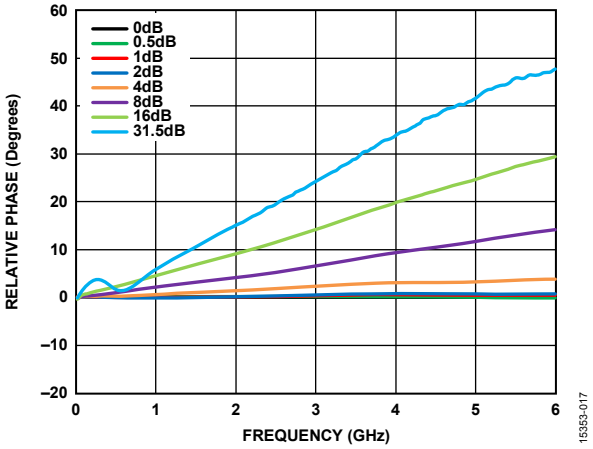


Figure 17. Relative Phase vs. Frequency over Major Attenuation States

INPUT POWER COMPRESSION AND THIRD-ORDER INTERCEPT

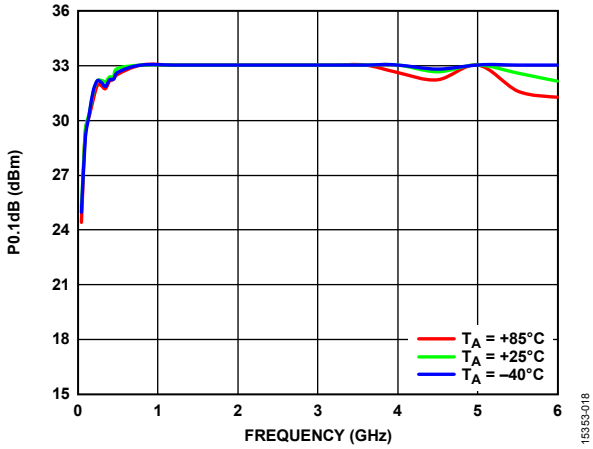


Figure 18. Input P0.1dB vs. Frequency at Minimum Attenuation State over Temperature, V_{DD} = 5 V

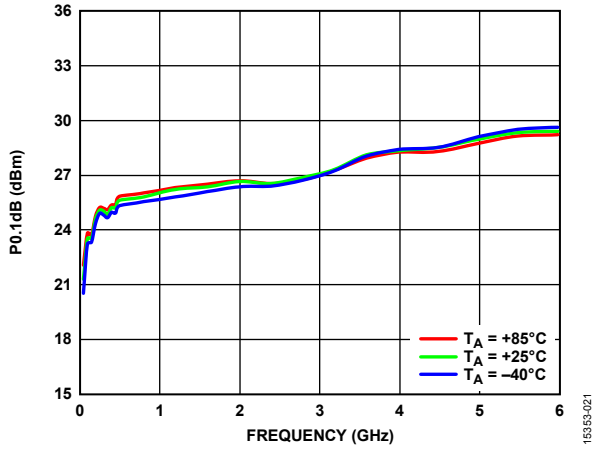


Figure 21. Input P0.1dB vs. Frequency at Minimum Attenuation State over Temperature, V_{DD} = 3 V

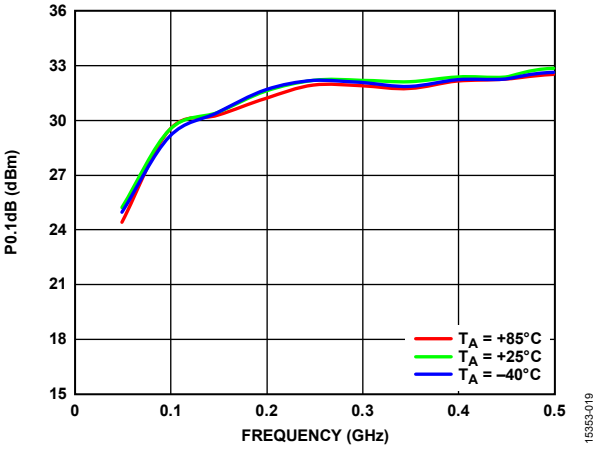


Figure 19. Input P0.1dB vs. Frequency at Minimum Attenuation State over Temperature, V_{DD} = 5 V (Low Frequency Detail)

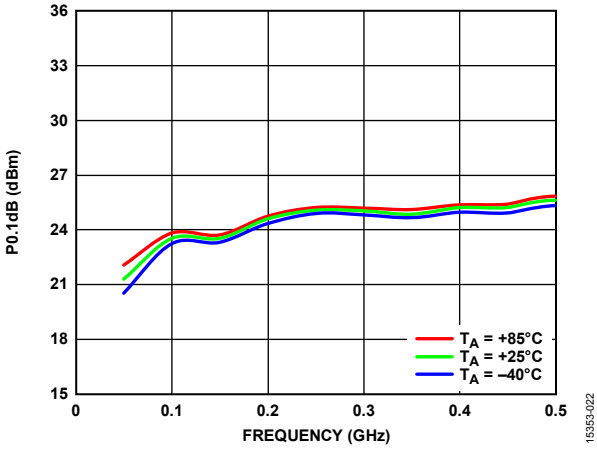


Figure 22. Input P0.1dB vs. Frequency at Minimum Attenuation State over Temperature, V_{DD} = 3 V (Low Frequency Detail)

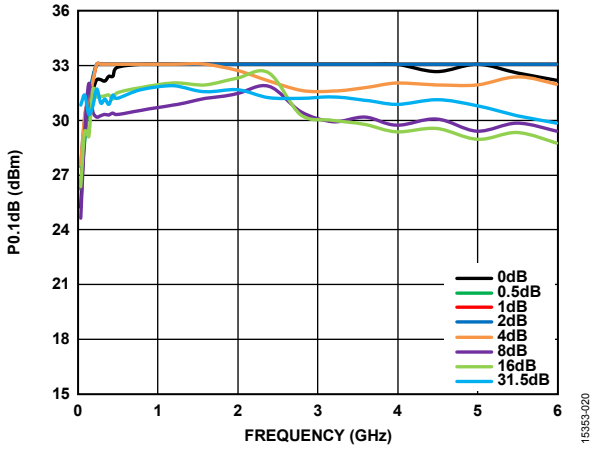


Figure 20. Input P0.1dB vs. Frequency over Major Attenuation States, V_{DD} = 5 V

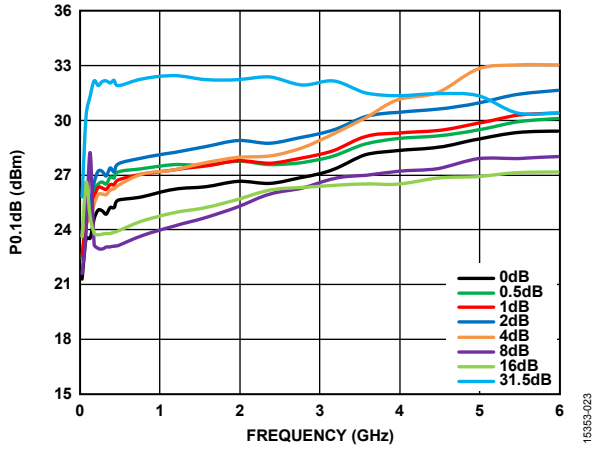


Figure 23. Input P0.1dB vs. Frequency over Major Attenuation States, V_{DD} = 3 V

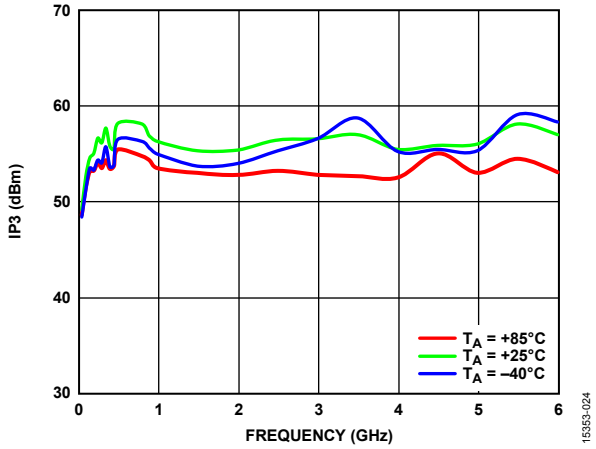


Figure 24. Input IP3 vs. Frequency at Minimum Attenuation State over Temperature, V_{DD} = 5 V

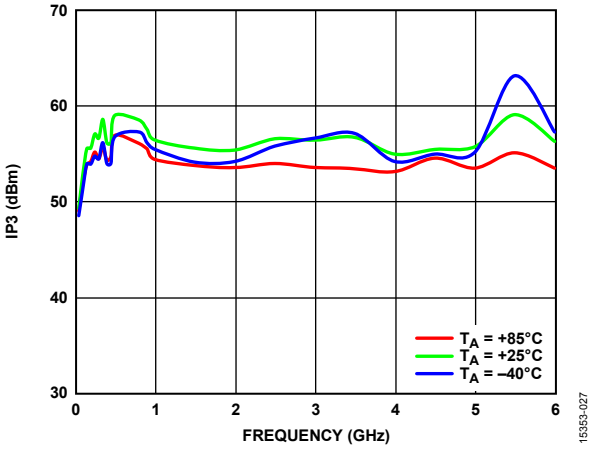


Figure 27. Input IP3 vs. Frequency at Minimum Attenuation State over Temperature, V_{DD} = 3 V

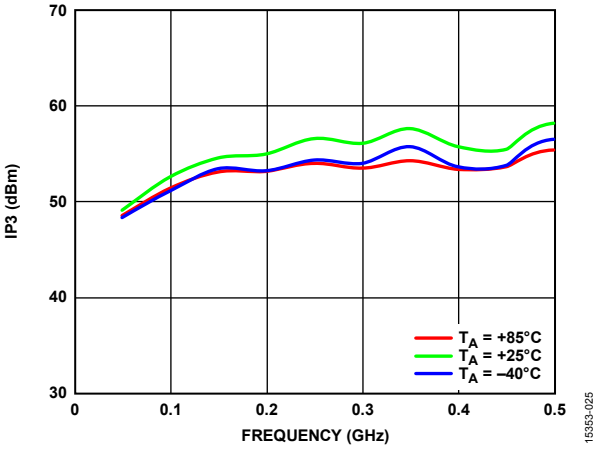


Figure 25. Input IP3 vs. Frequency at Minimum Attenuation State over Temperature, V_{DD} = 5 V (Low Frequency Detail)

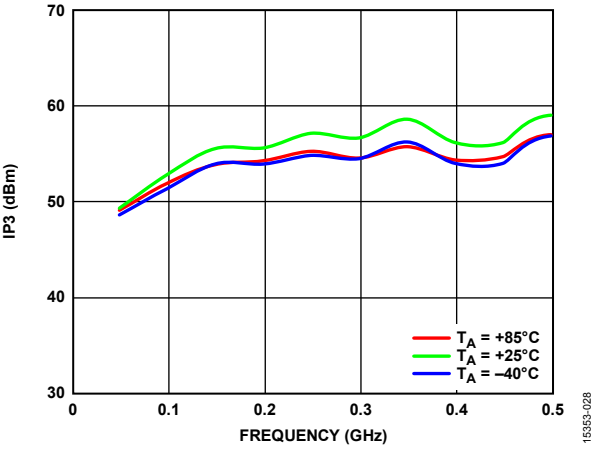


Figure 28. Input IP3 vs. Frequency at Minimum Attenuation State over Temperature, V_{DD} = 3 V (Low Frequency Detail)

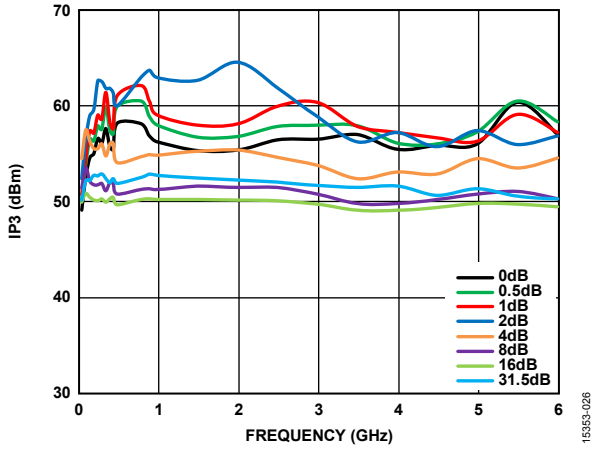


Figure 26. Input IP3 vs. Frequency over Major Attenuation States, V_{DD} = 5 V

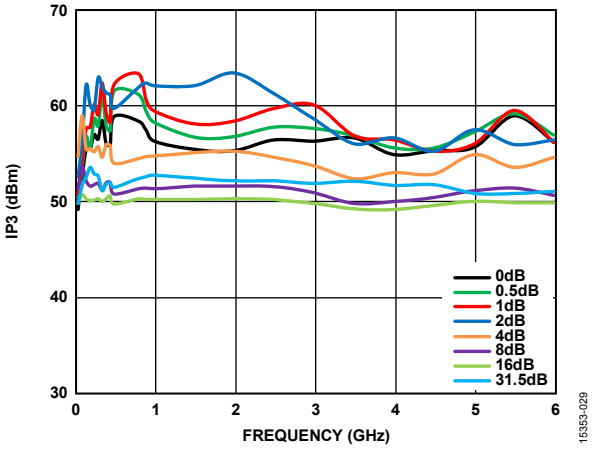


Figure 29. Input IP3 vs. Frequency over Major Attenuation States, V_{DD} = 3 V

THEORY OF OPERATION

The HMC624A incorporates a 6-bit attenuator die that offers an attenuation range of 31.5 dB in 0.5 dB steps. A CMOS driver die inside the HMC624A enables both serial and parallel mode control of the 6-bit attenuator (see Figure 30 and Table 6).

Table 6. D5 to D0 Truth Table

Digital Control Input[1]						Attenuation
D5	D4	D3	D2	D1	D0	State (dB)
High	High	High	High	High	High	0 (reference)
High	High	High	High	High	Low	0.5
High	High	High	High	Low	High	1.0
High	High	High	Low	High	High	2.0
High	High	Low	High	High	High	4.0
High	Low	High	High	High	High	8.0
Low	High	High	High	High	High	16.0
Low	Low	Low	Low	Low	Low	31.5

[1] Any combination of the control voltage input states shown in Table 6 provides an attenuation equal to the sum of the bits selected.

POWER SUPPLY

The HMC624A requires a single dc voltage applied to the VDD pin. The ideal power-up sequence is as follows:

1. Connect the ground reference.
2. Apply a supply voltage to the VDD pin.
3. Power up the digital control inputs. The relative order of the digital control inputs is not important.
4. Apply an RF input signal to ATTIN or ATTOUT.

The power-down sequence is the reverse of the power-up sequence.

POWER-UP INTERFACE

The HMC624A uses the PUP1 and PUP2 control voltage inputs to set the attenuation value to a known value at power-up before the initial control data word is provided in either serial or parallel mode. When the attenuator powers up with LE set to low, the state of PUP1 and PUP2 determines the power-up state of the device per the truth table shown in Table 7. The attenuator latches in the desired power-up state approximately 200 ms after power-up.

Table 7. PUPx Truth Table

Attenuation State	LE	PUP1	PUP2
31.5 dB	Low	Low	Low
24.0 dB	Low	High	Low
16.0 dB	Low	Low	High
0 dB (Reference)	Low	High	High
Determined by D0 to D5	High	Don't care	Don't care

SERIAL OR PARALLEL MODE SELECTION

The HMC624A can be controlled in either serial or parallel mode by setting the P/S pin to high or low, respectively (see Table 8).

Table 8. Mode Selection

P/S	Control Mode
Low	Parallel
High	Serial

SERIAL MODE INTERFACE

The HMC624A has a 3-wire serial peripheral interface (SPI): serial data input (SERIN), clock (CLK), and latch enable (LE). The serial control interface is activated when P/S is set to high.

In serial mode, the 6-bit SERIN data is clocked MSB first on the rising CLK edges into the shift register and then LE must be toggled high to latch the new attenuation state into the device. LE must be set to low to clock new 6-bit data into the shift register because CLK is masked to prevent the attenuator value from changing if LE is kept high (see Figure 31 and Table 2).

The HMC624A also features a serial data output pin, SEROUT, that outputs serial input data delayed by six clock cycles to control the cascaded attenuator using a single SPI bus.

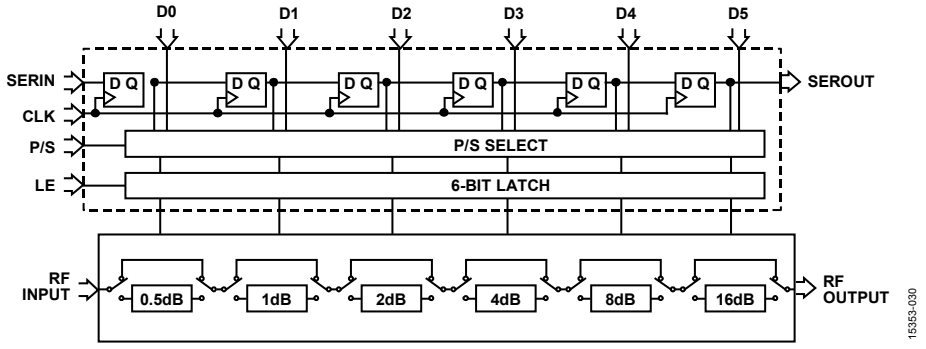


Figure 30. Simplified Circuit Diagram

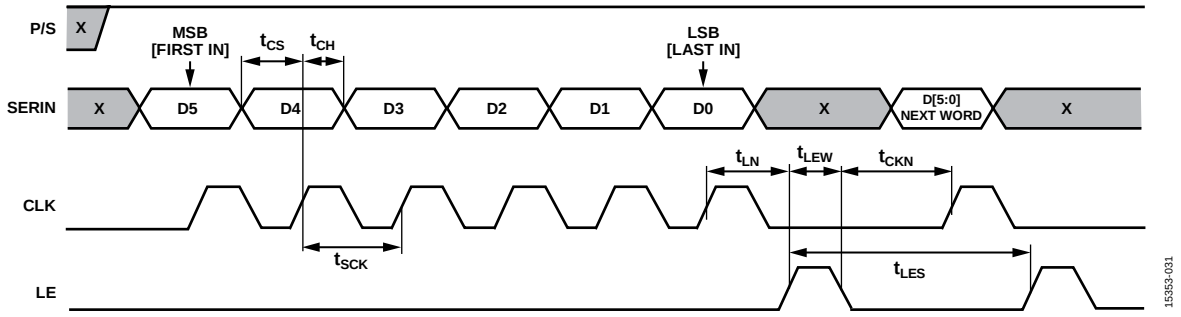


Figure 31. Serial Mode Timing Diagram

PARALLEL MODE INTERFACE

The HMC624A has six digital control inputs, D0 (LSB) to D5 (MSB), to select the desired attenuation state in parallel mode, as shown in Table 6. The parallel control interface is activated when P/S is set to low.

There are two modes of parallel operation: direct parallel and latched parallel.

Direct Parallel Mode

The LE pin must be kept high. The attenuation state is changed by the control voltage inputs (D0 to D5) directly. This mode is ideal for manual control of the attenuator.

Latched Parallel Mode

The LE pin must be kept low when changing the control voltage inputs (D0 to D5) to set the attenuation state. When the desired state is set, LE must be toggled high to transfer the 6-bit data to the bypass switches of the attenuator array, and then toggled low to latch the change into the device until the next desired attenuation change (see Figure 32 and Table 2).

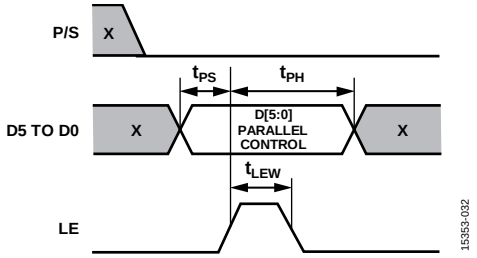


Figure 32. Latched Parallel Mode Timing Diagram

RF INPUT AND OUTPUT

The attenuator in the HMC624A is bidirectional; the ATTIN and ATTOUT pins are interchangeable as the RF input and output ports. The attenuator is internally matched to 50 Ω at both the input and the output; therefore, no external matching components are required.

The RF input and output pins of the HMC624A are internally dc-biased to V_{DD}; therefore, they require external dc blocking capacitors. Select the value of these dc blocking capacitors based on the minimum operating frequency; use larger value capacitors to extend the operation to lower frequencies.

ACGx PINS

The HMC624A is a positive bias GaAs attenuator; therefore, it requires floating capacitors between the attenuator bits and ground. The HMC624A uses on-chip floating capacitors that are sufficient for operation greater than 700 MHz. The HMC624A also features the ACGx pins to externally connect floating capacitors larger than 100 pF. Select the value of the external floating capacitors based on the minimum operating frequency, whereas the ACGx pins can be left open when operating above 700 MHz.

APPLICATIONS INFORMATION

EVALUATION BOARD

The HMC624A uses a 4-layer evaluation board. The copper thickness is 0.5 oz (0.7 mil) on each layer. The top dielectric material is 10 mil Rogers RO4350 for optimal high frequency performance, whereas the middle and bottom dielectric materials are FR-4 type materials to achieve an overall board thickness of 62 mil. RF traces are routed on the top copper layer, and the bottom layer is a grounded plane that provides a solid ground for the RF transmission lines. The RF transmission lines are designed using a coplanar waveguide (CPWG) model with a width of 16 mil and ground spacing of 13 mil to have a characteristic impedance of 50 Ω. For enhanced RF and thermal grounding, as many plated through vias as possible are arranged around transmission lines and under the exposed pad of the package.

Figure 33 shows the top view of the populated HMC624A evaluation board, available from Analog Devices, Inc., upon request (see the Ordering Guide).

The evaluation board is grounded from the dc pin, J11. The dc supply must be connected to the dc pin, J8, of the evaluation board. A 1 nF decoupling capacitor is placed on the supply trace to filter high frequency noise.

The RF input and output ports (ATTIN and ATTOUT) are connected through 50 Ω transmission lines to the SMA connectors, J1 and J2, respectively. The ATTIN and ATTOUT ports are ac-coupled with 330 pF capacitors. A thru calibration line is used to estimate the loss of the PCB over the environmental conditions being evaluated.

All the digital control pins are connected through digital signal traces to the 2 × 9-pin header, J3. The HMC624A evaluation board also uses two dual inline package (DIP), and four-position, single-pole dual-throw (SPDT) switches for the manual control of the device in direct parallel mode.

Figure 34 and Table 9 show the evaluation board schematic and bill of materials, respectively.

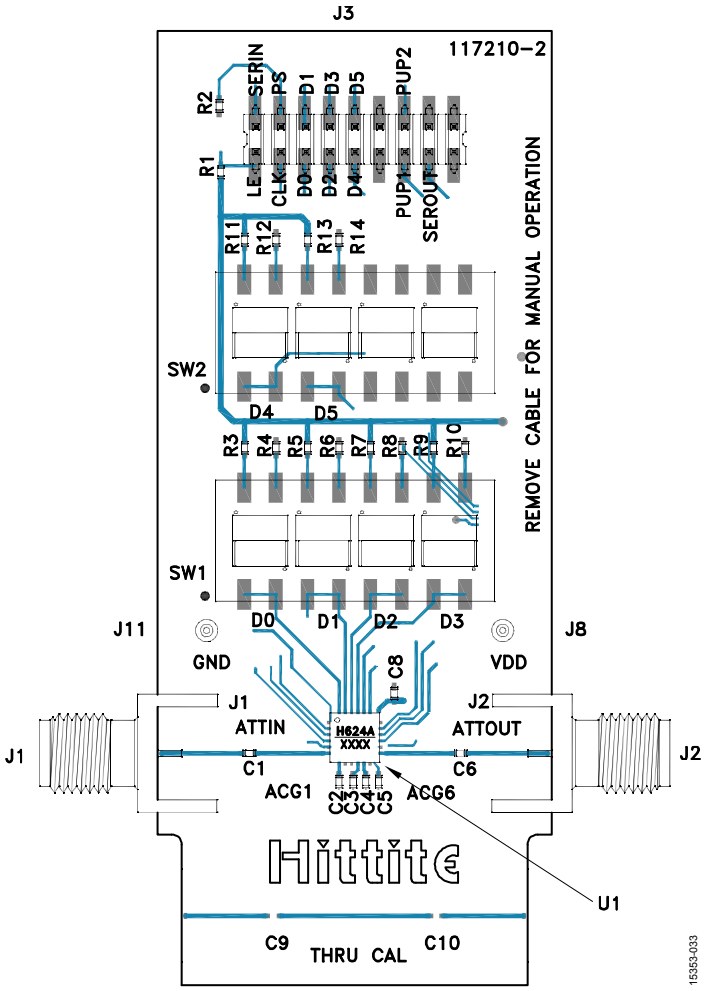


Figure 33. Populated Evaluation Board—Top View

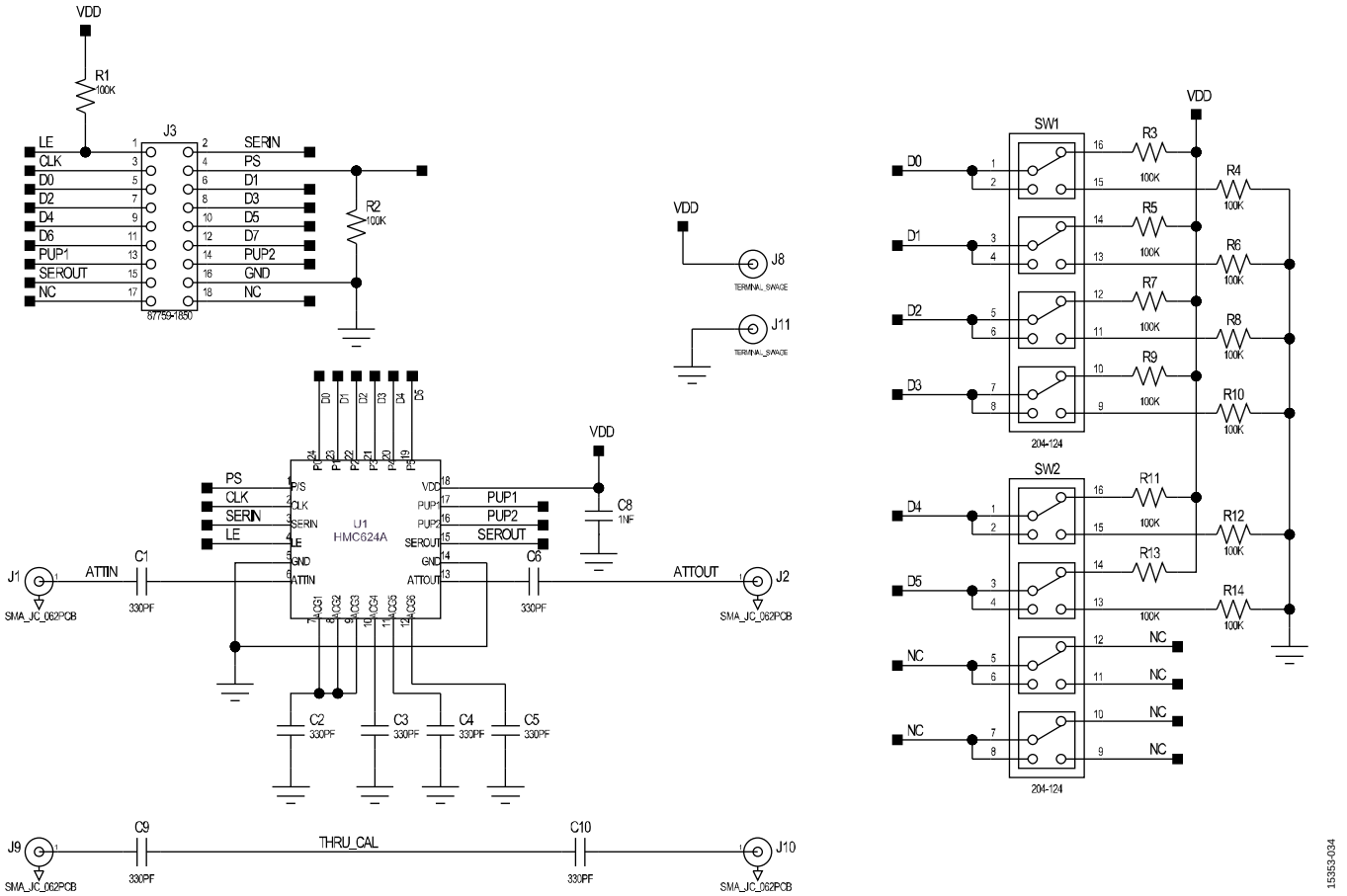
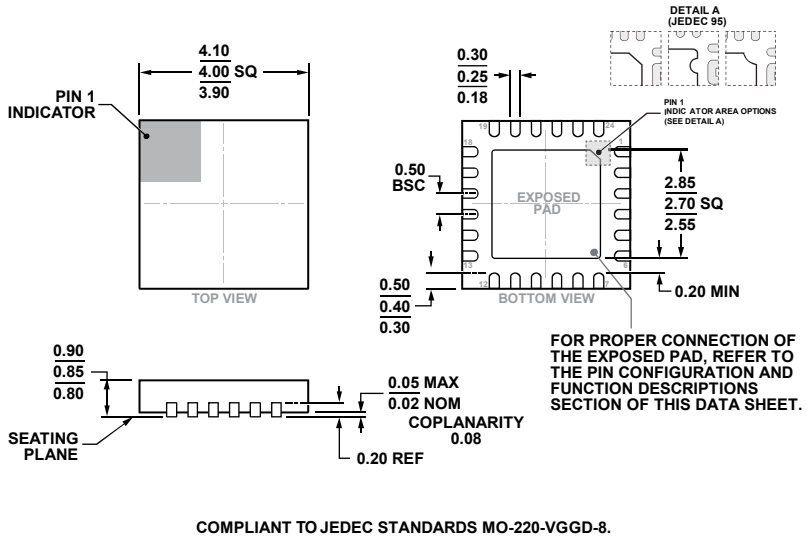


Figure 34. Evaluation Board Schematic

Table 9. Evaluation Board Bill of Materials

Component	Default Value	Description
J1, J2	Not applicable	SMA connector
J3	Not applicable	2 × 9-pin header
J8, J11	Not applicable	DC pins
J9, J10	Do not insert	SMA connector
C1 to C6	330 pF	Capacitor, 0402 package
C8	1 nF	Capacitor, 0402 package
C9, C10	Do not insert	Capacitor, 0402 package
R1 to R14	100 kΩ	Resistor, 0402 package
SW1, SW2	Not applicable	SPDT four-position DIP switch
U1	HMC624A	Digital attenuator, Analog Devices, Inc.
PCB	117210-2	Evaluation PCB, Analog Devices

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-220-VGGD-8.

Figure 35. 24-Lead Lead Frame Chip Scale Package [LFCSP]
4 mm × 4 mm Body and 0.85 mm Package Height
(CP-24-16)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	MSL Rating[2]	Package Description	Package Option	Branding[3]
HMC624ALP4E	−40°C to +85°C	MSL1	24-Lead Lead Frame Chip Scale Package [LFCSP]	CP-24-16	H624A XXXX
HMC624ALP4ETR	−40°C to +85°C	MSL1	24-Lead Lead Frame Chip Scale Package [LFCSP]	CP-24-16	H624A XXXX
117212-HMC624ALP4			Evaluation Board		

[1] E = RoHS Compliant Part.
[2] See the Absolute Maximum Ratings section.
[3] XXXX is the 4-digit lot number.