FAIRCHILD

April 2016

FAN7080_GF085
Half Bridge Gate Driver

Features

- Automotive Qualified to AEC Q100
- Floating Channel for Bootstrap Operation to +600 V
- Tolerance to Negative Transient Voltage on VS Pin
- VS-pin dv/dt Immune
- Gate Drive Supply Range from 5.5 V to 20 V
- Under-Voltage Lockout (UVLO)
- CMOS Schmitt-triggered Inputs with Pull-down
- High Side Output In-phase with Input
- IN input is 3.3 V/5 V Logic Compatible and Available on 15 V Input
- Matched Propagation Delay for both Channels
- Dead Time Adjustable

Applications

- Junction Box
- Half and full bridge application in the motor drive system Related Product Resources

Description

The FAN7080_GF085 is a half-bridge gate drive IC with reset input and adjustable dead time control. It is designed for high voltage and high speed driving of MOSFET or IGBT, which operates up to 600 V. Fairchild's high-voltage process and common-mode noise cancellation technique provide stable operation in the high side driver under high-dV/dt noise circumstances. An advanced level-shift circuit allows high-side gate driver operation up to V_S=-5 V (typical) at V_{BS}=15 V. Logic input is compatible with standard CMOS outputs. The UVLO circuits for both channels prevent from malfunction when V_{CC} and V_{BS} are lower than the specified threshold voltage. Combined pin function for dead time adjustment and reset shutdown make this IC packaged with space saving SOIC-8 Package. Minimum source and sink current capability of output driver is 250 mA and 500 mA respectively, which is suitable for junction box application and half and full bridge application in the motor drive system.

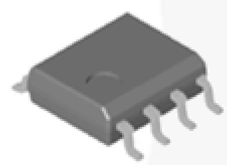
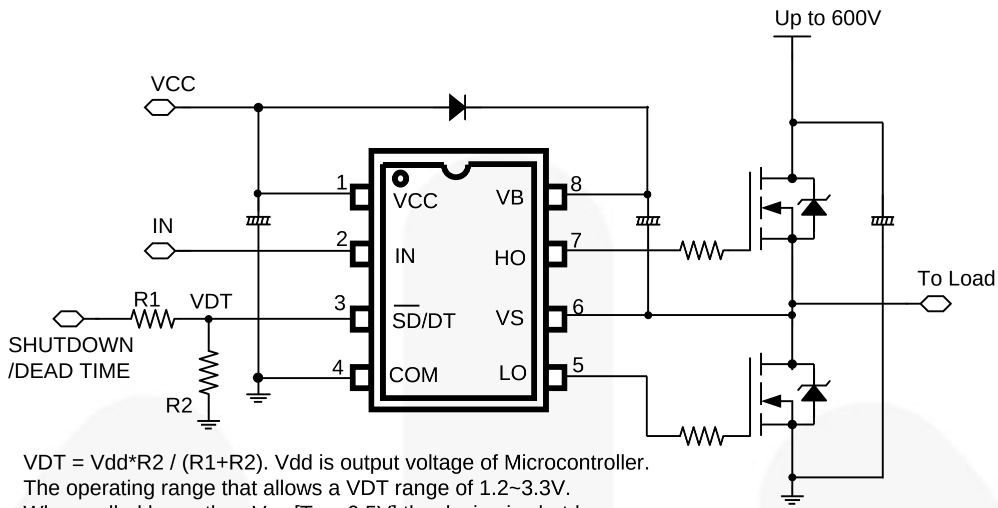


Figure 1. 8-Lead, SOIC, Narrow Body

Ordering Information

Part Number	Operating Temperature Range	Package	Packing Method
FAN7080M_GF085	-40°C ~ 125°C	8-Lead, Small Outline Integrated Circuit (SOIC), JEDEC MS-012, .150 inch Narrow Body	Tube
FAN7080MX_GF085			Tape & Reel

Typical Application



VDT = Vdd*R2 / (R1+R2). Vdd is output voltage of Microcontroller.
The operating range that allows a VDT range of 1.2~3.3V.
When pulled lower than V_{DT} [Typ. 0.5V] the device is shutdown.
Care must be taken to avoid below threshold spikes on pin 3 that can cause undesired shut down of the IC. For this reason the connection of the components between pin 3 and ground has to be as short as possible. And a capacitor (Typ. 0.02µF)between pin3 and COM can prevent this spike. This pin can not be left floating for the same reason.

Figure 2. Typical Application

Block Diagram

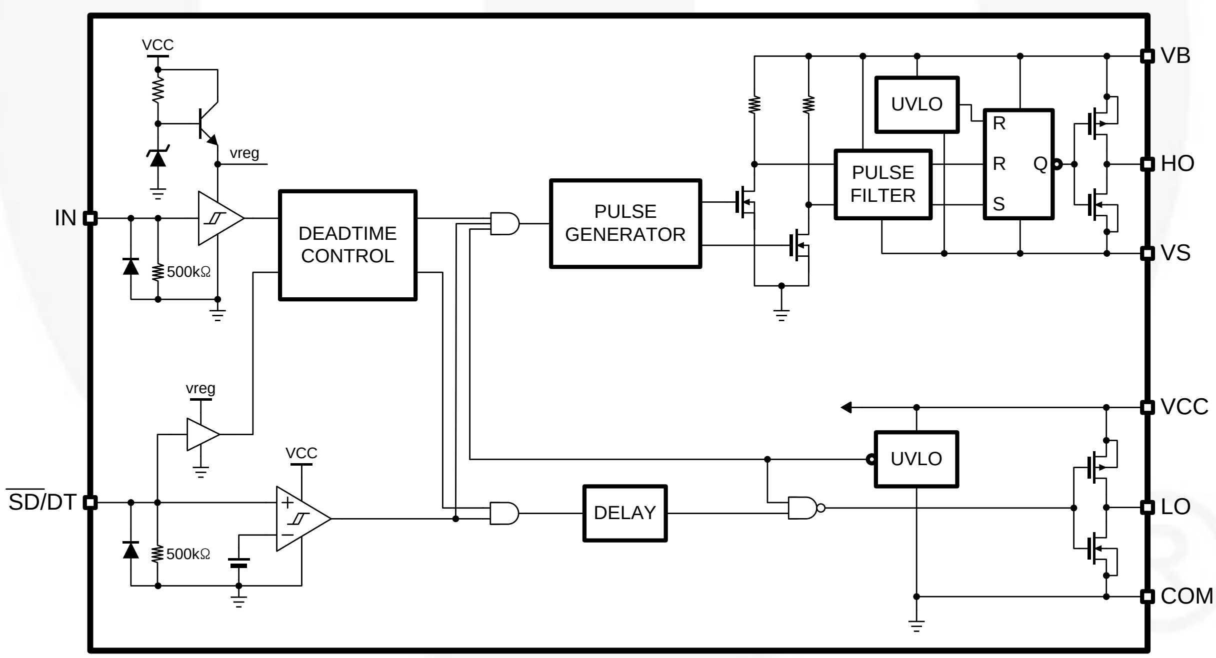


Figure 3. Block Diagram

Pin Configuration

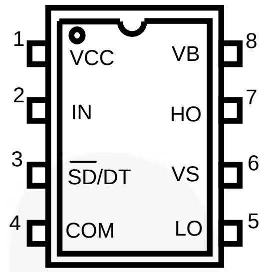


Figure 4. Pin Assignment (Top Through View)

Pin Descriptions

Pin #	Name	I/O	Pin Function Description
1	V_{CC}	P	Driver Supply Voltage
2	IN	I	Logic input for high and low side gate drive output
3	/SD/DT	I	Shutdown Input and dead time setting
4	COM	P	Ground
5	LO	A	Low side gate drive output for MOSFET Gate connection
6	V_S	A	High side floating offset for MOSFET Source connection
7	HO	A	High side drive output for MOSFET Gate connection
8	V_B	P	Driver Output Stage Supply

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter	Min.	Max.	Unit
V_S	High-Side Floating Offset Voltage	V_B-25	V_B+0.3	V
V_B	High-Side Floating Supply Voltage	-0.3	625	V
V_{HO}	High-Side Floating Output Voltage	V_S-0.3	V_B+0.3	V
V_{LO}	Low-Side Floating Output Voltage	-0.3	V_{cc}+0.3	V
V_{CC}	Supply Voltage	-0.3	25	V
V_{IN}	Input Voltage for IN	-0.3	V_{CC}+0.3	V
I_{IN}	Input Injection Current (1)		+1	mA
PD	Power Dissipation (2.3)		0.625	W
θ_{JA}	Thermal Resistance, Junction to Ambient (2)		200	°C/W
T_J	Junction Temperature		150	°C
T_{STG}	Storage Temperature	-55	150	°C
ESD	Human Body Model (HBM)		1000	V
	Charge Device Model (CDM)		500	

Notes:

1. Guaranteed by design. Full function, no latchup. Tested at 10 V and 17 V.
2. The Thermal Resistance and power dissipation rating are measured per below conditions:
   JESD51-2: Integral circuits thermal test method environmental conditions, natural convection/Still Air
   JESD51-3: Low effective thermal conductivity test board for leaded surface-mount packages.
3. Do not exceed power dissipation (P_D) under any circumstances.

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance. Fairchild does not recommend exceeding them or designing to Absolute Maximum Ratings.

Symbol	Parameter	Min.	Max.	Unit
V_B (4)	High-Side Floating Supply Voltage (DC) Transient: -10 V at 0.1 µS	V_S+6	V_S+20	V
V_S	High-Side Floating Supply Offset Voltage (DC) Transient: -25 V(max.) at 0.1 µS at V_{BS} < 25 V	-5	600	V
V_{HO}	High-Side Output Voltage	V_S	V_B	V
V_{LO}	Low-Side Output Voltage	0	V_{CC}	V
V_{CC}	Supply Voltage for Logic Input	5.5	20	V
V_{IN}	Logic Input Voltage	0	V_{CC}	V
dv/dt	Allowable Offset Voltage Slew Rate (5)		50	V/nS
T_{PULSE}	Minimum Pulse Width (5,6)	1100		nS
F_S	Switching Frequency (6)		200	KHz
T_A	Operating Ambient Temperature	-40	125	°C

Notes:

4. The V_S offset is tested with all supplies based at 15 V differential
5. Guaranteed by design.
6. When V_{DT} = 1.2 V. Refer to Figures 5, 6, 7 and 8.

Electrical Characteristics

Unless otherwise specified -40°C ≤ T_A ≤ 125°C, V_{CC} = 15 V, V_{BS}=15 V, V_S = 0 V, C_L =1 nF

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{CC} and V_{BS} Supply Characteristics						
V_{CCUV+} V_{BSUV+}	V_{CC} and V_{BS} Supply Under-Voltage Positive going Threshold			4.2	5.5	V
V_{CCUV-} V_{BSUV-}	V_{CC} and V_{BS} Supply Under-Voltage Negative going Threshold		2.8	3.6		V
V_{CCUVH} V_{BSUVH}	V_{CC} and V_{BS} Supply Under-Voltage Hysteresis		0.2	0.6		V
t_{DUVCC}	Under-Voltage Lockout Response Time	V_{CC}: 6 V→2.5 V or 2.5 V→6 V	0.5		20	µs
t_{DUVBS}		V_{BS}: 6 V→2.5 V or 2.5 V→6 V	0.5		20	µs
I_{LK}	Offset Supply Leakage Current	V_B = V_S = 600 V		20	50	µA
IQ_{BS}	Quiescent V_{BS} Supply Current	V_{IN} = 0 or 5 V, V_{SDT} = 1.2 V	20	75	150	µA
IQ_{CC}	Quiescent V_{CC} Supply Current	VI_N = 0 or 5 V, V_{SDT} = 1.2 V		350	1000	µA
Input Characteristics						
V_{IH}	High Logic level Input Voltage		2.7			V
V_{IL}	Low Logic Level Input Voltage				0.8	V
I_{IN+}	Logic Input High Bias Current	V_{IN} = 5 V		10	50	µA
I_{IN-}	Logic Input Low Bias Current	V_{IN} = 0 V		0	2	µA
V_{DT}	V_{DT} Dead Time Setting Range		1.2		5.0	V
V_{SD}	V_{SD} Shutdown Threshold Voltage			0.8	1.2	V
R_{SDT}	High Logic Level Resistance for /SD /DT	V_{SDT} = 5 V	100	500	1100	kΩ
I_{SDT-}	Low Logic Level Input bias Current for /SD /DT	V_{SDT} = 0 V		1	2	µA
Output Characteristics						
$V_{OH(HO)}$	High Level Output Voltage (V_{CC} - V_{HO})	I_O = 0			0.1	V
$V_{OL(HO)}$	Low Level Output Voltage (V_{HO})	I_O = 0			0.1	V
$I_{O+(HO)}$	Output High, Short-Circuit Pulse Current		250	300		mA
$I_{O-(HO)}$	Output Low, Short-Circuit Pulse Current		500	600		mA
$R_{OP(HO)}$	Equivalent Output Resistance				60	Ω
$R_{ON(HO)}$					30	Ω
$V_{OH(LO)}$	High Level Output Voltage (V_B – V_{LO})	I_O = 0			0.1	V
$V_{OL(LO)}$	Low Level Output Voltage (V_{LO})	I_O = 0			0.1	V
$I_{O+(LO)}$	Output High, Short-Circuit Pulse Current		250			mA
$I_{O-(LO)}$	Output Low, Short-Circuit Pulse Current		500			mA
$R_{OP(LO)}$	Equivalent Output Resistance				60	Ω
$R_{ON(LO)}$					30	Ω

Dynamic Electrical Characteristics

Unless otherwise specified -40°C ≤ T_A ≤ 125°C, V_{CC} = 15 V, V_{BS}=15 V, V_S = 0 V, C_L =1 nF

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
t_{ON}	Turn-On Propagation Delay[7]	V_S=0 V		750	1500	ns
t_{OFF}	Turn-Off Propagation Delay	V_S=0 V		130	250	ns
t_R	Turn-On Rise Time			40	150	ns
t_F	Turn-Off Fall Time			25	400	ns
D_T	Dead Time, LS Turn-off to HS Turn-on and HS Turn-on to LS Turn-off	V_{IN} = 0 or 5 V at VDT = 1.2 V	250	650	1200	ns
		V_{IN} = 0 or 5 V at VDT = 1.2 V	1600	2100	2600	
M_{DT}	Dead Time Matching Time	DT1 – DT2 at VDT = 1.2 V		35	110	ns
		DT1 – DT2 at VDT = 3.3 V			300	
M_{TON}	Delay Matching, HS and LS Turn-on	VDT = 1.2 V		25	110	ns
M_{TOFF}	Delay Matching, HS and LS Turn-off	VDT = 1.2 V		15	60	ns
t_{SD}	Shutdown Propagation Delay			180	330	ns
F_S1	Switching Frequency	V_{CC} = V_{BS} = 20 V			200	Khz
F_S2		V_{CC} = V_{BS} = 5.5 V			200	

Notes:

7. t_{ON} includes DT

Typical Waveforms

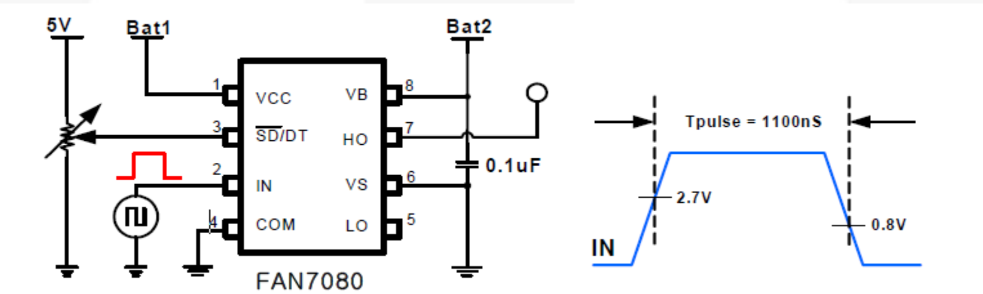


Figure 5. Short Pulse Width Test Circuit and Pulse Width Waveform

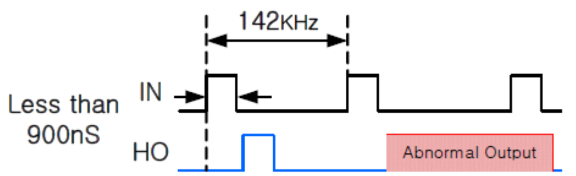


Figure 6. Abnormal Output Waveform with Pulse Width

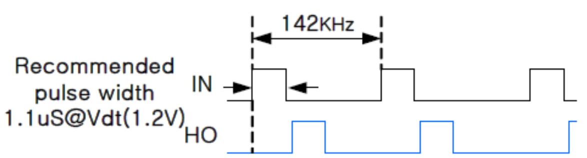


Figure 7. Recommendation of Pulse width Output Waveform

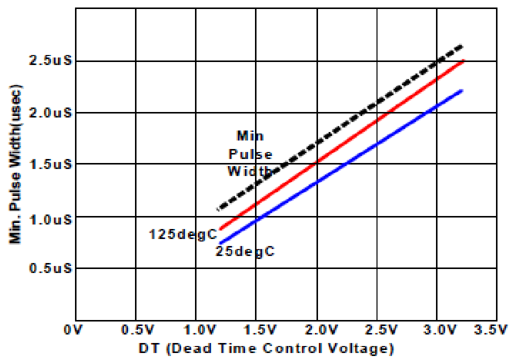


Figure 8. Pulse Width vs. VDT

Typical Performance Characteristics

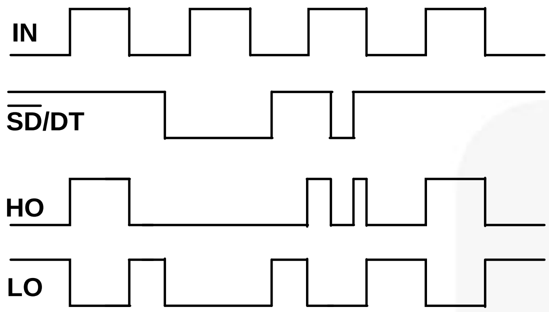


Figure 9. Input/Output Timing Diagram

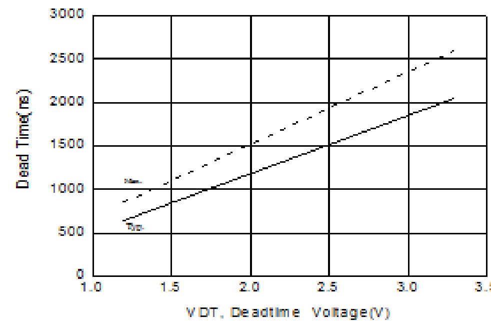


Figure 10. Dead Time vs. V_{DT} (V_{CC}=V_{BS}=15 V, -40°C < T_J < 125°C)

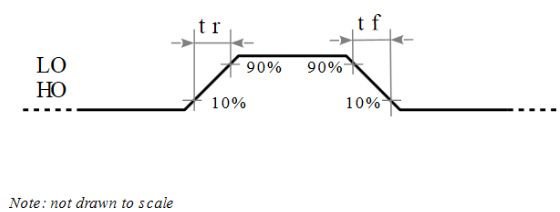


Figure 11. Switching Time Waveform Definitions

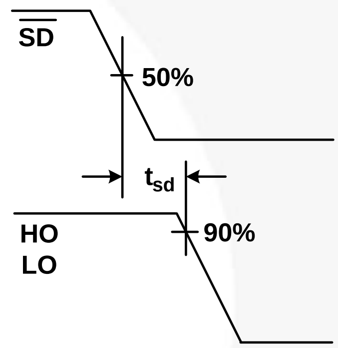


Figure 12. Shutdown Waveform Definitions

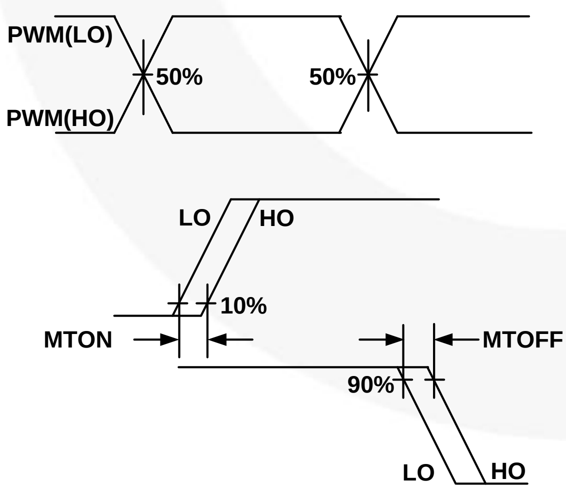


Figure 13. Delay Matching Waveform Definitions

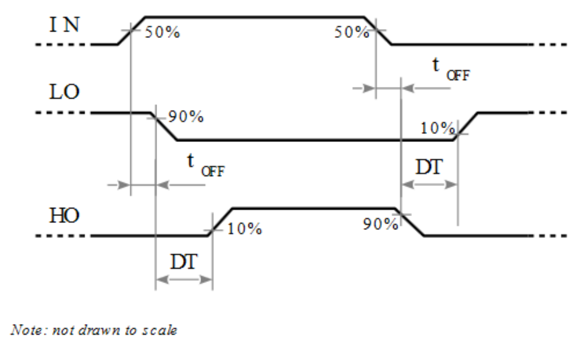


Figure 14. Dead Time Waveform Definitions

Typical Performance Characteristics

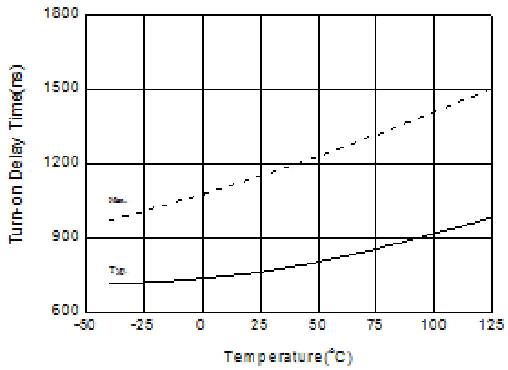


Figure 15. Turn-on Delay Time of HO vs. Temperature (V_{CC}=V_{BS}=15 V, C_L=1 nF)

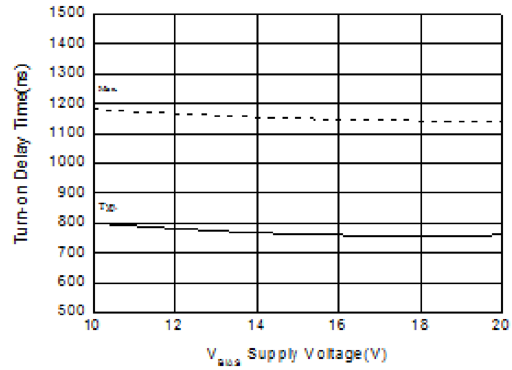


Figure 16. Turn-on Delay Time of HO vs. V_{BS} Supply Voltage (V_{CC}=15 V, C_L=1 nF, T_A=25°C)

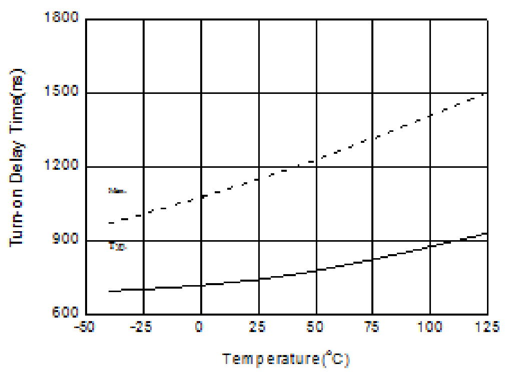


Figure 17. Turn-on Delay Time of LO vs. Temperature (V_{CC}=V_{BS}=15 V, C_L=1 nF)

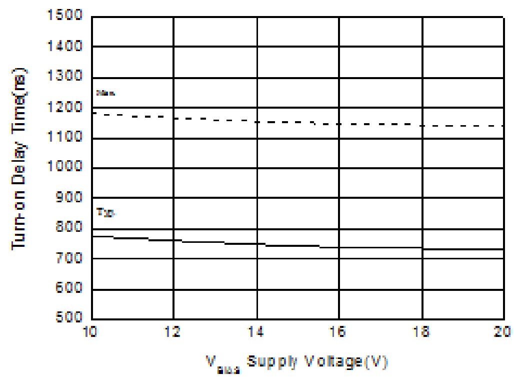


Figure 18. Turn-on Delay Time of LO vs. V_{BS} Supply Voltage (V_{CC}=15 V, C_L=1 nF, T_A=25°C)

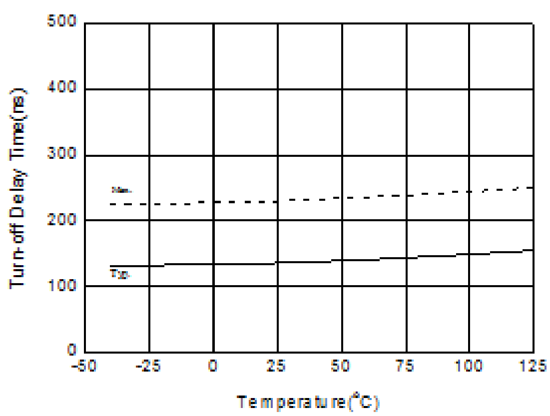


Figure 19. Turn-off Delay Time of HO vs. Temperature (V_{CC}=V_{BS}=15 V, C_L=1 nF)

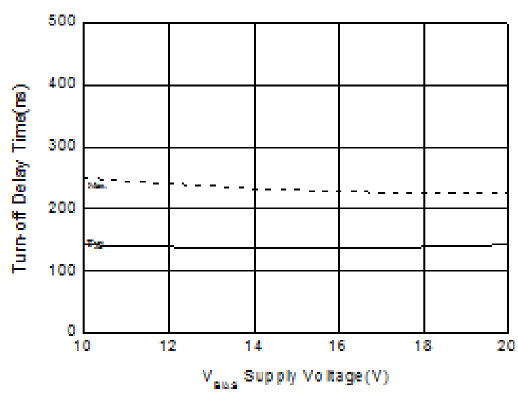


Figure 20. Turn-off Delay Time of HO vs. V_{BS} Supply Voltage (V_{CC}=15 V, C_L=1 nF, T_A=25°C)

Typical Performance Characteristics

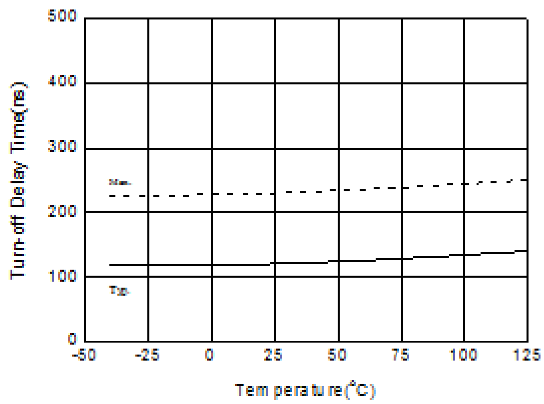


Figure 21. Turn-off Delay Time of LO vs. Temperature (V_{CC}=V_{BS}=15 V, C_L=1 nF)

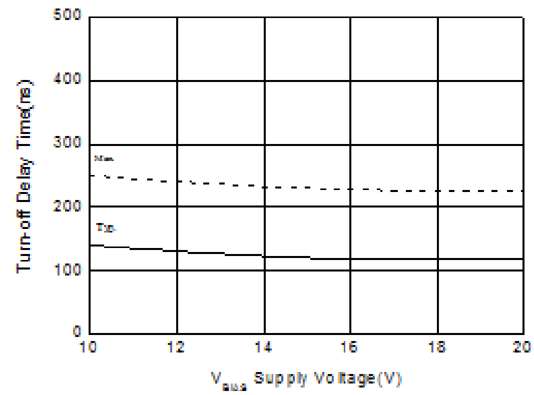


Figure 22. Turn-off Delay Time of LO vs. V_{BS} Supply Voltage (V_{CC}=15 V, CL=1 nF, T_A=25°C)

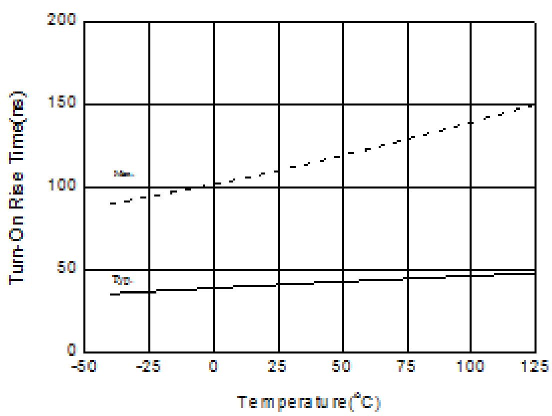


Figure 23. Turn-on Rise Time of HO vs. Temperature (V_{CC}=V_{BS}=15 V, C_L=1 nF)

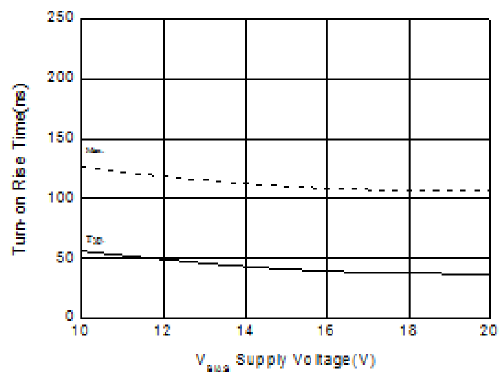


Figure 24. Turn-on Rise Time of HO vs. V_{BS} Supply Voltage (V_{CC}=15 V, CL=1 nF, T_A=25°C)

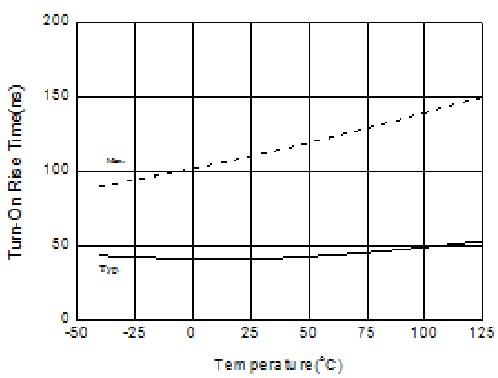


Figure 25. Turn-on Rise Time of LO vs. Temperature (V_{CC}=V_{BS}=15 V, C_L=1 nF)

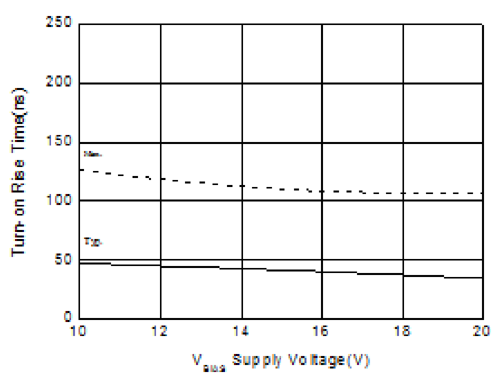


Figure 26. Turn-on Rise Time of LO vs. V_{BS} Supply Voltage (V_{CC}=15 V, C_L=1 nF, T_A=25°C)

Typical Performance Characteristics

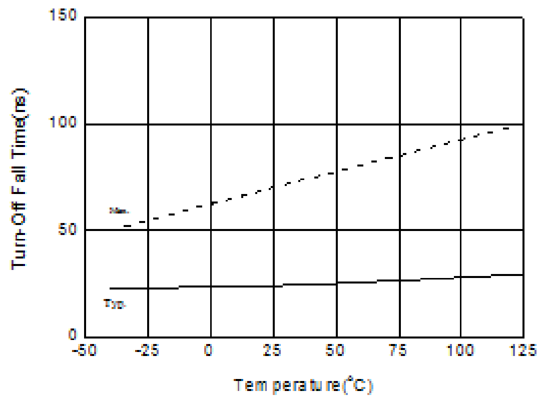


Figure 27. Turn-off Fall Time of HO vs. Temperature (V_{CC}=V_{BS}=15 V, C_L=1 nF)

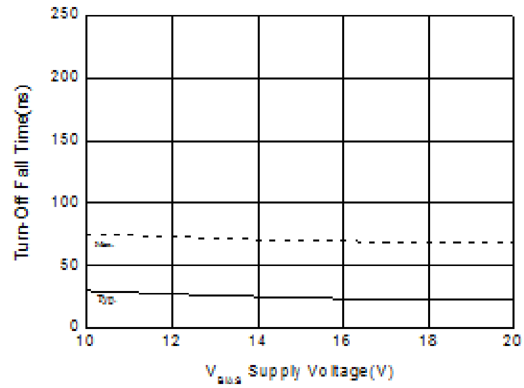


Figure 28. Turn-off Fall Time of HO vs. V_{BS} Supply Voltage (V_{CC}=15 V, C_L=1 nF, T_A=25°C)

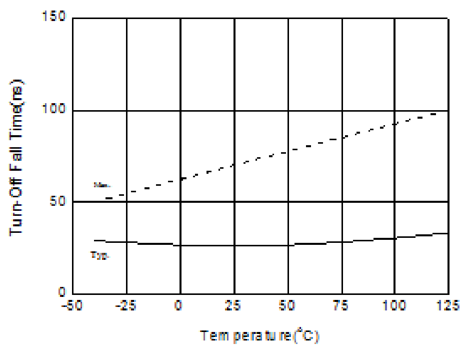


Figure 29. Turn-off Fall Time of LO vs. Temperature (V_{CC}=V_{BS}=15 V, C_L=1 nF)

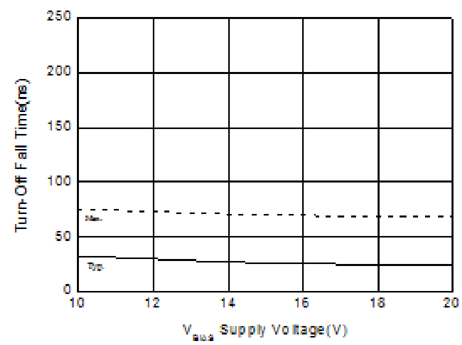


Figure 30. Turn-off Fall Time of LO vs. Temperature (V_{CC}=V_{BS}=15 V, C_L=1 nF)

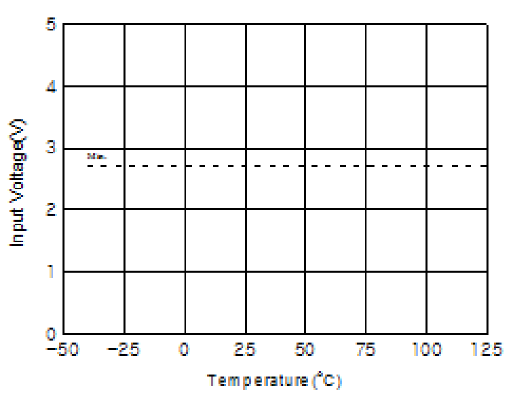


Figure 31. Logic Low Input Voltage vs. Temperature

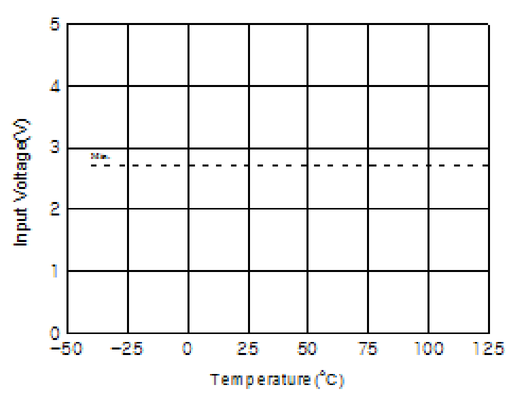


Figure 32. Logic High Input Voltage vs. Temperature

Typical Performance Characteristics

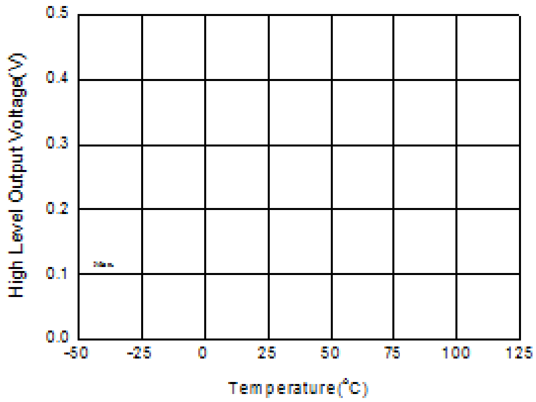


Figure 33. High Level Output of HO vs. Temperature (V_{CC}=V_{BS}=15 V)

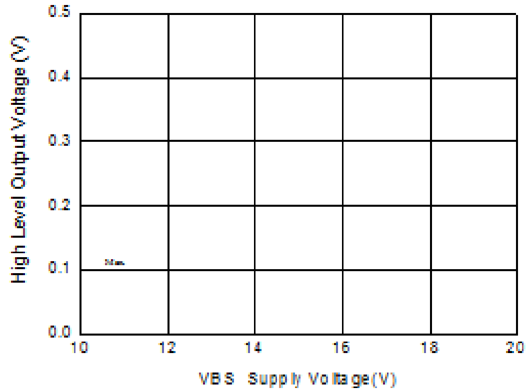


Figure 34. High Level Output of HO vs. V_{BS} Supply Voltage (V_{CC}=15 V, T_A=25°C)

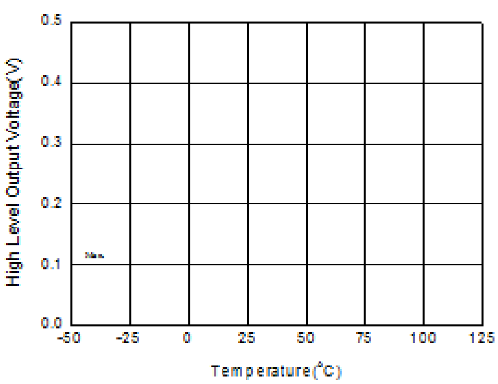


Figure 35. High Level Output of LO vs. Temperature (V_{CC}=V_{BS}=15 V)

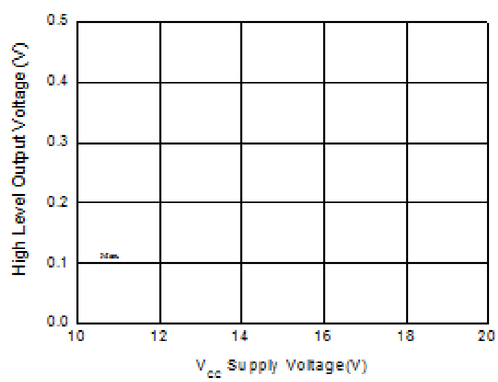


Figure 36. High Level Output of LO vs. V_{BS} Supply Voltage (V_{CC}=15 V, T_A=25°C)

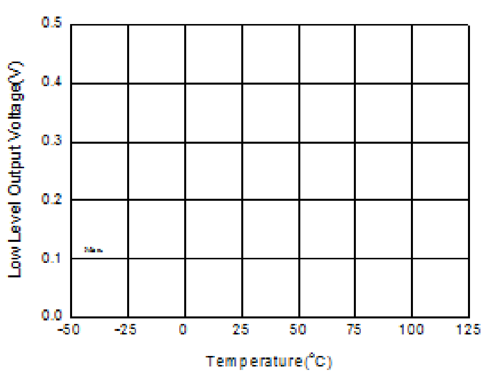


Figure 37. Low Level Output of HO vs. Temperature (V_{CC}=V_{BS}=15 V)

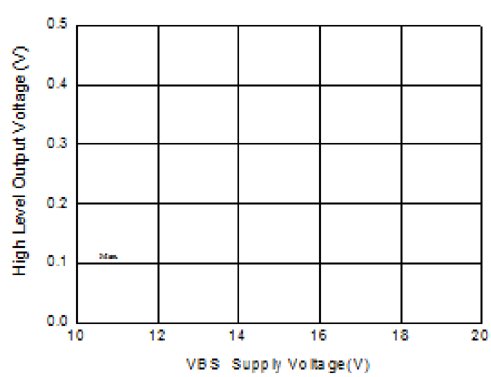


Figure 38. Low Level Output of HO vs. V_{BS} Supply Voltage (V_{CC}=15 V, T_A=25°C)

Typical Performance Characteristics

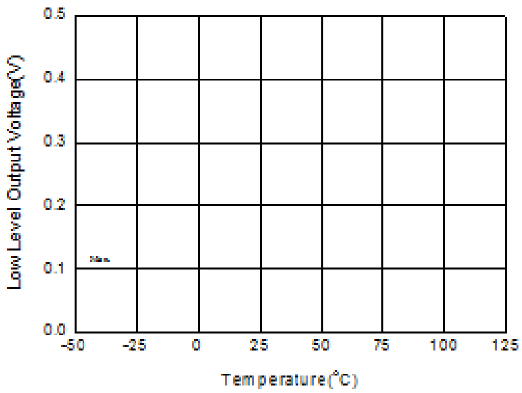


Figure 39. Low Level Output of LO vs. Temperature (V_{CC}=V_{BS}=15 V)

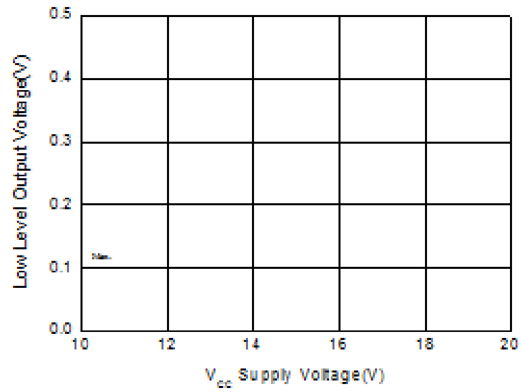


Figure 40. Low Level Output of LO vs. V_{CC} Supply Voltage (V_{CC}=15 V, T_A=25°C)

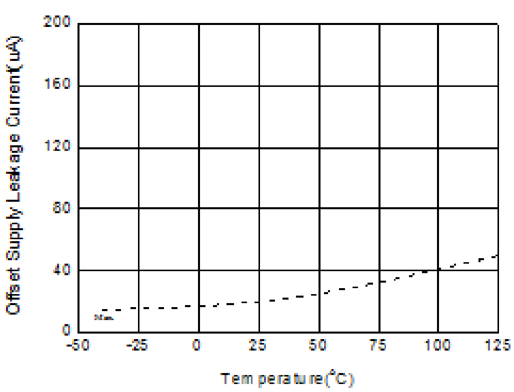


Figure 41. Offset Supply Leakage Current vs. Temperature (V_{CC}=V_{BS}=600 V)

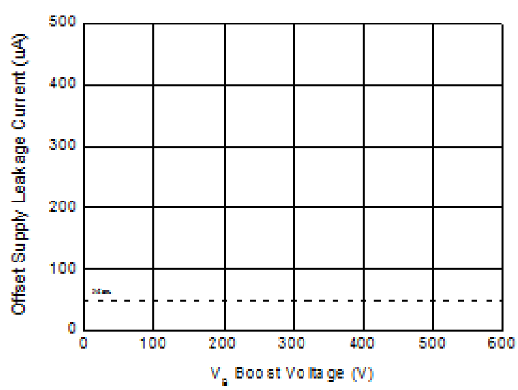


Figure 42. Offset Supply Leakage Current vs. V_B Boost Voltage(V_{CC}=15 V, T_A=25°C)

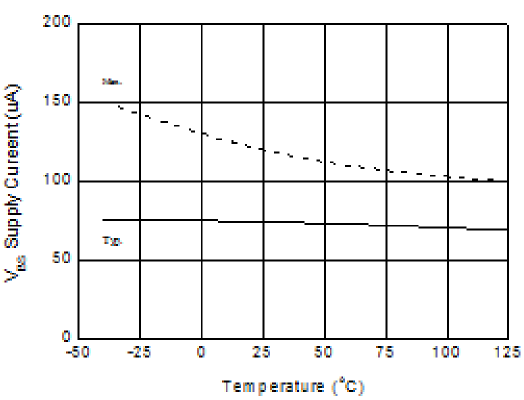


Figure 43. V_{BS} Supply Current vs. Temperature (V_{BS}=15 V)

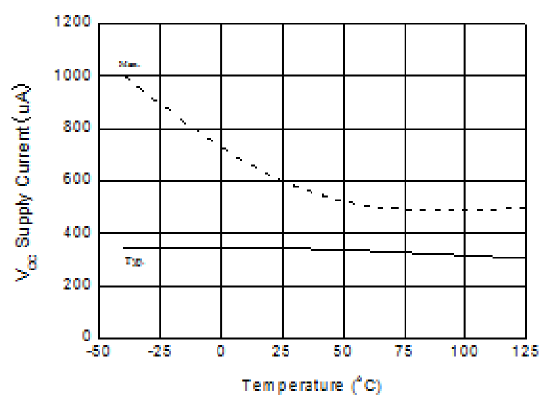


Figure 44. V_{CC} Supply Current vs. Temperature (V_{CC}=15 V)

Typical Performance Characteristics

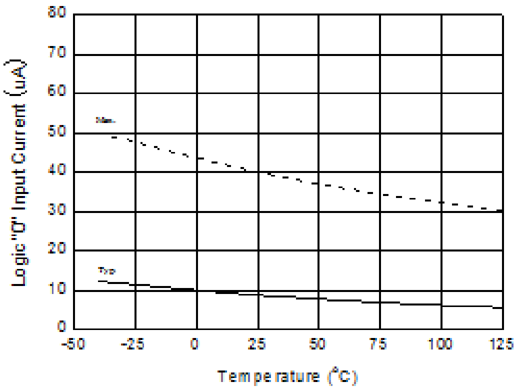


Figure 45. Logic High Input Current vs. Temperature (V_{IN}=5 V)

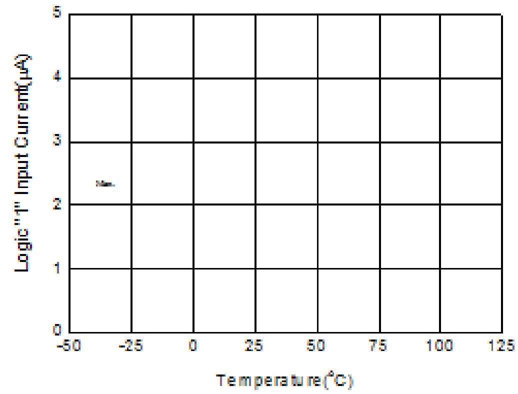


Figure 46. Logic Low Input Current vs. Temperature (V_{IN}=5 V)

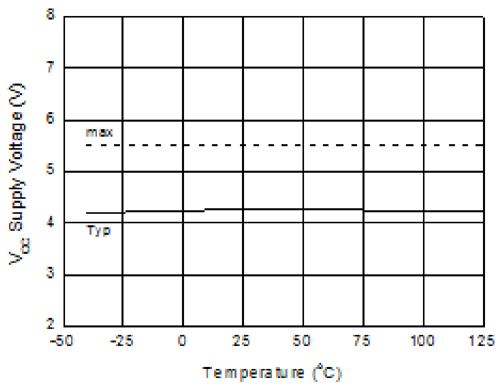


Figure 47. V_{CC} Under-Voltage Threshold (+) vs. Temperature

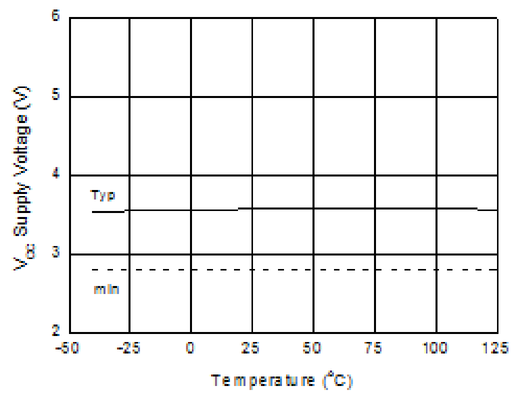


Figure 48. V_{CC} Under-Voltage Threshold (-) vs. Temperature

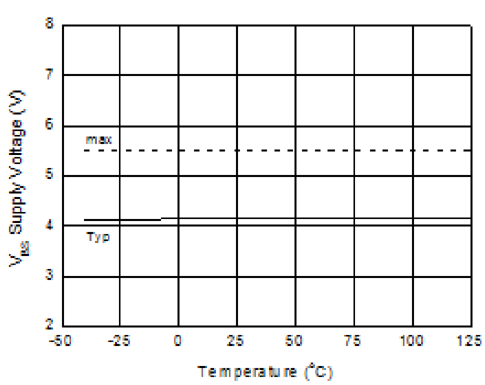


Figure 49. V_{BS} Under-Voltage Threshold (+) vs. Temperature

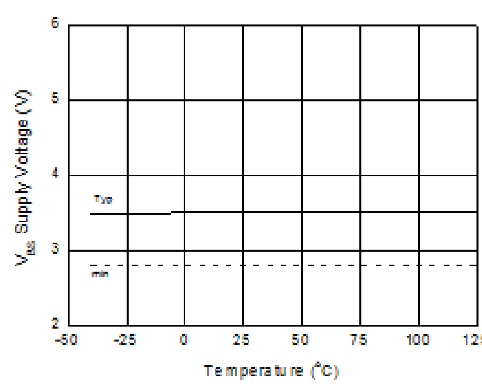


Figure 50. V_{BS} Under-Voltage Threshold (-) vs. Temperature

Typical Performance Characteristics

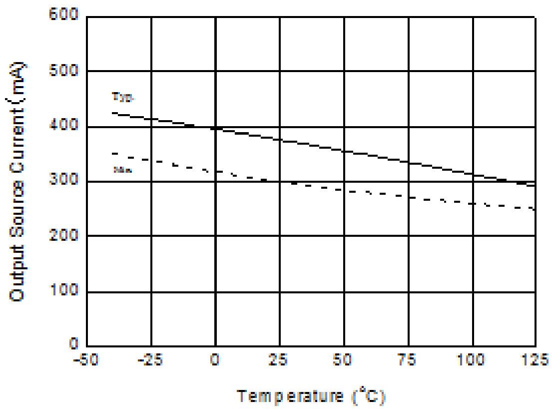


Figure 51. Output Source Current of HO vs. Temperature (V_{CC}=V_{BS}=15 V)

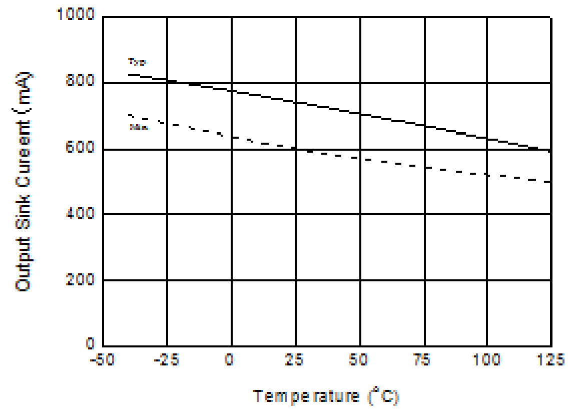


Figure 52. Output Sink Current of HO vs. Temperature (V_{CC}=V_{BS}=15 V

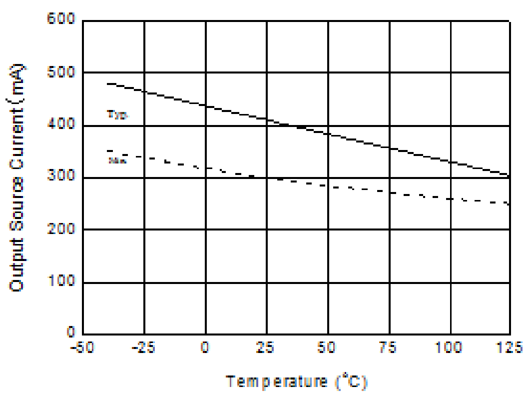


Figure 53. Output Source Current of LO vs. Temperature (V_{CC}=V_{BS}=15 V)

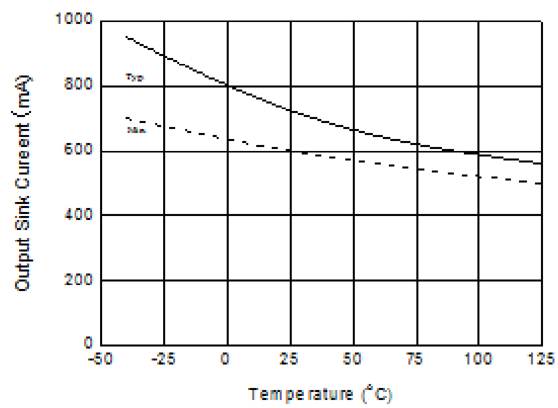


Figure 54. Output Sink Current of LO vs. Temperature (V_{CC}=V_{BS}=15 V

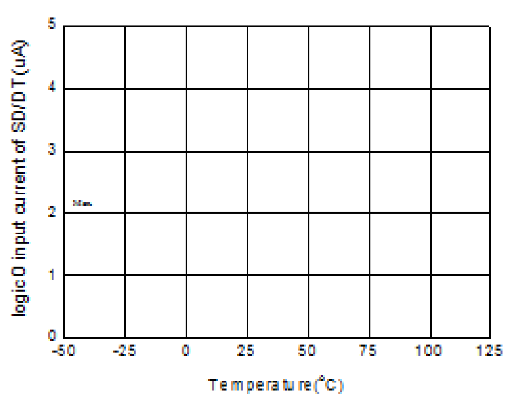


Figure 55. Logic Low Input Current of SD/DT vs. Temperature

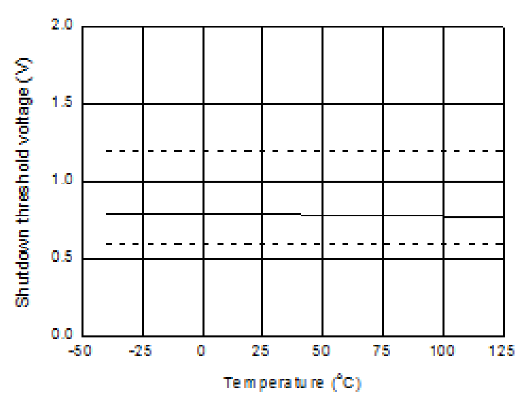


Figure 56. Shutdown Threshold Voltage vs. Temperature

Typical Performance Characteristics

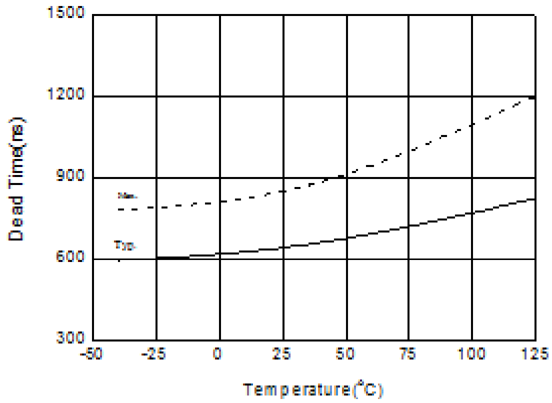


Figure 57. Deadtime vs. Temperature (V_{CC}=V_{BS}=15 V, V_{DT}=1.2 V)

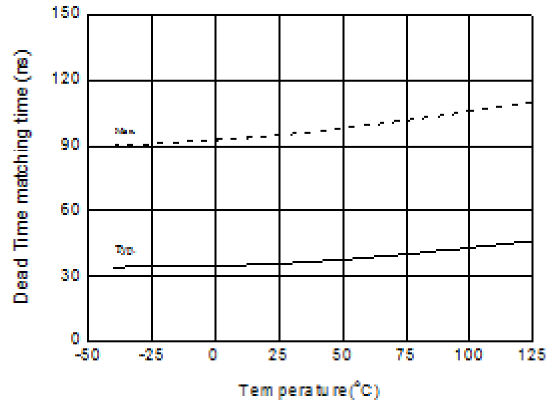


Figure 58. Deadtime Matching Time vs. Temperature (V_{CC}=V_{BS}=15 V, V_{DT}=1.2 V)

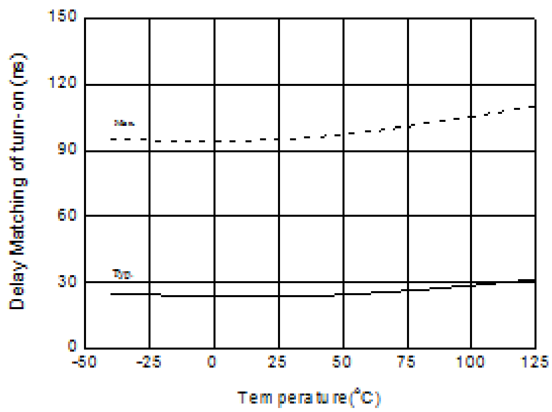


Figure 59. Turn-on Delay Matching vs. Temperature (V_{CC}=V_{BS}=15 V, V_{DT}=1.2 V)

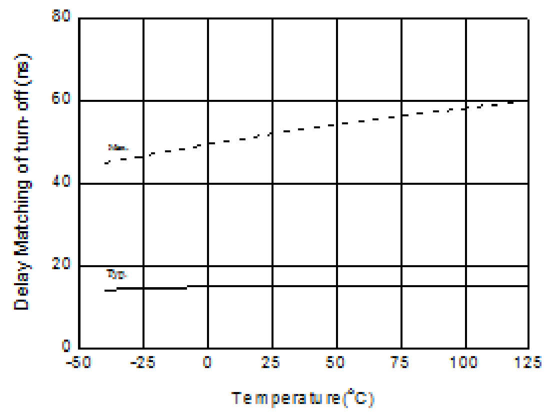


Figure 60. Turn-off Delay Matching vs. Temperature (V_{CC}=V_{BS}=15 V, V_{DT}=1.2 V)

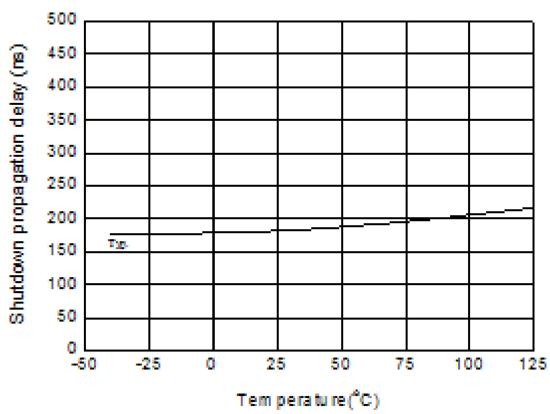


Figure 61. Shutdown Propagation Delay vs. Temperature

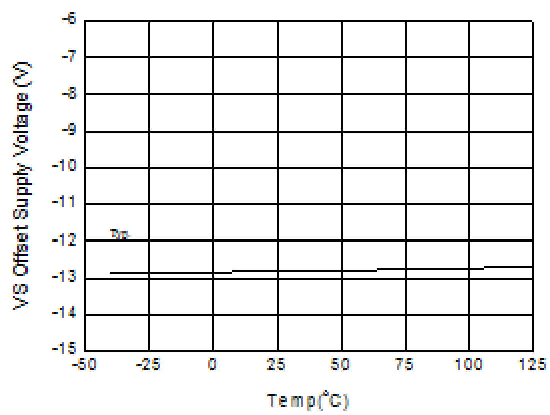
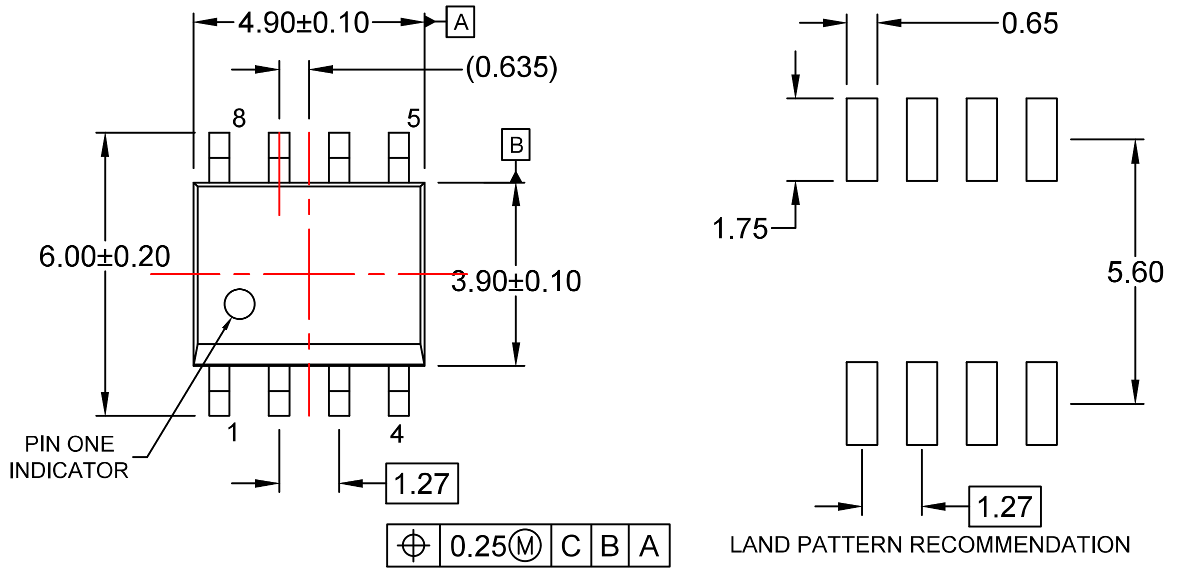
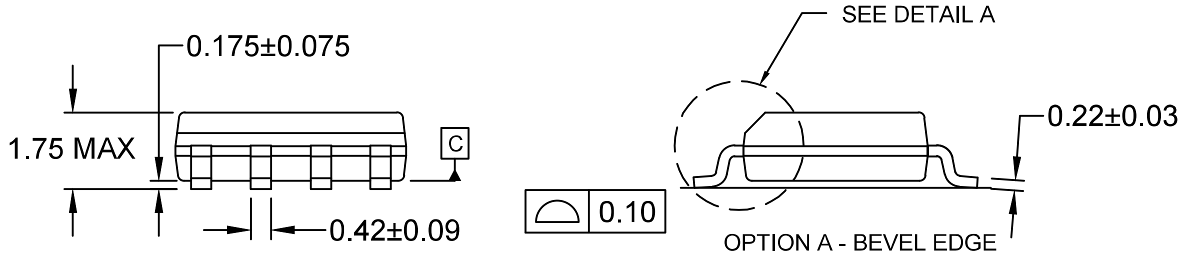
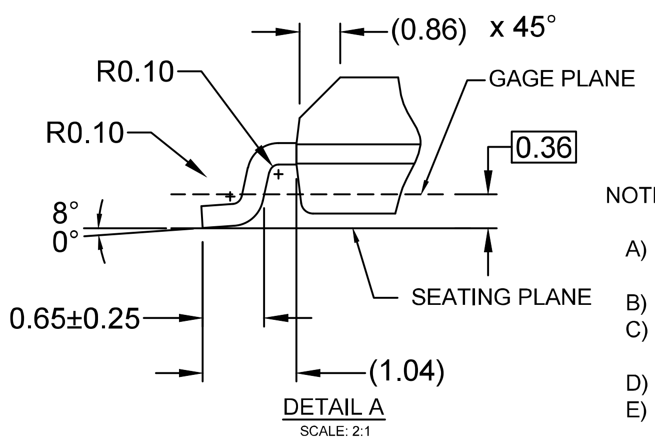
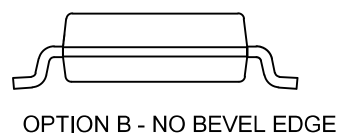


Figure 62. Maximum vs. Negative Offset Voltage vs. Temperature (V_{CC}=V_{BS}=15 V)









NOTES:

A) THIS PACKAGE CONFORMS TO JEDEC MS-012, VARIATION AA.
B) ALL DIMENSIONS ARE IN MILLIMETERS.
C) DIMENSIONS DO NOT INCLUDE MOLD FLASH OR BURRS.
D) LANDPATTERN STANDARD: SOIC127P600X175-8M
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